XC9500 CPLD Power Sequencing

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Introduction

Mixed signal systems - typically 5V/3.3V today - require logic parts that can operate with two power supplies. Xilinx XC9500 CPLDs are designed to operate in either mixed 5V/3.3V systems or 5V only systems. To handle both conditions, care has been taken to assure that designers need not introduce elaborate circuitry to guarantee that 5V and 3.3V power supplies rise or fall in any particular sequence. This application note describes the underlying XC9500 circuitry to give designers the understanding they need to best use these powerful CPLDs.

XC9500 CPLDs are provided with at least two separate power supply pins. V_{CCINT} supplies power for the internal logic, memory and charge pumps. V_{CCIO} supplies power for the output drivers. The I/O supply allows the CPLD to be used in either 5V or 3.3V logic level systems by appropriate attachment. This approach raises the issue of biasing internal structures in nonstandard configurations. Experimentation and analysis of the structures has shown that the devices are safe under all anticipated power sequences. Figure 1 details the basic structure. D1 and D2 are primarily for superior ESD protection of the pins, but are a point of focus for this discussion.
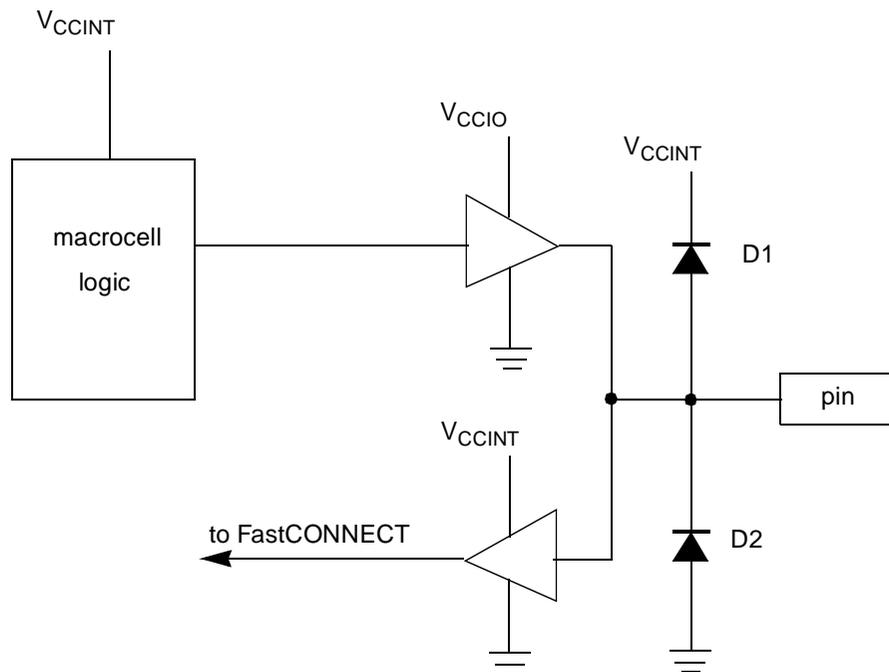
Figure 1:   Simplified XC9500 I/O Cell Structure

Discussion

Two common power supply configurations occur. First, the single supply system involves attaching both V_{CCINT} and V_{CCIO} to the same voltage, 5V +/- 0.25V. The second configuration is V_{CCINT} is attached to 5V and V_{CCIO} is attached to 3.3V. Connecting both supplies to 3.3V is not permitted as well as connecting V_{CCINT} to 3.3V and V_{CCIO} to 5V. We will not consider these two cases. Under these restrictions, it is unlikely that V_{CCIO} and V_{CCINT} will be split up if a 5V

only system is used, but the following analysis should also cover this case. Of specific interest is the case of having V_{CCIO} = 3.3V and V_{CCINT} = 5V which in turn, produces two cases of interest.

Specific concern arises if one of the power supplies is off while the other is on. There are two ways this could happen. Figure 2 shows the situation where V_{CCINT} is turned on and V_{CCIO} is turned off. Figure 3 shows the case where V_{CCINT} is turned off and V_{CCIO} is turned on.

Several factors come into play:

1. the supply impedance (Zsupply)

2. the current limit of external drivers attached to the pin

3. the state of the macrocell logic driving into the output driver.

We will discuss each factor in order, to see how it affects the condition of the CPLD when power sequencing occurs.
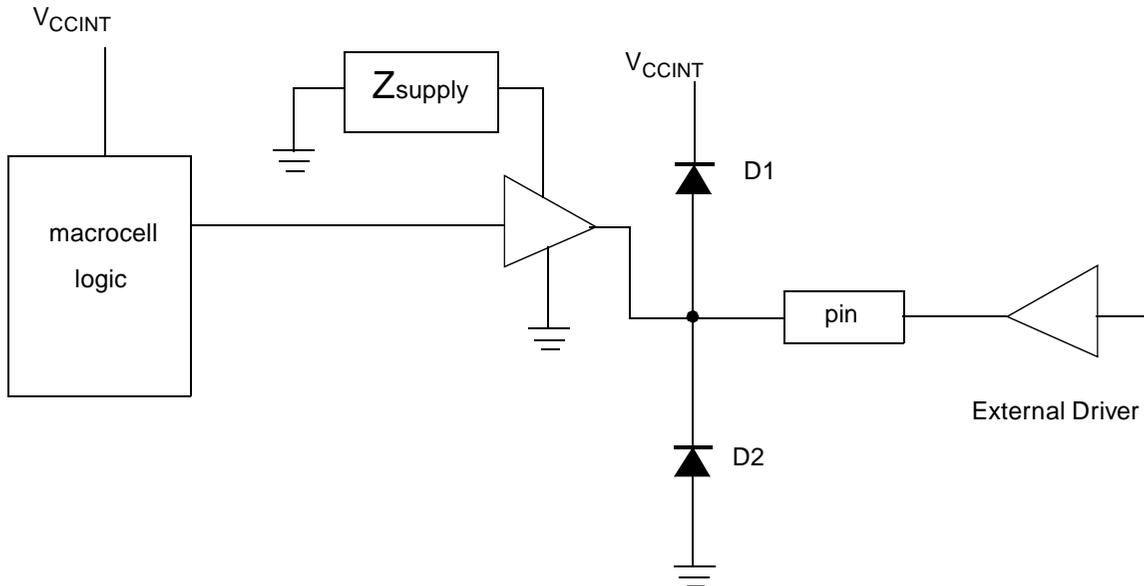
Figure 2: XC9500 Output Driver with VCCIO turned off (Input Receiver not shown)
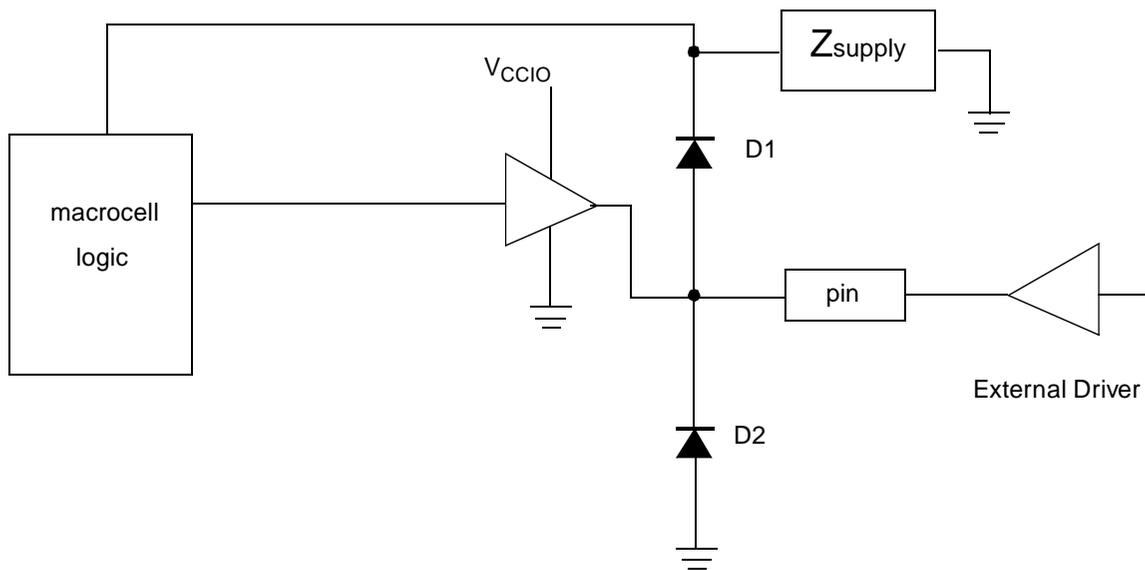
Figure 3: XC9500 Output Driver with V_{CCIO} turned on (Input Receiver not shown)

Supply Impedance

The supply impedance is important because current may flow from the CPLD into the turned off power supply, if a path and an available source (i.e., the other supply) exists. This can occur if an external CMOS chip is driving into the CPLD pin (see Figure 2 and Figure 3).

Most power supplies are either linear (series pass) or switching. In either case, the supply output typically has some silicon impedance and a fairly large capacitor to ground. The supply output capacitor can accept substantial current, but as current arrives, the accumulated charge increases the capacitor voltage. If this turned off supply is initially uncharged, there may be a substantial initial cur-

rent. The initial current self limits as the capacitor voltage approaches the driving voltage (from the pin). The current goes to zero when diode D1 turns off. In this situation, the external driving CMOS chip would be attempting to drive 3.3V with its rated I_{OH}.

Note that for this discussion, we are assuming the power supplies remains attached to the chip pins electrically, whether they are powered up or not.

External Driver Current Limit

The drive limitation of an attached driver comes into play in that it provides the source of current mentioned above. Very few CMOS digital drivers deliver 100 mA, where many may deliver 10 mA. It is conceivable that several drivers at 10 mA could simultaneously drive into the pin a value totaling 100 mA. We will assume that is possible. It would take an amp driven into the pin for several seconds before any diode damage to D1 would occur (Figures 1,2,3). This has been experimentally determined, by grounding V_{CCINT} and applying large currents to the pin

Macrocell State

Figure 4 shows a simplified model of the output driving structure for an XC9500 CPLD. Note the pair of output N-Channel transistors attached to the pin. The inverter permits the output totem pole structure to behave similar to a PMOS-NMOS complementary pair.

If V_{CCINT} is 0, both N1 and N2 may be floating. In this case, it is possible that either or both are turned on or off. If N1 is on and N2 is off, the pin will tend to float to VCCIO. If N1 is off and N2 is on, the pin will tend to float to ground. If both N1 and N2 turn on, leakage current will flow through them, and the pin assumes a value between logic one and logic zero. If both N1 and N2 are turned off, the pin voltage will float at an arbitrary point. The transistor sizes (N1 and N2) are substantially large so that they will not be damaged in any of the four configurations.

If VCCINT is high and the macrocell logic is 1, N2 is turned on and N1 turned off. Macrocell logic can also be low, in which case N2 is off and N1 is turned on. If VCCIO is off, the pin will track whichever transistor (N1 or N2) is turned on. Hence, if A is logic 1 (Figure 4) the pin will go to ground. If A is logic zero, the pin will go to VCCIO. Either way, there is no problem, unless an externally attached part is also driving into the CPLD. This conflict should be avoided by correct logic design.

Conclusion

XC9500 CPLDs are designed to operate in single 5V or mixed 3.3V/5V systems and tolerate any power supply sequencing applied to them without damaging the CPLD, the supply or the external circuits assuming correct logic design has occurred.
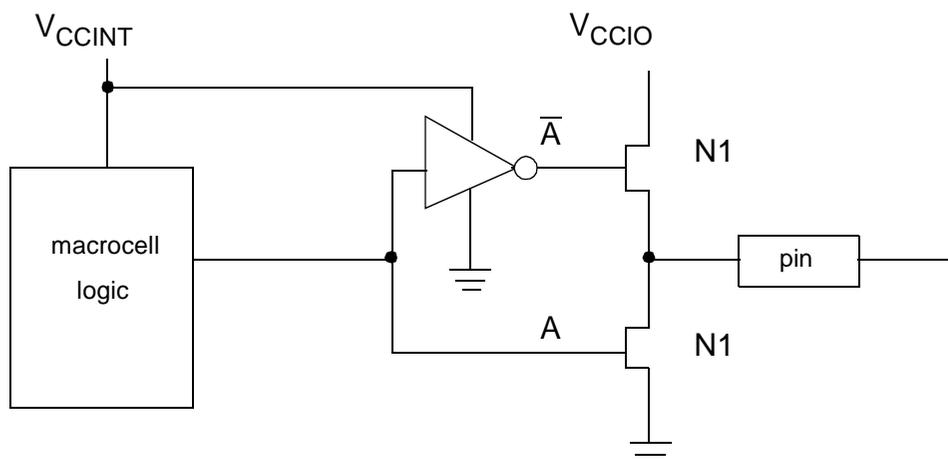
Figure 4: Close-up of Simplified N-Channel Output Stage (Diodes not shown)