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Terminating Unused I/O Pins in Xilinx XPLA1 and XPLA2 CoolRunner CPLDs

Introduction

The CoolRunner™ family of CPLDs are the first PLDs to employ a TotalCMOS™ design methodology. Because these devices are fabricated on CMOS process technology, it is important to consider the options available in terminating unused pins. Allowing unused inputs and I/O pins to float can cause the voltage on the pin to be in the linear region of the CMOS input structures, which can increase the power consumption of the device.

All unused dedicated inputs and JTAG/ISP function pins (when JTAG/ISP is used) on CoolRunner devices must be terminated. For unused I/O pins, some CoolRunner devices have on-chip, programmable, weak pull-down resistors that can be used for termination, but other devices require termination by the user. The table below indicates whether or not a particular CoolRunner device is equipped with the on-chip weak pull-downs.

Termination Options

For devices that do not have the on-chip weak pull-downs, Xilinx recommends using external 10 kΩ pull-up resistors on all inputs or I/Os that are not used. This provides the flexibility to use these pins should late design changes require additional I/O. These unused pins may also be tied directly to V_{CC}, but this will make it more difficult to reclaim the use of the pin should this be needed by a subsequent design revision. It is also acceptable to terminate the pins inside by connecting them to V_{CC} or ground. This must be done in the design entry phase through either schematic or HDL.

When using the JTAG/ISP functions, 10 kΩ pull-up resistors should be used on each of the four mandatory signals. Letting these signals float can cause the voltage on TMS to come close to a logic Low, which could cause the device to enter JTAG/ISP mode at unspecified times.

In CoolRunner CPLDs that have the on-chip weak pull-downs, the software fitter automatically activates them for all unused I/O pins. No current is consumed by the device when the internal pull-down is enabled. If you connect the pin to V_{CC}, the device would only sink current, not source it, therefore there is no pull-down current incorporated into the L_{DD} specification. The pull-down is very weak, and when the pin is connected to 5V, the maximum sink current is less than 10 µA per I/O. Note that the fitting software considers buried macrocells that do not use the pin for an input as unused, and activates the on-chip pull-down. It is our recommendation that the unused I/O pins be left unconnected on CoolRunner 64 and CoolRunner 128 designs.

Disabling the weak pull-downs

In certain cases, a design may require that unused I/O pins be left 3-stated, instead of being connected to the on-chip weak pull-down resistor (Table 1). This is accomplished in software via property statements. The statement

```
xpla property 'tri-state all';
```

disables the pull-down circuit on all of the unused I/O pins. If disabling the pull-down on a single pin is desired, this is done with the statement

```
xpla property 'dingo:12 tri-state';
```

In this case, the weak pull-down on pin 12, to which signal dingo is assigned, is disabled. The symbol name "dingo" need not be declared separately.

Table 1: **Termination Options for XPLA1 and XPLA2 CoolRunner CPLDs**

Part Number	External Termination Recommended	On-chip Weak Pull-down Resistors
XPLA Family		
XCR22V10-/I	X	
XCR032-/I	X	
XCR064-/I		X
XCR128-/I		X
XPLA Enhanced Family		
XCR032C/N	X	
XCR3064A/D		X
XCR5064C/N		X
XCR3128A/D		X
XCR5128C/N		X
XPLA2 Family		
XCR3320C/N		X
XCR3960C/N		X

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/10/00	1.1	Converted to Xilinx format.