Conserving Power With Auto Power Down Mode in SpartanXL™ FPGAs

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Summary

Power consumption plays an important role in battery-powered applications such as laptop computers, electronic toys, wireless devices (i.e. cellular phones) and solar battery powered satellite systems. SpartanXL FPGAs are designed with segmented routing, 3.3-V operation and advanced process technology to meet the needs for low power and high performance. This application note shows how to reduce power consumption by selectively disabling portions of the design that are not required all the time. This approach is particularly useful for the devices which must be operating all the time. This application note discusses different strategies for reducing the supply current (I_{CC}) incrementally for an operating device.

Xilinx Families

SpartanXL Only

Introduction

The SpartanXL family is built with segmented architecture to combine low power consumption with high performance and density. The device power depends on a number of factors including: supply voltage, device architecture, resource utilization (number of interconnects, logic cells and IO cells used), clock frequency, signal toggling rate (percentage of signals switching), number of outputs being used and the load each output is driving.

Low Power Applications

The low supply current possible is especially useful for products that must use power as efficiently as possible. This applies to battery-powered equipment such as notebook computers, digital cameras, camcorders and cellular telephones. Satellites, which must make the best possible use of the limited power from solar panels, serve as yet another example. Low power offers additional benefits such as low operating temperature, low cost packages and high device reliability.

Power Down Modes

There are two kinds of power down modes that can be used to conserve power in SpartanXL FPGAs. They are: manual mode and the automatic mode. Both of them provide low quiescent (standby) current down to 100 µA while retaining the bit map (i.e., configuration data) with which the device had been configured.

In the manual mode, the device is fully inactive, the register data is lost, and the activation and de-activation of the power down mode is controlled by the $\overline{\text{PWRDWN}}$ pin. For more information on this mode, refer to the application note *XAPP124, Using Manual Power Down Mode With SpartanXL™ FPGAs* at http://www.xilinx.com/xapp/xapp124.pdf on the Xilinx web site.

In the automatic mode, all the features of a design which consume relatively a large amount of power are independently controlled to reduce the supply current incrementally. This reduction in supply current can be accomplished without using global reset. As a result, the register data is maintained through out power down period. The device remains active as the inputs are connected and the outputs are not tri-stated. This application note discusses each of these features in detail in the following section.

Power Saving Techniques

Power consumption is a sum of static power and dynamic power. The static power is mostly due to normal leakage currents in an inactive device. The dynamic power is due to the switching of internal nodes and inputs and outputs in an active device. The techniques that can be used to selectively lower the overall power are described below.

Saving Power with Low Voltage Thresholds

The strategies discussed in this section provide the greatest power savings when 3.3V signal standards are used. Where possible, disable the “5V tolerant I/Os (SpartanXL only)” option when implementing the design. The option can be found in the Configuration Options template, part of the Xilinx development software. Selecting 5V tolerance (the default), enables a circuit that draws a small amount of additional current and protects the input buffers from large signals. Use of the 3.3V signal standards compatible with the SpartanXL inputs, LVTTL, LVCMOS and PCI3V standards, all allow for lower I_{CC}, since none of these require 5V tolerance.

Saving Power at the Inputs

The inputs to most CMOS devices draw little I_{CC} current (quiescent or dynamic). When present, pull-up and pull-down resistors account for most of the current drawn by the inputs. These resistors typically range from 50KΩ to 100KΩ. The voltage level applied to the input, V_{IN}, determines how much current the resistor draws. In order to save power at the inputs to the device, avoid instantiating these resistors wherever possible in the design.

Pull-up resistors are enabled by default for all unused I/Os. Such pins should be tied to V_{CC} outside the device. This action will force the current through the pull-up to zero.

With no pull-up and pull-down resistors, any remaining current drawn by an input is known as leakage current (I_L), which ranges from 1 µA to 4 µA typical. Like other CMOS ICs, the cross-current that occurs in the input circuits of the SpartanXL FPGA is lowest when a voltage of V_{CC} or GND is applied to the pin. This current increases as the voltage approaches the switching threshold (1.5V for LVTTL). When power savings are desired, drive as many signal inputs as possible to either the GND or the V_{CC} rail.

Achieving a DC State

Another way to save power is to keep all signals within the device from switching. This DC state is accomplished by holding the inputs of the SpartanXL device at a static, defined logic level. This measure effectively reduces the dynamic power level of the device to zero. In many designs, a major portion of the total dynamic power demanded by the SpartanXL device is due to its clock tree, which consists of all the interconnects that distributes the clock signal internally. Power drawn varies according to how extensive the tree is. Pulling the clock input to a static logic level is an important way to save power, especially when the clock frequency is high.

Avoiding Unnecessary High Frequency Clocks

Power consumption is proportional to operational frequency. Running the clock at a frequency higher than necessary wastes valuable battery power. Do not operate the device at higher frequencies, unless it is really required. In some cases, only a portion of the design needs to be running at higher frequencies at any given time. In that scenario, slow down or stop the frequency for the remaining portions. To save the power due to transition on output flip flops, use the Clock Enable (CE) signal for all the flip-flops in the design. All the clock transitions are ignored when the CE signal is inactive and so the output flip flops do not toggle. Activate the CE signal when the registered outputs need to be operating.

Reducing the Number of Columns where the Clock is Driving

The current required to drive varies with number of columns the clock is driving in the device. Reducing the number of columns should reduce the current requirements. For example, if it is possible to combine the flip-flops in two half or partially filled columns to just one column, the current should be reduced. Although the reduction may not be exactly by half, but is a considerable amount.

Disabling the Outputs

The amount of I_{CC} required for a SpartanXL output to drive a simple CMOS load (with no pull-up and the pull-down resistors) will typically be on the order of 0.10 µA. The easiest and most effective way to save power at the outputs is to use the Global Tri-State (GTS) net. This feature is available when a STARTUP symbol is instantiated into the design and its GTS signal is assigned to an I/O of the FPGA. The signal can be either active-High, or, through the addition of an inverter, active-Low. When saving power is desired, asserting the signal will put all outputs into a high impedance state. In cases where disabling all outputs at once to save power is impractical, it is also possible to selectively disable outputs simply by instantiating an output buffer with a tri-state control input (BUFT) where needed.

Two features of the I/O structure that draw significant supply current are pull-up and pull-down resistors. To save power at the outputs (as well as at bidirectional I/Os), the recommendation is the same as for inputs: wherever possible avoid instantiating both kinds of resistors.

Reducing Loading on the Outputs

In many applications, excessive loading on the outputs significantly increases the power. If possible, reduce the load on the outputs to save considerable amount of power.

Reducing External Capacitive Loading

Power dissipation is also proportional to capacitance. The capacitance constitutes of internal and external capacitance. The lumped internal capacitance is associated with the power dissipated internally by the device. The external capacitance is associated with power dissipated outside the device. The internal capacitance is beyond your control as it depends completely on device characteristics. However, the external capacitance is usually a function of PCB traces loading and other IC loads, which are constrained by other aspects of the design. Keep excess capacitive load to a minimum where possible.

Table 1: Revisions

Version	Description
3/22/99	Rev. 1.1 Modified the title to “Conserving Power with Auto Power Down Mode in SpartanXL FPGAs”. Added the section “Power Down Modes”.