FPGAs Can Be an Effective Alternative to Mask Gate Arrays

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In this fast-paced electronics industry, gate array engineers are under increasing pressure to produce new ASIC designs ever more quickly. As traditional masked gate arrays decline in usage, a new generation of programmable devices have become a viable alternative for the gate array user.

The new "ASIC Replacement" FPGAs have continued to narrow the price gap with mask ASICs while maintaining the user advantages of quick production and in-system reprogrammability. These FPGAs have begun to replace mask gate arrays in traditional ASIC volume applications, from networking encryption engines to PC adapters to digital camcorders.

In this article we examine recent advances in programmable technology and the advantages of the new ASIC Replacement FPGA.

For a list of Spartan and SpartanXL devices, see the *Xilinx Spartan Series* Table on page 5 in the "3.3V SpartanXL FPGA Series" article.

ASIC Replacement FPGAs

The Xilinx Spartan Series FPGAs were created to provide a cost effective and flexible replacement for low-end (<40K system gates) ASICs in volume production. These new FPGAs offer the ASIC designer the advantages of in-system reprogrammability at prices that are competitive with masked gate arrays. To become an effective ASIC solution, the Spartan Series had to substantially reduce die-size over the previous generation FPGAs while measurably improving gate-area density and system performance.

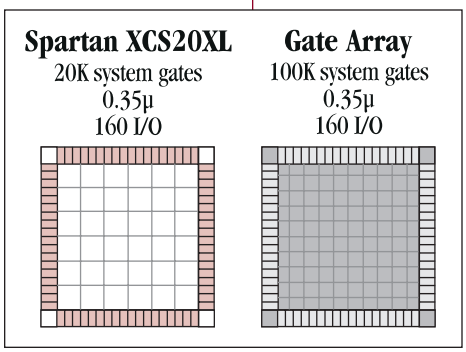

Figure 1. Spartan FPGAs match die size with mask gate arrays.

Although FPGAs have historically lagged the ASIC industry by one or two fab-process generations, current Spartan Series FPGAs were able to surpass most of today's gate arrays by employing a leading-edge, multi-feature size 0.35µ/0.25µ technology. In the past, a larger die size was necessary to provide sufficient logic density for typical FPGA designs but caused FPGAs to be priced out of range for higher volume production.

Because the high-end Xilinx FPGAs (such as the Virtex Series) contain more transistors (75 million) than the Pentium II microprocessor, Xilinx wafer foundry partners have chosen these complex devices to debug new fab processes, replacing DRAMs as the technology driver. Becoming a fab process driver means that Xilinx FPGAs will remain on the leading edge of process technology for years to come.

FPGAs Close the Price Gap

The SpartanXL family (3V version) is currently the lowest cost FPGA family in the industry. The entire Spartan/SpartanXL Series incorporates ASIC-like features such as dual-port synchronous on-chip memory and supports frequencies up to 80+MHz.

The key to the Spartan family's low production pricing is an "I/O pad-limited" die size. "I/O pad-limited" means that a die is reduced to the limits imposed by the I/O bonding pads. Pad-limited enables the Spartan Series FPGA die to be cost equivalent to most mask gate arrays of up to 205 I/O pins. With Spartan or SpartanXL prices starting at $2.95 (84 PLCC, 100K units, -3 speed), the series is able to realistically compete with mask gate arrays for production based upon the same I/O count.

For example, the 160 I/O SpartanXL S20XL, shown in **Figure 1**, has a comparable die size and cost as the 160 I/O 0.35µm gate array, even though the gate array contains a denser architecture (and higher gate count). By sizing the die at the pad-limits, the FPGA cost can be equivalent to most gate arrays.

Lower Manufacturing Cost

Because Spartan Series FPGAs were designed for low power consumption, inexpensive plastic packages can be used to help keep manufacturing costs low. Other production savings accrue from a

streamlined test methodology, built-in self-test features, and shorter test times. The combination of lower manufacturing overhead and small die-size eliminate cost barriers and enables Spartan Series FPGAs to be effective for both prototyping and for mass production.

FPGA Production Parts "Off-the-shelf!"

It is paramount to attain the best development time-to-production because today's product life cycles are often brief (9-18 months). Programmable logic is uniquely able to support both rapid prototyping and a quick ramp to full manufacturing. For many Xilinx customers the immediate availability of production is the most important benefit of programmable logic. After development, early production shipments are critical to market acceptance.

When FPGAs are used in production, marketing channels are quickly stocked for initial sales and new product revenue flow begins. Because the standard ASIC has an 8-16 week production leadtime, a 3-4 month sales delay would substantially decrease revenues and profits throughout the life of the product (see **Figure 2**). By using FPGAs in production; however, your market penetration is immediate.

The well-known McKinsey study found that a six-month delay costs one third of the profits over the lifetime of the product.

FPGA-to-ASIC Conversions

FPGA-to-ASIC conversions have been a popular approach to reduce unit production costs. However, it has become more difficult to cost justify these conversions in lower-density designs because of the new low price FPGAs along with the flexibility that FPGAs offer in today's quickly changing markets.

Conversion to a lower density ASIC means losing FPGA advantages of "off-the-shelf" production deliveries and simple field software updates, while incurring re-design risks (see **Figure 3**). Conversion costs such as NRE, silicon re-spins, test vectors, new device characterization, and internal engineering costs, usually outweigh the nominal unit cost difference between FPGAs and ASICs.

In higher density designs, using an ASIC that is crafted to exactly mirror the FPGA features can minimize the costs and the associated re-design risks. For example, the Xilinx HardWire™ family

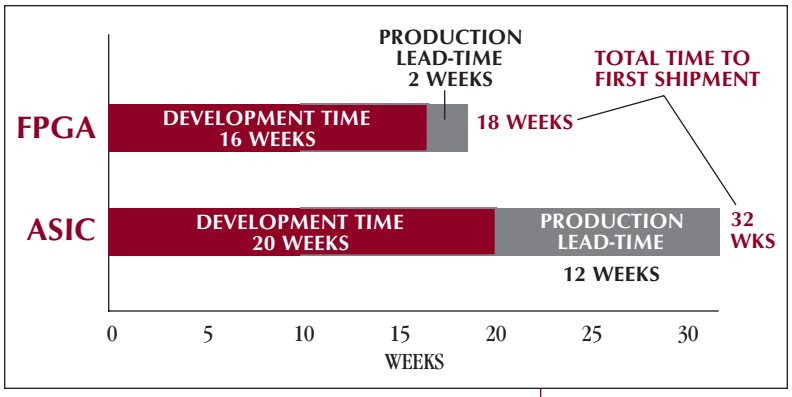

Figure 2: FPGA beats ASIC by more than 3 months to first customer shipment!

offers exact ASIC replacements for our higher-density FPGAs, making conversion very quick, easy, and inexpensive.

However, for most other manufacturers' FPGAs, the conversion time-to-production is frequently under-estimated. The time from start to full production typically exceeds four months. The common milestones are:

- Conversion/internal engineering time — three weeks
- Prototype fab time — three weeks
- Full production deliveries — 10 weeks

In total, 16 weeks are spent before production is fully ramped and the transition to the ASIC is complete. When a short product life or a mid-life product enhancement is likely, conversions become worthless.

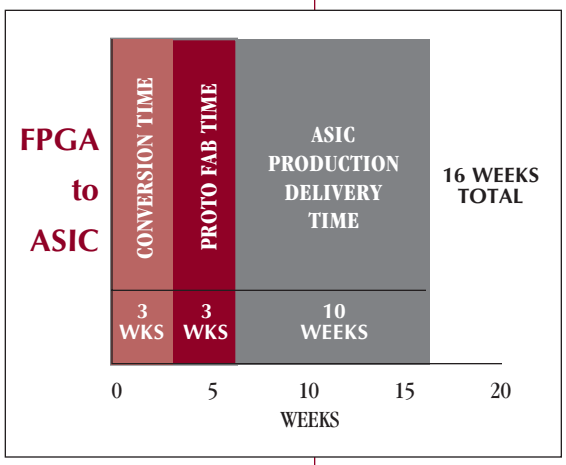

Figure 3: FPGA to ASIC conversion to production takes at least four months.

Conclusion

There are compelling advantages to use programmable logic for both development and production. Today's FPGAs support standard Verilog and VHDL design flows that help ASIC designers transition to programmable logic. Advanced process technology has leveled the playing field, and allowed FPGAs to be very price competitive with low-density gate arrays. When ASIC users now consider pricing, time-to-production, and reprogrammability, the preferred ASIC technology becomes the new Spartan Series FPGAs.