# APPLICATION NOTE

**Xilinx has acquired the entire Philips CoolRunner Low Power CPLD Product Family. For more technical or sales information, please see: www.xilinx.com**

## XAPP 301

# Using sum of products control terms in Philips CoolRunner™ CPLDs

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## DOCUMENT SCOPE

This document describes how to use sum of products equations to drive control terms in Philips CoolRunner™ CPLDs. The procedure for creating the control term is illustrated, and design considerations such as timing and register use are discussed. The concepts presented here apply to all Philips CoolRunner™ CPLDs.

## INTRODUCTION

Under normal use, Philips CoolRunner™ CPLDs provide either direct product term or sum term support for asynchronous resets, asynchronous presets, output enables, and clocks. Sum of products control terms are not directly supported. Figure 1 shows a block diagram of the XPLA logic block used in Philips CPLDs.

Note the control terms located above the PAL array. The block diagram shows there are six control terms available to each logic block, and each one can be either a product term (all ANDs) or a sum term (all ORs) comprised of the 36 inputs into the Zero–Power Interconnect Array (ZIA). Unlike the logic available for each macrocell output, there is not an additional OR gate directly in front of the macrocell that allows control terms to support sums of products. For example, control terms like

OUT_EN = A & B & C & D

or

RESET = A # B # C # D

are directly supported in Philips CPLDs, but control terms like

PRESET = (A & B) # (C & D)

are not. The & and # symbols represent logical AND and OR, respectively.

In reality, there is a single product term available for each control term, and OR functions are Demorganized to change them into AND functions. Each control term is actually implemented as a product term that uses either a buffered or inverted path into the macrocell (see Figure 2).

Consider the RESET control term equation. Using Demorgan's Theorem, this will be altered during logic synthesis to

RESET = ! ( !A & !B & !C & !D)

which can then be implemented using the product term and the inverted path into the macrocell.

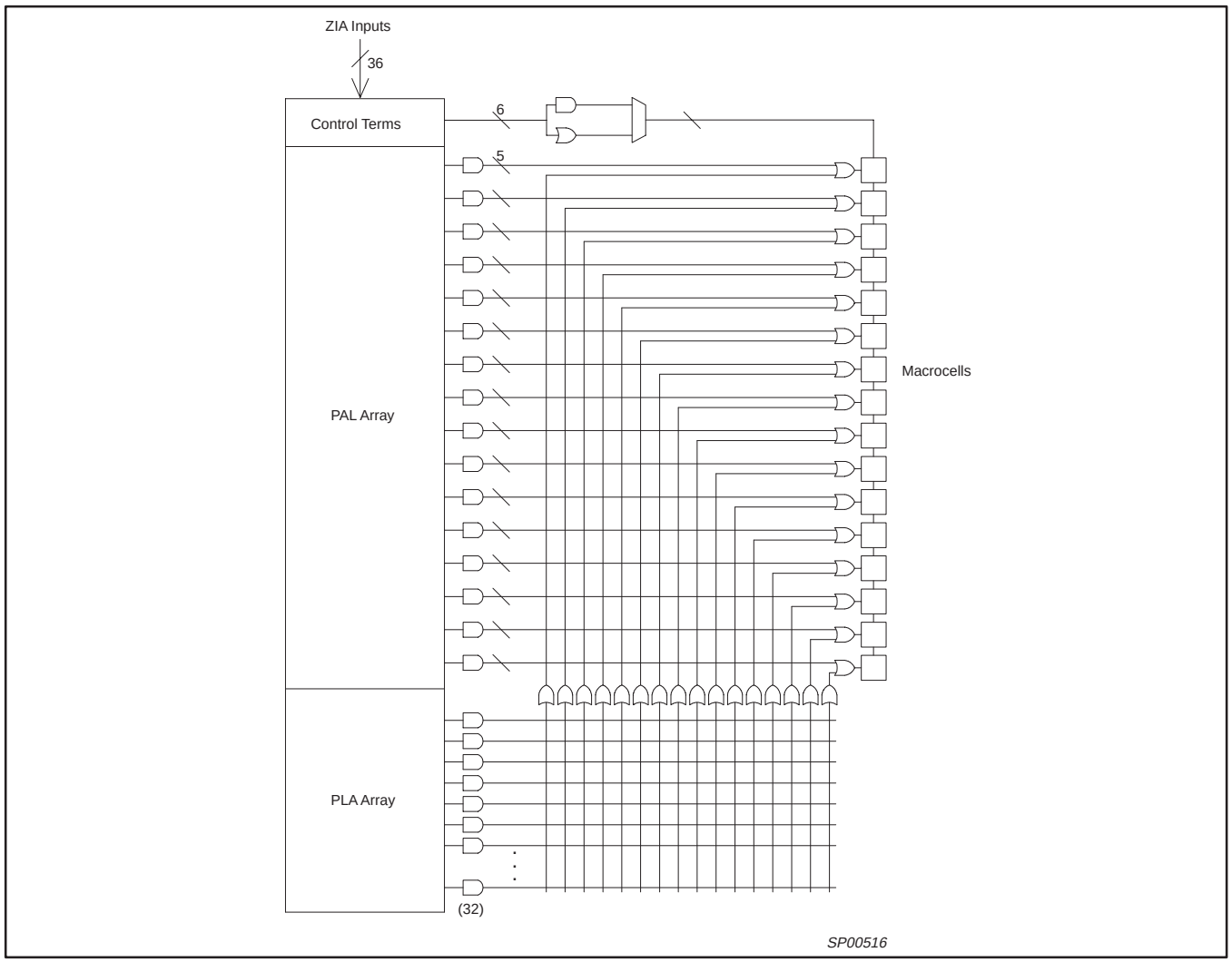


**Figure 1 Philips XPLA Logic Block**

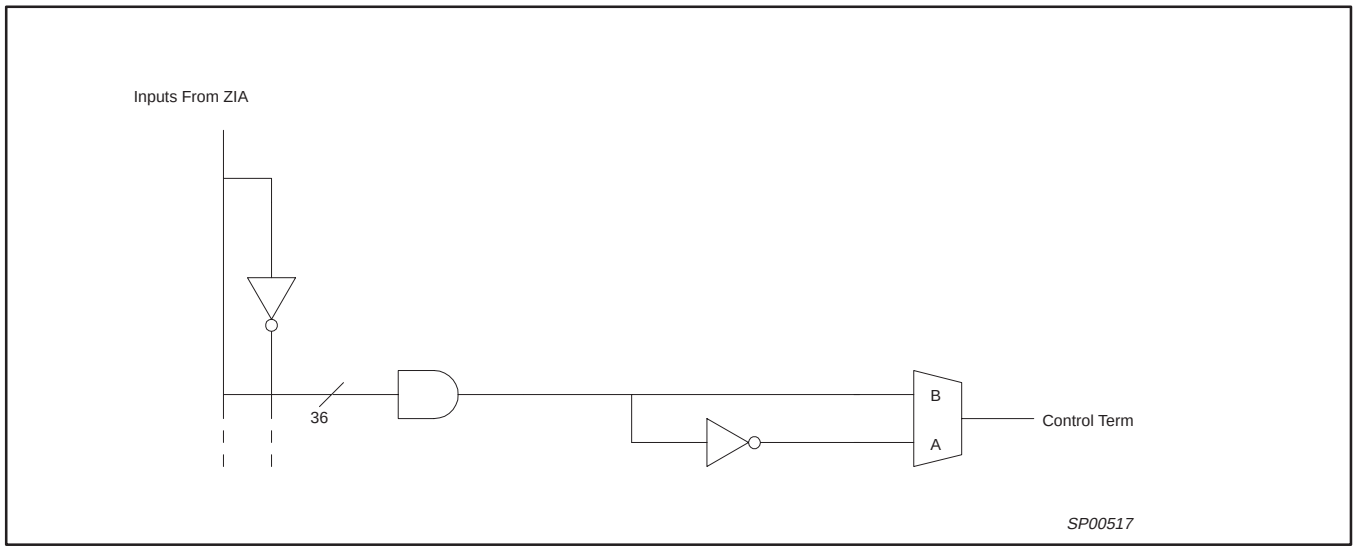


**Figure 2. Product Term Implementation for Control Terms in Philips CPLDs.**

## IMPLEMENTING SUM OF PRODUCT CONTROL TERMS

To use sum of product control terms in Philips CoolRunner™ CPLDs, you must use an intermediate node to generate the sum of products, and then assign this intermediate node to the control term. In this way, the control term appears to the logic compiler and optimizer to be a single input (the intermediate node) to a product term. For example, consider the PRESET control term shown below:

PRESET = (A & B) # (C & D).

This cannot be directly implemented, but if the control term is assigned to an intermediate node like

PRE_NODE = (A & B) # (C & D)

and then assigned to preset like

PRESET = PRE_NODE,

then the sum of products control term could be implemented.

In order to make this work, the intermediate node cannot be collapsed during optimization of the logic. It must be preserved so that the sum of products is resolved at the node and the output of the node is used as the single input to the control term. Otherwise, the intermediate node will be removed from the design and the fitter will attempt to apply a sum of products directly to a control term. This condition will result in a fatal error from the design fitter.

Preventing a node from being collapsed during logic optimization is usually done by attaching an attribute to the node that tells the logic optimizer to preserve this particular node. The procedure for preserving nodes varies depending on the design system you are using. For example, if you are using Philips XPLA Designer and the Philips Hardware Description Language (PHDL), you would assign a ‘keep’ attribute while declaring the intermediate node. The declaration of the intermediate node and the assignment of the node would look something like

```
module EXAMPLE

declarations

A, B, C, D          pin;

PRE_NODE            node istype ‘com, keep’;

OUTPUT              pin istype ‘reg’;

equations

PRE_NODE = (A & B) # (C & D);

OUTPUT.AP = PRE_NODE;
```

These statements assign the sum of products control term equation to the intermediate node, PRE_NODE, and then assign PRE_NODE to the asynchronous preset of the signal OUTPUT. Figure 3 shows schematically how the above logic assignments are implemented inside the device.

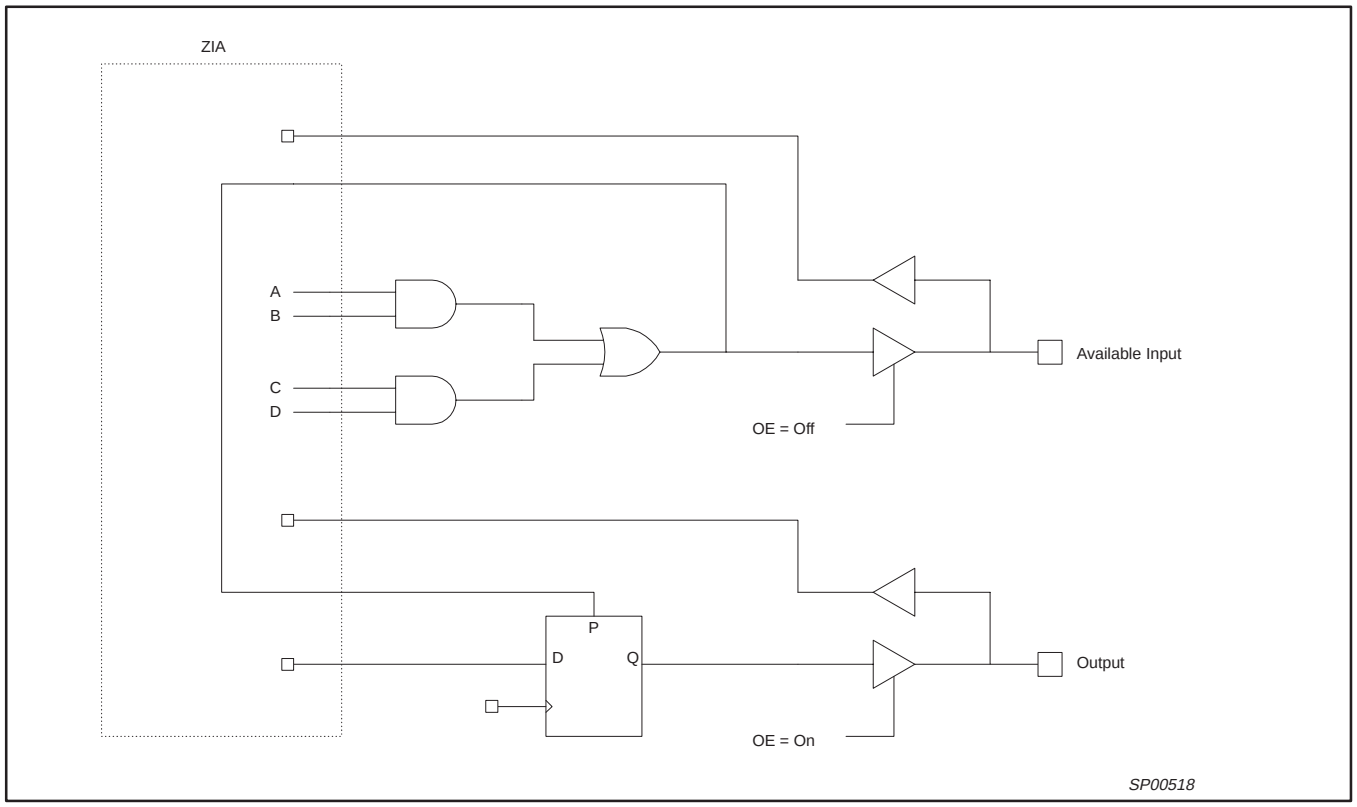


**Figure 3 Schematic Representation of Sum of Products Control Term Implemented in Philips CPLD.**

As you can see, PRE_NODE is preserved in the design and the sum of products is resolved there. The output of the node then feeds back to the ZIA and is used as a single input to a control term.

## DESIGN CONSIDERATIONS

There are design trade–offs that must be considered when implementing sum of product control terms. First, as shown in figure 3, the creation of the internal node uses one of the available macrocells for resolution of the sum of products. This node use results from specifying that the node must not be collapsed, and is necessary to prevent the compiler and fitter from applying the sum of products directly to the control term. Note, however, that the node uses the internal feedback path (before the output buffer) for sending the sum of products result back to the ZIA. Whenever buried nodes are created in this manner, the output buffer is disabled and the node signal is not propagated to the output pin. This allows the pin associated with the macrocell where the intermediate node resides to be used as a dedicated input.

The other consideration is the fact that the time it takes for a sum of products control term to have an affect is longer than the time it takes for a product term or sum term control term to have an affect. Figure three shows that in addition to propagating through the ZIA and the logic array like ordinary control terms, sum of product control terms must first pass from the input to the internal feedback node, and then proceed through the same path as normal control terms. Thus, whenever sum of product control terms are used, the time specified in the data sheet for the asynchronous reset, asynchronous preset, or output enable to take affect should be lengthened by tPDF, the amount of time it takes for a signal to propagate from the input to the internal feedback.

## TECHNICAL SUPPORT

For more information, contact the Philips CPLD Technical Support Line at 1–888–COOLPLD (1–888–2665753) or 505–858–2996; or send email to coolpld@scs.philips.com.

**NOTES**

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