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XAPP325
Understanding CoolRunner™ clocking options

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UNDERSTANDING COOLRUNNER™ CLOCKING OPTIONS

The CoolRunner™ family of CPLDs includes versatile clocking options that include both synchronous (external) and asynchronous (internal, equation-based) clocking and selectable clock polarity at every macrocell. This application brief describes in detail these clocking options, and shows how to access these features using Philips XPLA Designer. We also detail how to synthesize 'soft' flip-flops and latches for those instances where these devices can be useful.

Table 1. Clock resources by device type

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Dedicated Input Pin Clocks</th>
<th>I/O Pin Clocks</th>
<th>Control Term Clocks</th>
<th>Total Clock Resources</th>
</tr>
</thead>
<tbody>
<tr>
<td>PZx032–/I</td>
<td>clk0</td>
<td>clk1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>PZx032C/N</td>
<td>clk0</td>
<td>clk1</td>
<td>2 x 2 logic blocks = 4</td>
<td>6</td>
</tr>
<tr>
<td>PZx064–/I</td>
<td>clk0</td>
<td>clk1, clk2, clk3</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>PZ3064A/D</td>
<td>clk0</td>
<td>clk1, clk2, clk3</td>
<td>2 x 4 logic blocks = 8</td>
<td>12</td>
</tr>
<tr>
<td>PZ5064C/N</td>
<td>clk0</td>
<td>clk1, clk2, clk3</td>
<td>2 x 4 logic blocks = 8</td>
<td>12</td>
</tr>
<tr>
<td>PZx128–/I</td>
<td>clk0</td>
<td>clk1, clk2, clk3</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>PZ3128A/D</td>
<td>clk0</td>
<td>clk1, clk2, clk3</td>
<td>2 x 8 logic blocks = 16</td>
<td>20</td>
</tr>
<tr>
<td>PZ5128C/N</td>
<td>clk0</td>
<td>clk1, clk2, clk3</td>
<td>2 x 8 logic blocks = 16</td>
<td>20</td>
</tr>
<tr>
<td>PZ3960C/N</td>
<td>clk0–clk7</td>
<td>0</td>
<td>2 x 48 logic blocks = 96</td>
<td>104</td>
</tr>
</tbody>
</table>

Figure 1.
I/O Pin Clocks
The second type of clock source comes from clock pins that are associated with I/O macrocells. There is one of these input types on the CoolRunner™32, and three of these on the CoolRunner™64 and CoolRunner™128 devices. These clock inputs have more versatility than the dedicated input type. In the synchronous clocking configuration (Figure 2), the output buffer is set to the High-Z state, and the I/O pin is propagated to the associated clock network and the logic array (via the ZIA). This behaves identically to the dedicated input clock in all respects. The Macrocell is still usable for internal ‘buried’ logic in this configuration. Configuration of the macrocell for buried logic and disabling the output buffer is automatically done by the design software.

The I/O pin clocks can also be used to generate asynchronous ‘equation-based’ clocks. Figure 3 shows that in this configuration the output buffer is enabled. Therefore, the logic that is generated in the macrocell is propagated to the associated clock network, the I/O pin, and is also fed back into the logic array. Since macrocells in the XPLA architecture can deploy as many as 37 Sum of Product equations, the resulting clocking equation in this configuration may be much more complex than in competing devices that have only a single product term available for asynchronous clocking. It also significant to note that the asynchronous clock that is generated is observable on the associated I/O pin. For this reason, the associated pin should not be terminated by tying to ground or VDD. The timing for asynchronous clocks is different in that the Tco time is extended by the amount of time that it takes for the signal to propagate through the array and reach the clock network, and the Tsu time is reduced. This time is dependent on whether the PAL or PAL+PLA paths are used to generate the equation. For clock equations that use only the PAL path, Tco is extended by Tpdf_pal. Using the PAL+PLA path extends Tco by Tpdf_pla.

Control Term Clocks
The third type of clock source is provided by the control terms in each logic block. These types of clocks available only in the XPLA Enhanced and XPLA2 device families. Figure 4 shows the macrocell architecture for each of these families. In the XPLA Enhanced device family (Figure 4a), there are six control terms in each logic block, and in the XPLA2 device family (Figure 4b), there are eight control terms in each logic block. As shown for the XPLA Enhanced family, two of the six control terms are shared by the output enable multiplexer and the clock source multiplexer. These control terms can be used as an output enable, a clock, or both. The XPLA2 family has two extra control terms that are dedicated to only the clock source multiplexer. These clocks can be individually configured as any PRODUCT term or SUM term equation created from the 36 signals available inside the logic block. If a SUM-OF-PRODUCTS equation is required, it must be implemented in a macrocell and then fed-back into a control term through the ZIA (see the application note Using Sum of Products Control Terms for more information).

Each control term clock is available to all the macrocells within a logic block, but it must be duplicated on another control term if the same clock is used in different logic blocks. These clocks are not attached to a low-skew clock network, and they must pass through the interconnect array and a single product term before reaching the flip-flop. Therefore, Tco time is extended by the amount of time that it takes for the signal to propagate through the appropriate array, and the Tsu time is reduced. Unlike the other two types of clock sources, control term clocks are not associated with specific pins and may be assigned to any I/O or dedicated input.
Figure 4. Macrocell Architectures

XPLA Enhanced Family Macrocell Architecture

XPLA2 Family Macrocell Architecture
Using XPLA Designer to generate clocks
XPLA Designer will automatically assign clocks to the correct pins/macrocells based on the context of the clocking desired. Synchronous clocks are generated by declaring the name you want for the clock, and simply using this by itself in a .clk equation, as shown below for the clock signal we’ve created called CLOCK_1.

```vhdl
Module DEMO
Title 'A simple design:3-bit counter'
CLOCK_1 pin;
bit2..bit0 pin istype 'reg';
count = [bit2..bit0];
equations
    count.CLK = CLOCK_1;
    count = count.q + 1;
end;
```

Asynchronous clocks are also easy to generate. Again, simply declare the variables that will make up the equation that the clock will be based upon. In the example below, we are generating a clock from the variables A, B, and C. Then in the .clk equation, we write any expression we want for the clock. The software will assign asynchronous clocks (product term or sum term) first to the control term clocks, until all available control term clocks are used. Then the design software will assign asynchronous clocks to a macrocell, enable the output buffer, and feed the clock equation to the register through the dedicated clock network as in Figure 3.

```vhdl
Module DEMO2
Title 'A simple design:3-bit asynch counter'
A,B,C pin;
bit2..bit0 pin istype 'reg';
count = [bit2..bit0];
equations
    count.CLK = (A&B) # C;
    count = count.q + 1;
end;
```

Soft Flip-Flops
For the rare cases where there are too few clocks in a CoolRunner™ device to implement a large number of input registers (for example), soft D flip-flops or transparent latches may be useful. The following examples illustrate the generation of a transparent latch and D Flip-Flop using only the gates in the logic array. It is important to note that the ‘clock’ width must be longer than $T_{pd}$!

```vhdl
Module Soft_Latch
Title 'Soft Latch w/ Latch Enable -'
D pin;
LE pin;
/
Q pin istype 'com,keep,retain';
equations
    Q = (D & LE) # (Q & !LE) # (D & Q);
end
```

```vhdl
Module Soft_D2
Title 'Soft D Flip Flop-Rising Edge triggered -'
D pin;
CLK pin;
IL node istype 'com,keep,retain';
Q pin istype 'com,keep,retain';
equations
    IL = (D & !CLK) # (IL & CLK) # (D & IL);
    Q = (IL & CLK) # (Q & !CLK) # (IL & Q);
end
```
Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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