A 400MHz Frequency Counter

This article describes a full-featured, single-chip frequency counter that operates at 400 MHz, consumes only 130 mW at the maximum input frequency, and occupies less than 90% of an XC4002XL, the smallest XC4000 family member.

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The conventional block diagram of the frequency counter is shown in Figure 1. The heart of the design is a six-digit decade counter that is driven by a programmable pre-scaler. This pre-scaler is gated by a half-second pulse, and the frequency is determined from the number of input cycles counted in this period.

The time base for the counter is created from a standard 32,768-Hz crystal oscillator. Its output is divided to provide the half-second gating pulse. In a short interval between the gating pulses, the contents of the decade counter are decoded for the 7-segment displays, and the segment states are captured.

The frequency counter has a three-decade auto-ranging capability. At the end of each half-second period, the count value is examined to determine if it is in range. If it is not, the amount of pre-scaling is adjusted for the next half-second period. Hysteresis is built into the auto-ranging circuits to stop any display hunting when the input frequency is at a range boundary.

When the input frequency falls below the auto-range capacity, the display of leading zeros is suppressed. The outputs to the liquid-crystal display are modulated at 128 Hz to provide AC drive directly to the LCD.

Semi-synchronous Design

The design uses a cascade of synchronous 2-bit state machines, with each stage clocking the next asynchronously. This design style was influenced by the XC4000XL architecture . Each CLB provides two flip-flops that share the clock. A fully asynchronous design would waste half of the flip-flops since there is no individual clock access.

Typically, the 2-bit state machine is a modified Johnson counter. The 4-input function generator that precedes each of the flip-flops has three uncommitted inputs that can be used to modify the state sequence.

Detailed Design Description

The first stage of the counter is the most critical. At 400 MHz, it is operating at the maximum possible toggle frequency, and the design must, therefore, be kept as simple as possible.

Frequency Counter Block Diagram

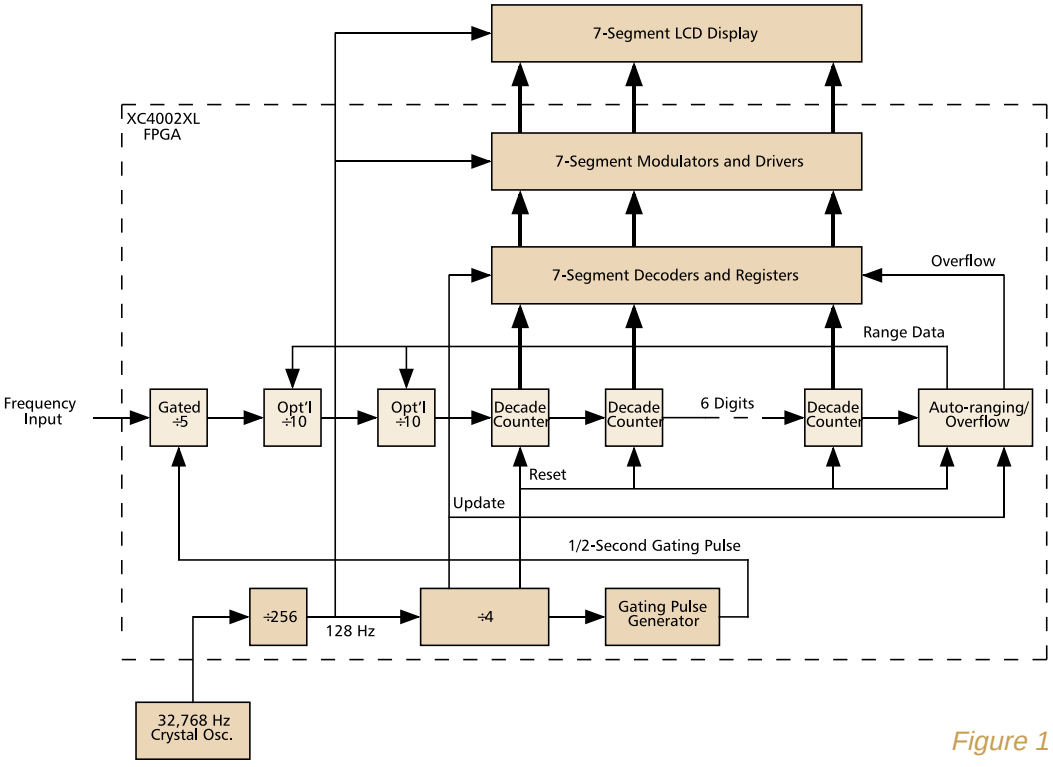

Figure 1

Continued on the following page

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400MHz Divide-by-2 Stage

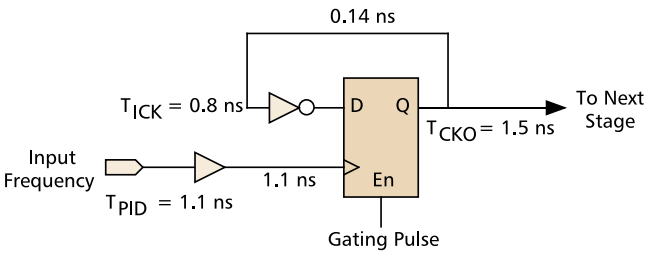

Figure 2

Consequently, the first stage is an unconditional divide-by-2, as shown in Figure 2. The clock-to-setup delay of 2.44 ns permits 400-MHz operation even under worst-case conditions. The flip-flop is located in the leftmost column of CLBs. This location gave the shortest route from the IOB, just 1.1ns.

While speed requirements necessitate simplicity around the first flip-flop, its clock-enable input can be used to effectively gate the input signal. If the first flip-flop is disabled, no subsequent clocks are generated and the whole counter chain is disabled. Thus, the effect is the same as removing the input from the counter.

Fixed Divide-by-5 Stage

The residual pre-scaler in the lowest frequency range is divide-by-5. This is in conflict with having the first stage be an unconditional divide-by-2, since five is an odd number.

The solution to this problem is shown in Figure 3. A divide-by-2/divide-by-3 counter divides with a toggle flip-flop. This flip-flop is then fed back to control the modulus of the counter, alternating it between divide-by-2 and divide-by-3. The result is that the flip-flop toggles at one-fifth of the input clock with a 2:3 mark-space ratio.

In this case, however, the output is taken directly from the counter. When combined with the first stage, this gives a division ratio that alternates between four and six. This averages to divide-by-5, but with a variable mark-space ratio. Over two periods, the mark-space ratio is 2:2:2:4. Two clock edges are produced every ten input clocks, and the division ratio is correct.

The count sequence of the divide-by-2/divide-by-2/3 counter was selected to allow the feedback signal more time to set-up. The control input is “don’t care” except at the second clock edge after the toggle-flip-flop is clocked. Thus there are two clock cycles for the feedback path to settle. With a 400-MHz input, 10 ns is available which is more than adequate.

Divide-by-5 Stage

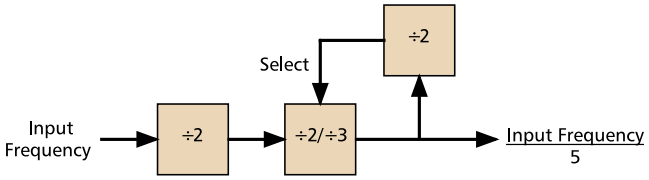

Figure 3

Optional Divide-by-10 Stages

The optional divide-by-10 pre scaler stages are both the same.

The circuit is a simple modification of the divide-by-5 described above. The only difference is that the toggle-flip-flop is replaced by a 2-bit Johnson counter. The division ratio is achieved by controlling the divide-by-2/divide-by- counter to divide successively by 2, 3, 3, and 2 within one cycle of the Johnson counter.

When a stage is not required, a multiplexer selects the input clock instead of the divided output. A simple clock multiplexer is adequate since the select control only changes when the counter is disabled.

Decade Counter

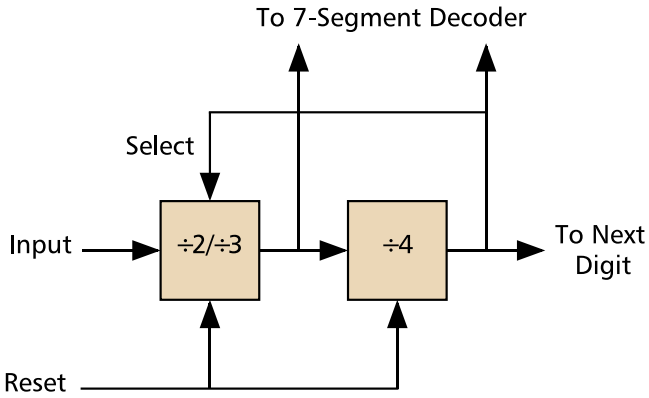

Figure 4

Decade Counter

The decade-counter design, shown in Figure 4, is based on the divide-by-10 pre-scaler. The non-binary sequence is not a problem, because LUTs are used as decoders for the 7-segment displays, and any mapping is possible. The design of the counter also provides leading-zero suppression. As shown in the state diagram in Figure 5, there are two zero states that

have different state assignments. One is a displayed-zero state, while the other is a suppressed-zero state.

When the counter is reset to the suppressed-zero state, all zeros are leading zeros. As counting progresses, however, the counter rolls over to the displayed-zero state. This cannot happen until at least one carry has been generated, and the zero can no longer be a leading zero. Whether a leading zero is actually suppressed or not can be determined in the 7-segment decoder. The suppressed-zero location in the LUT is programmed either for blank or a duplicate zero.

In this frequency counter design, only the three most significant leading zeros are suppressed. The others are displayed along with a kilohertz decimal point to indicate low input frequencies.

Decade Counter State Diagram

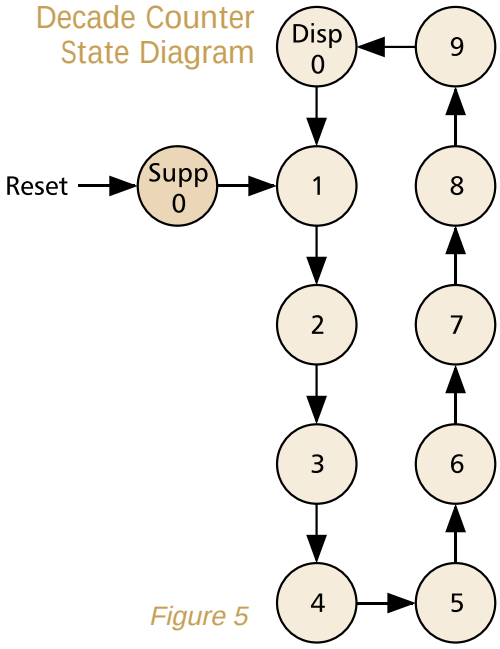

Figure 5

7-segment Decoders and Drivers

The 7-segment decoders are simple LUTs that are connected to the decade counters. During the interval between gating pulses, the LUT outputs are clocked into a register. This register, in turn, drives the display, holding it stable for one counting period.

The segment bits are modulated as they pass through their respective IOBs, thus providing AC drive to the LCD. This modulation uses a 50% duty-cycle128-Hz signal from the time-base and an XOR function that is built into the IOBs. The 128-Hz signal also drives the LCD substrate.

Time-base

The time base is derived from a crystal oscillator module. 32,768 Hz, a standard watch frequency, was chosen because the half-second gate pulse could be obtained by simple binary division.

The first four division stages are a cascade of 2-bit Johnson counters, and the resulting 128 Hz signal modulates the LCD outputs. In addition, the 128 Hz is divided in another 2-bit Johnson counter that is decoded to provide the control signals that update the display register and reset the counter.

The 32-Hz signal from the final Johnson Counter clocks a synchronous counter that outputs a 16:1 mark/space ratio. The mark is the half-second gating pulse, and the space enables the Johnson-counter decoders to create one set of update and reset pulses. Synchronous operation of this final counter was chosen to ensure a precise half-second pulse. At 32 Hz, the clock-distribution power is negligible.

Implementation

The design was entered using schematic capture. To guarantee the performance objectives, six CLBs and one IOB were hand-placed using LOC constraints in the schematic. These hand-placed resources represent less than 10% of the total FPGA. The remaining logic was mapped and placed automatically.

The ripple nature of the design did not permit clock frequencies to be specified in the design. Instead, net-delay constraints were place on a total of 9 nets. These constraints covered the input and pre-scaler stages.

80-MHz operation was required up to the input of first decade counter. This requirement was to guarantee that the counters would still operate correctly if the maximum input frequency is applied when no optional pre-scaling is selected. Otherwise, the auto-ranging circuits would receive invalid information and might fail to operate.

Results

Using a 3.6-V NiCad battery, the counter operates reliably at 420 MHz. As the input frequency varies, the supply current changes from 2 mA with no input to 40 mA at the maximum input frequency. At idle, the current draw is dominated by the time-base crystal oscillator.

The design used 56 of 64 CLBs, less than 90% of the device. Including four test-point signals, all of the available IOBs were used. Using the default settings of the implementation software, the design compiles in just four minutes.

Conclusions

The design is somewhat unconventional in the rate at which its frequency requirements reduce as one moves away from the input. However, it is not that unusual to find small regions of high frequency operation in an otherwise moderate frequency design. The frequency counter demonstrates that, with only a minor amount of manual effort devoted to the high-speed regions, the whole design can easily be implemented in an FPGA.

The semi-synchronous design style proved very effective. One non-obvious advantage is that the data and the clock are combined into a single signal. This greatly simplifies the placement and routing since there are no timing relationships to be maintained between stages. Σ