FPGA-Link System Level Integration of FPGAs

FPGA-Link from TRILOGIC is a product that extracts information from "post-route" FPGA design files and automatically creates all the necessary symbols, schematics, and hierarchical associations to integrate the FPGA into a system-level design ready for simulation.

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Once your FPGA design is complete you need to incorporate the FPGA into a system-level schematic design and manage the effect of FPGA design changes. This task may seem trivial, but it involves many tedious processes to ensure correct integration for system-level simulation and PCB design. For each FPGA in the system, a "PCB-level" symbol must be constructed and a simulation model created or integrated. When changes, such as pin reassignments, are made to the FPGA, the resulting changes must be reflected and verified on the schematic and symbol.

To effectively manage the process of design changes, FPGA-Link creates a top-level symbol, or optionally connects to an existing symbol, that links the FPGA design with the rest of the system. This allows the FPGA symbol to change without modifying the system level schematic. The connectivity between hierarchy levels is maintained and can be verified.

Xilinx Design Input Flow - Alliance or Foundation Series Software

Two output files, .pad and .dly, are output by the Xilinx Place and Route program. The .pad file includes all used pins and their locations. The .dly file is used to determine pin types. FPGA-Link reads all specified pins from the .pad file, the .dly file, and an optional configuration file, then looks in the Viewlogic IntelliFlow database to find other information about the Xilinx device, such as power and ground pins. If FPGA-Link cannot determine the pin type of any of the pins in the .pad file you will be presented with a list of those pins and asked to specify their types.

Xilinx Design Input Flow - XACT Series

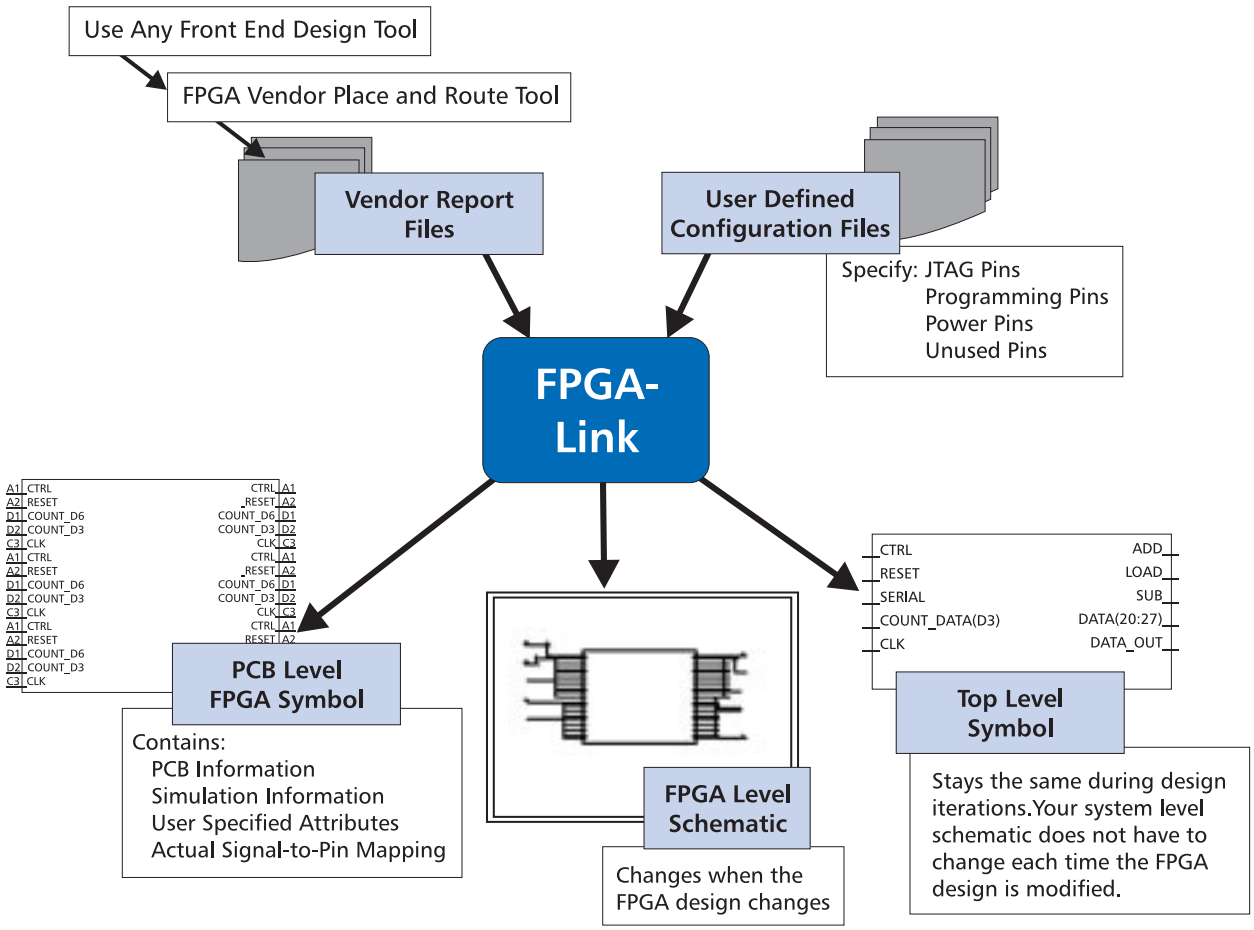
The older Xilinx XACT Place and Route tools output an .xnf file, which includes all used pins, their locations, and types. To generate this file, make sure the "Produce Timing Simulation Data" option is turned on in the Design Implementation Options dialog box. FPGA-Link reads all specified pins from the .xnf file, and from an optional user-defined configuration file, then looks in the Viewlogic IntelliFlow database to find other information about the specific Xilinx device (such as power and ground pins).

User Customizable Options

You have the ability to supply additional information to FPGA-Link for creating more intelligent design models. Some of the advanced functions include:

- Explicitly defining JTAG/programming pins, power pins, and unused or unconnected pins.
- Automatically adding capacitors for power and signal pins.
- Linking to FPGA Simulation models (Schematic, EDIF, VHDL, Verilog).
- Including specific symbol attributes such as part number, cost, description, and so on.
- Automatically creating bus pins.
- Controlling symbol object sizes such as pin length, pin spacing, label and attribute text.

FPGA-Link provides tremendous time savings to the FPGA and system design engineer. It quickly and correctly integrates FPGAs into system-level designs, and maintains design integrity during FPGA design changes.



FPGA-Link Outputs

When FPGA-Link executes, it combines the data provided from the place and route tools with the optional user configuration data, and automatically generates the following outputs:

- A symbol containing PCB attributes and simulation information.
- A schematic with the FPGA symbol on it (and optional capacitors).
- Either attributes to link to simulation models, or underlying schematics to represent the design.
- Either a new top-level symbol for use in system-level schematics, or a link to an existing top-level symbol.

For linking to simulation data, you can specify an "Underlying Model" type as EDIF, VHDL, or Verilog. If the model is set to EDIF, FPGA-Link creates underlying schematics for the design. If it is VHDL or Verilog, FPGA-Link adds the required attributes to perform simulation of the symbol.

Conclusion

FPGA-Link provides tremendous time savings to the FPGA and system design engineer. It quickly and correctly integrates FPGAs into system-level designs, and maintains design integrity during FPGA design changes. FPGA-Link operates in conjunction with Viewlogic's Workview Office design environment. FPGA-Link is priced at $1,500 and is distributed through a Value Added Reseller channel. Free 30-day evaluations can be obtained through the TRILOGIC website or by sending an email request to info@trilogic.com Σ.

For more information, contact TRILOGIC at 1-800-486-3585, info@trilogic.com or www.trilogic.com.