Plan Now for Lower Supply Voltages

The relentless pressure to achieve higher speed, higher density, lower cost, and lower power consumption is driving Xilinx (and other IC manufacturers) to use ever-thinner gate oxides and smaller geometries, resulting in a requirement for lower supply voltages.

At 0.35 microns, devices cannot reliably tolerate a 5 volt supply, and require a 3.3 volt supply instead. At 0.25 microns, the supply voltage must be lowered to 2.5 volts. At 0.18 microns, a 1.8 volt supply will be likely. To take advantage of the technical and economic benefits of these smaller process geometries, you will face several challenges:

- Distributing multiple supply voltages on the PC board.
- Interfacing between CMOS devices using different supply voltages.
- Sequencing supply voltages.

Distributing Multiple Supply Voltages on the PC Board

At today's speeds, the analog characteristics of a PC board play a strong role in determining digital system performance. Even modest-length (3 inch) interconnects must be treated as transmission lines. Pay attention to each signal path, including the complete current loop from the positive supply connection, through the IC and interconnects, through the ground distribution, through the decoupling capacitors, back to the positive supply terminal.

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Modern designs require PC boards with at least four layers (and usually more). At least one inner layer must be dedicated as a ground plane and kept as undisturbed as possible. Any major hole in the ground plane forces the ground current to take detours — increasing the inductance and causing ground voltage spikes. In simple designs, 5 volt and 3.3 volt supplies can share a common power plane.

To demonstrate the importance of good Vcc decoupling, assume that you have a 40 MHz clock and the device consumes 1 amp. Most of the current flow will be in the first 5 ns of the 25 ns clock period. This 5 amp peak current must be supplied by the sum of the decoupling capacitors. In this example, 5 amps times 5 ns causes a 250 mV drop on a 0.1 µF decoupling capacitance, creating a possible problem. Here are some recommendations:

- Decoupling capacitors must have very low inductance and series resistance. The total capacitance value is less important, as long as it exceeds 0.1 µF. The best way to achieve low impedance at gigahertz speeds is to use multiple capacitors in parallel. Use 0.01 to 0.1 µF ceramic capacitors mounted very close to each Vcc pin and directly connected to the ground plane.
- Signal lines must be kept short. A narrow, 0.25 inch (6 mm) trace represents an inductance of 20 nH. A current transient of 100 mA/ns causes a voltage drop of 2 volts across this inductance, which is unacceptable.
- Some PC boards can use an extremely thin dielectric layer between the ground and Vcc planes to achieve excellent distributed decoupling capacitance.
- Ground bounce, cross-talk, and other external noise must be minimized. Xilinx provides a slew-rate-limited output option, individually programmable for each pin, so you can slow the transition rate on all non-critical outputs.

Interfacing Between Devices with Different Supply Voltages

Because all supply voltages share a common ground, there are no problems interfacing at Low logic levels. All potential problems occur when interfacing at High logic levels. For example:

- **3.3 volt logic High driving a 5 volt input** — There is no problem when the 5 volt device has a TTL-level input threshold of approximately 1.3 volt. This is true for most CMOS devices. The driving 3.3 volt output

High level is close to Vcc, and thus well above the required Vih of 2 volts.

- **5 volt logic High driving 3.3 volt input** — In most cases, the High 5 volt output voltage will force excessive current into the 3.3 volt input. The pins on older Xilinx 3.3 volt FPGAs, and on most other manufacturers' 3.3 volt devices have a clamp diode between each pin and Vcc to protect the circuit against electrostatic discharge (ESD). This diode starts conducting when the pin is driven more than 0.7 volts positive with respect to its Vcc. This diode presents a problem in mixed-voltage systems, because it clamps whenever a 5 volt logic High is connected to a 3.3 volt input.

  Xilinx has overcome this problem by eliminating the clamp diode between the pin and Vcc in the circuit structure of the Xilinx XC4000XL family. The pin can thus be driven as high as 5.5 volts without regard to the actual supply voltage on the receiving input. Therefore, these devices are unconditionally 5 volt tolerant, and you can ignore all interface precautions. Excellent
  ESD protection (several thousand volts) is achieved by means of a patented diode-transistor structure that does not connect to Vcc. Directly connecting an active High 5 volt CMOS output to an active High 3.3 volt output creates contention and must be avoided.

  When 3.3 volt inputs are being driven from a TTL-level output using an n-channel pull-up transistor — available as an option on all XC4000 and XC4000E and XC4000EX devices — the input current is naturally limited to less than a few mA, even when the 5 volt supply is at 5.25 volts while the 3.3 volt supply is at 3.0 volts; a very unlikely combination. At nominal supply voltage levels, the current is approximately 1 mA.

  When non-5-volt-tolerant inputs are driven from a CMOS-level, complementary, rail-to-rail output, you must somehow limit the current. A 1 Kohm resistor limits the current to less than 2 mA, but causes a slight speed penalty (1 Kohm x 35 pF = 35 ns)

- **3.3 volt logic High driving a "CMOS threshold" 5 volt input** — This interface situation should be avoided. An active High 3.3 volt output cannot be pulled higher, because the internal pull-up transistor represents an impedance of approximately 50 ohms for any current in either direction. A pull-up resistor to 5 volts is therefore useless. If the internal pull-up transistor is disabled (open drain output) the pin can be pulled higher, until the ESD clamp becomes conductive. The pins on the Xilinx XC4000X family can thus be configured as open drain, and an external resistor can pull them all the way to 5 volts (with a resulting RC speed penalty).

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Sequencing Supply Voltages

Any system with more than one supply voltage faces the possibility of these voltages being applied in an undefined or uncontrolled sequence. For most ICs, this means you must calculate the maximum current flowing into the pins of the non-powered device. The current value depends on the powered-up device's output structure (complementary outputs drive the highest current) and on the voltage compliance (impedance) of the non-powered Vcc distribution net. If it is held rigidly to ground, the undesired current will be high. If the non-powered Vcc can easily be pulled High, the current will be far less. Most inputs will tolerate 50 mA for a few seconds, and 10 mA for unlimited time. For significantly higher currents there might be the short-term risk of latch-up, and the long-term risk of metal migration if the high current persists for thousands of hours.

The Xilinx XC4000XL family is 5 volt tolerant, even when their Vcc is zero. Therefore, these devices have no problem with arbitrary power sequencing or even with "hot plug-in". When 5 volt power is applied first, there is no current into the Xilinx FPGAs. When 3.3 volt power is applied first, the device outputs can be kept in a 3-state condition by connecting the 5 volt Vcc line as an active-Low Global 3-state input to the

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3.3 volt devices, again eliminating any undesirable current.

Converting to Lower Voltage Designs

Xilinx 3.3 volt FPGAs are fully compatible with their 5 volt equivalents. You can start a design using 5 volt supplies, later plugging in the 3.3 volt devices with no concern for functionality, speed, pin locations, or logic levels.

The next transition — to 2.5 volts — will arrive within a year. This change will be less of a challenge because Xilinx will, at first, use 2.5 volts only for the internal logic, while running the I/O with 3.3 volt power. You must provide the additional Vcc, but you need not be concerned about signal level incompatibilities. However, we will increase the number of Vcc and ground pins.

To ease these transitions, the IC industry plans to accommodate direct interfacing between three successive generations: first between 5, 3.3, and 2.5 volt devices, and then in 1999, 3.3, 2.5, and 1.8 volt devices.

Conclusion

New improvements in IC technology enable a wealth of new, smaller systems with higher performance and lower power requirements. To take advantage of these improvements, designers must provide new supply voltages — 3.3 volts now and 2.5 volts in the near future.

In many cases, these new, lower-voltage devices will be used side-by-side with older, 5 volt parts. These mixed-voltage environments could create a variety of design challenges, especially when using FPGAs that are not specifically designed to operate in mixed-voltage environments. The new 3.3 volt Xilinx FPGA families are immune to all power sequencing problems and can be interfaced directly with 5 volt devices, making them an ideal solution for many mixed-voltage systems. ◆

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