Xilinx CORE Generator

System

Compatibility Guide

September 1999

Table of Contents

Overview

This manual is a collection of compatibility guides of various Xilinx DSP cores.

Each compatibility guide shows in some detail how a core changes or stays the same when supported in various Xillinx core generation tools, namely, the **LogiBlox** , the **CORE Generator System V1.5** , and the **CORE Generator System V2.1** .

The purpose of this guide is to help our customers quickly identify key features when switching to a different version of our core generation tool. For easy navigation, we have presented the information in tables.

Manual Contents

The compatibility guides in this manual describe the following features of the specific core:

- **Name**
- **Functionality**
- **Port name**
- **Parameters**

Compatibility Guide: Data Register

Latch Based Register

Table 1: Functionality Comparison

CORE Generator System V2.1 vs. LogiBlox	CORE Generator System V2.1 vs. CORE Generator System V1.5
• CORE Generator System V2.1 Latch Based Register Core is functionally similar to LogiBlox Latch core.	• N/A

Table 2: Core Name Cross Reference

Tool	Core Name	Location in the Tree
LogiBlox	Data Register Style = Latches	Data Registers
CORE Generator System V1.5	N/A	N/A
CORE Generator System V2.1	LD-based Register	Basic Elements -> Registers, Shifters & Pipelining

Table 3: Port Name Cross Reference

LogiBlox	CORE Generator System V1.5	CORE Generator System V2.1 or later	Direction	Description
D_IN[N:0]	N/A	D[N:0]	Input	Data Input
Q_OUT[N:0]	N/A	Q[N:0]	Output	Data Output
GATE	N/A	G	Input	Gate
GATE_EN	N/A	GE	Input	Gate Enable
N/A	N/A	ASET	Input	Asynchronous Set to All 1's
N/A	N/A	ACLR	Input	Asynchronous Clear to All 0's
ASYNC_CTRL	N/A	AINIT	Input	Asynchronous Initialize
N/A	N/A	SSET	Input	Synchronous Set toAll 1's
N/A	N/A	SCLR	Input	Synchronous Clear to All 0's
SYNC_CTRL	N/A	SINIT	Input	Synchronous Initialize

Notes:

1. In LogiBlox, ASYNC_CTRL loads the value assigned to the ASYNC_VAL attribute and in CORE Generator System V2.1, AINIT loads the value assigned to the AINIT_VAL attribute.
2. In LogiBlox, SYNC_CTRL loads the value assigned to the SYNC_VAL attribute and in CORE Generator System V2.1, SINIT loads the value assigned to the SINIT_VAL attribute.

Table 4: Parameter Names Cross Reference

LogiBlox (.mod)	COREGenerator V1.5 (.log)	COREGenerator V2.1 or later (.xco)	Type	COREGenerator V2.1 Default setting
module DATA_REG STYLE = CLB_LD	N/A	SELECT LD_Latch		
Symbol	N/A	component_name	String	blank
BUS_WIDTH	N/A	data_width	Integer	16
N/A	N/A	gate_enable	Keyword	false
N/A	N/A	ge_overrides	Keyword	sync_controls_override_ge
N/A	N/A	asynchronous_settings	Keyword	none
ASYNC_VAL	N/A	async_init_value	Hex	0
N/A	N/A	synchronous_settings	Keyword	none
SYNC_VAL	N/A	sync_init_value	Hex	0
N/A	N/A	set_clear_priority	Keyword	clear_overrides_set
USE_RPM	N/A	create_rpm	Keyword	true

Notes:

3. Check the respective datasheet for syntax, definition, and default value of each keyword.

Compatibility Guide: Data Register

FD Register

Table 5: Functionality Comparison

CORE Generator System V2.1 vs. LogiBlox	CORE Generator System V2.1 vs. CORE Generator System V1.5
• Similar functionality	• CORE Generator System V2.1 supports up to 64 bit data width as opposed to 32 in CORE Generator System V1.5 • CORE Generator System V2.1 supports an optional Clock Enable input as opposed to providing it by default • CORE Generator System V2.1 supports optional Asynchronous Set, Clear and Init as opposed to supporting only Asynchronous Reset in V1.5 • CORE Generator System V2.1 supports Synchronous Set, Clear and Init which was not available in CORE Generator System V1.5

Table 6: Core Name Cross Reference

Tool	Core Name	Location in the Tree
LogiBlox	Data Register Style = D-Type	Data Registers
COREGenerator System V1.5	Register	LogiCORE-> Basic Elements
COREGenerator System V2.1	FD Register	Basic Elements -> Registers, Shifters & Pipelining

Table 7: Port Name Cross Reference

LogiBlox	COREGenerator System V1.5	COREGenerator System V2.1 or later	Direction	Description
D_IN[N:0]	D[N:0]	D[N:0]	Input	Data Input
Q_OUT[N:0]	Q[N:0]	Q[N:0]	Output	Data Output
CLOCK	C	CLK	Input	Clock
CLK_EN	CE	CE	Input	Clock Enable
N/A	N/A	ASET	Input	Asynchronous Set toAll 1’s
N/A	CLR	ACLR	Input	Asynchronous Clear to All 0’s
ASYNC_CTRL	N/A	AINIT	Input	Asynchronous Initialize
N/A	N/A	SSET	Input	Synchronous Set to All 1’s
N/A	N/A	SCLR	Input	Synchronous Clear to All 0’s
SYNC_CTRL	N/A	SINIT	Input	Synchronous Initialize

Notes:

4. In LogiBlox, ASYNC_CTRL loads the value assigned to the ASYNC_VAL attribute and in CORE Generator System V2.1, AINIT loads the value assigned to the AINIT_VAL attribute.
5. In LogiBlox, SYNC_CTRL loads the value assigned to the SYNC_VAL attribute and in CORE Generator System V2.1, SINIT loads the value assigned to the SINIT_VAL attribute.

Table 8: Parameter Names Cross Reference

LogiBlox (.mod)	COREGenerator V1.5 (.log)	COREGenerator V2.1 or later (.xco)	Type	COREGenerator V2.1 Default setting
Symbol	component_Name	component_name	String	blank
BUS_WIDTH	port_width	data_width	Integer	16
N/A	N/A	clock_enable	Keyword	false
N/A	N/A	ce_overrides	Keyword	sync_controls_override_ce
N/A	N/A	asynchronous_settings	Keyword	none
ASYNC_VAL	N/A	async_init_value	Hex	0
N/A	N/A	synchronous_settings	Keyword	none
SYNC_VAL	N/A	sync_init_value	Hex	0
N/A	N/A	set_clear_priority	Keyword	clear_overrides_set
USE_RPM	N/A	create_rpm	Keyword	true

Notes:

6. Check the respective datasheet for syntax, definition, and default value of each keyword.
7. To generate a module which is equivalent in functionality to the CORE Generator System V1.5, **clock_enable** should be set to **true** and **asynchronous_settings** should be set to **clear**. All other parameters labeled as "N/A" should be set to their respective default values.

Compatibility Guide: Gate

Single Output Gate

Table 9: Functionality Comparison

CORE Generator V2.1 vs. LogiBlox	CORE Generator System V2.1 vs. CORE Generator System V1.5
• CORE Generator System V2.1 supports one type of implementation, Normal Gates, whereas LogiBlox supports five styles: Edge Decode, Maximum Speed, Minimum Area, Normal Gates, and Wired AND. • CORE Generator System V2.1 has a selectable registered or non-registered output as opposed to combinatorial only in LogiBlox.	• N/A

Table 10: Core Name Cross Reference

Tool	Core Name	Location in the Tree
LogiBlox	Simple Gates	Simple Gates
COREGenerator System V1.5	N/A	N/A
COREGenerator System V2.1	Bit Gate	Basic Elements -> Logic Gates & Buffers

Table 11: Port Name Cross Reference

LogiBlox	COREGenerator V1.5	COREGenerator V2.1 or later	Direction	Description
A[N:0]	N/A	I[N:0]	IN	Gate Input
O	N/A	O	OUT	non-registered output
N/A	N/A	Q[0:0]	OUT	registered output
N/A	N/A	CLK	IN	Clock
N/A	N/A	CE	IN	Clock Enable
N/A	N/A	ASET	IN	Asynchronous Set to All 1’s
N/A	N/A	ACLR	IN	Asynchronous Clear to All 0’s
N/A	N/A	SSET	IN	Synchronous Set to All 1’s
N/A	N/A	SCLR	IN	Synchronous Clear to All 0’s

Table 12: Parameter Names Cross Reference

LogiBlox (.mod)	CORE Generator System V1.5 (.log)	CORE Generator System V2.1 or later (.xco)	Type	CORE Generator System V2.1 Default Setting
OPTYPE=TYPE_1 STYLE = NORMAL_GATES	N/A	SELECT Bit_Gate		
symbol	N/A	component_name	String	blank
BUS_WIDTH	N/A	number_of_inputs	Integer	2
module(3)	N/A	gate_type(4)	Keyword	and
INVMASK	N/A	input_inversion_mask	Hex	0
DECODEMASK	N/A	N/A	N/A	N/A
N/A	N/A	output_options	Keyword	registered
N/A	N/A	clock_enable	Keyword	false
N/A	N/A	ce_overrides	Keyword	sync_controls_override_ce
N/A	N/A	asynchronous_settings	Keyword	none
N/A	N/A	power_on_reset_value	0 or 1	0
N/A	N/A	synchronous_settings	Keyword	none
N/A	N/A	set_clear_priority	Keyword	clear_overrides_set
N/A	N/A	create_rpm	Keyword	false

Notes:

8. Check the respective datasheet for syntax, definition, and default value of each keyword.
9. INVMASK and DECODEMASK attributes use opposite polarities to achieve the same effect.
10. The different modules supported are: AND, NAND, OR, NOR, XOR, XNOR, INVERT.
11. The different gate_type supported are: and, nand, or, nor, xor, xnor. INVERTER and BUFFER are supported under the Bus Gate Core.

Compatibility Guide: Gate

Bus Gate

Table 13: Functionality Comparison

CORE Generator V2.1 vs. LogiBlox	CORE Generator V2.1 vs. CORE Generator V1.5
• CORE Generator System V2.1 supports one type of implementation, Normal Gates, whereas LogiBlox supports three styles: Maximum Speed, Minimum Area and Normal Gates. • CORE Generator System V2.1 has a selectable registered or non-registered output as opposed to combinatorial only in the LogiBlox. • CORE Generator System V2.1 supports a maximum of 4 input buses as opposed to 8 input buses in LogiBlox.	• N/A

Table 14: Core Name Cross Reference

Tool	Core Name	Location in the Tree
LogiBlox	Simple Gates	Simple Gates
COREGenerator System V1.5	N/A	N/A
COREGenerator System V2.1	Bus Gate	Basic Elements -> Logic Gates & Buffers

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Table 15: Port Name Cross Reference

LogiBlox	COREGenerator V1.5	COREGenerator V2.1 or later	Direction	Description
A[N:0].. B[N:0]	N/A	IA[N:0].. ID[N:0]	Input	Input Buses
O[N:0]	N/A	O[N:0]	Output	Output for non-registered gate
N/A	N/A	Q[N:0]	Output	Output for registered gate
N/A	N/A	CLK	Input	Clock
N/A	N/A	CE	Input	Clock Enable
N/A	N/A	ASET	Input	Asynchronous Set to All 1’s
N/A	N/A	ACLR	Input	Asynchronous Clear to All 0’s
N/A	N/A	AINIT	Input	Asynchronous Initialize
N/A	N/A	SSET	Input	Synchronous Set to All 1’s
N/A	N/A	SCLR	Input	Synchronous Clear to All 0’s
N/A	N/A	SINIT	Input	Synchronous Initialize

Table 16: Parameter Names Cross Reference

LogiBlox (.mod)	CORE Generator System V1.5 (.log)	CORE Generator System V2.1 or later (.xco)	Type	CORE Generator System V2.1 Default setting
OPTYPE=TYPE_3 STYLE = NORMAL_GATES	N/A	SELECT Bus_Gate		
symbol	N/A	component_name	String	blank
INPUT_BUSSES	N/A	number_of_input_buses	1 to 4	2
BUS_WIDTH	N/A	input_bus_width	Integer	16
module(3)	N/A	gate_type(4)	Keyword	and
N/A	N/A	input_a_inversion_mask	Hex	0
N/A	N/A	input_b_inversion_mask	Hex	0
N/A	N/A	input_c_inversion_mask	Hex	0
N/A	N/A	input_d_inversion_mask	Hex	0
N/A	N/A	output_options	Keyword	registered
N/A	N/A	clock_enable	Keyword	false
N/A	N/A	ce_overrides	Keyword	sync_controls_override_ce
N/A	N/A	asynchronous_settings	Keyword	none
N/A	N/A	async_init_value	Hex	0
N/A	N/A	synchronous_settings	Keyword	none
N/A	N/A	sync_init_value	Hex	0
N/A	N/A	set_clear_priority	Keyword	clear_overrides_set
N/A	N/A	create_rpm	Keyword	true

Notes:

12. Check respective the datasheet for syntax, definition, and default values of each keyword.
13. The different modules supported are: AND, NAND, OR, NOR, XOR, XNOR, INVERT.
14. The different gate_type supported are: and, nand, or, nor, xor, xnor, inverter and buffer. The number of input busses supported for the Inverter and the Buffer is 1.

Compatibility Guide: Gate

Bus Gated with Control

Table 17: Functionality Comparison

CORE Generator System V2.1 vs. LogiBlox	CORE Generator System V2.1 vs. CORE Generator System V1.5
• CORE Generator System V2.1 supports one type of implementation, Normal Gates, whereas LogiBlox supports three types of implementation: Maximum Speed, Minimum Area, and Normal Gates. • CORE Generator System V2.1 has a selectable registered or non-registered output as opposed to combinatorial only in the LogiBlox.	• N/A

Table 18: Core Name Cross Reference

Tool	Core Name	Location in the Tree
LogiBlox	Simple Gates	Simple Gates
COREGenerator System V1.5	N/A	N/A
COREGenerator System V2.1	Bit Bus Gate	Basic Elements -> Logic Gates & Buffers

Table 19: Port Name Cross Reference

LogiBlox	COREGenerator V1.5	COREGenerator V2.1 or later	Direction	Description
B[N:0]	N/A	I[N:0]	Input	Input Bus
A	N/A	CTRL	Input	Control bit
O[N:0]	N/A	O[N:0]	Output	Output for non-registered gate
N/A	N/A	Q[N:0]	Output	Output for registered gate
N/A	N/A	CLK	Input	Clock
N/A	N/A	CE	Input	Clock Enable
N/A	N/A	ASET	Input	Asynchronous Set to All 1’s
N/A	N/A	ACLR	Input	Asynchronous Clear to All 0’s
N/A	N/A	SSET	Input	Synchronous Set to All 1’s
N/A	N/A	SCLR	Input	Synchronous Clear to All 0’s

Table 20: Parameter Names Cross Reference

LogiBlox (.mod)	CORE Generator System V1.5 (.log)	CORE Generator System V2.1 or later (.xco)	Type	CORE Generator System V2.1 Default Setting
OPTYPE = TYPE_2 SYTLE = NORMAL_GATES	N/A	SELECT Bit_Bus_Gate		
symbol	N/A	component_name	String	blank
BUS_WIDTH	N/A	input_bus_width	Integer	16
module	N/A	gate_type	Keyword	and
INVMASK	N/A	input_inversion_mask	Hex	0
DECODEMASK	N/A	N/A	N/A	N/A
N/A	N/A	output_options	Keyword	registered
N/A	N/A	clock_enable	Keyword	false
N/A	N/A	ce_overrides	Keyword	sync_controls_override_ce
N/A	N/A	asynchronous_settings	Keyword	none
N/A	N/A	async_init_value	Hex	0
N/A	N/A	synchronous_settings	Keyword	none
N/A	N/A	sync_init_value	Hex	0
N/A	N/A	set_clear_priority	Keyword	clear_overrides_set
N/A	N/A	create_rpm	Keyword	true

Notes:

15. Check the respective datasheet for syntax, definition, and default value of each keyword.
16. INVMASK and DECODEMASK attributes use opposite polarities to achieve the same effect.
17. The different modules supported are: AND, NAND, OR, NOR, XOR, XNOR, INVERT.
18. The different gate_type supported are: and, nand, or, nor, xor, xnor. INVERTER and BUFFER are supported under the Bus Gate Core.

Compatibility Guide: Multiplexers

Bit Multiplexer

Table 21: Functionality Difference

CORE Generator V2.1 vs. LogiBlox	CORE Generator V2.1 vs. CORE Generator V1.5
• CORE Generator System V2.1 supports one type of implementation, Normal Gates, whereas LogiBlox supports four types of implementation: Maximum Speed, Minimum Area, Normal Gates, and Wired AND. • CORE Generator System V2.1 Multiplexer Select input is always Binary encoded as opposed to the two Encoding styles supported in LogiBlox (One Hot, Binary). • CORE Generator System V2.1 has a selectable registered or non-registered output as opposed to a combinatorial output only for the LogiBlox Multiplexer.	• N/A

Table 22: Core Name Cross Reference

Tool	Core Name	Location in the Tree
LogiBlox	Multiplexers	Multiplexers
COREGenerator System V1.5	N/A	N/A
COREGenerator System V2.1	Bit Multiplexer	Basic Elements -> Multiplexer

Table 23: Port Name Cross Reference

LogiBlox	COREGenerator V1.5	COREGenerator V2.1 or later	Direction	Description
M[N:0]	N/A	M0.. M_{n-1}	Input	Multiplexer Inputs
O	N/A	O	Output	Output for non-registered Mux
N/A	N/A	Q[0:0]	Output	Output for registered Mux
S[M:0]	N/A	S[M:0]	Input	Binary encoded select inputs
N/A	N/A	CLK	Input	Clock
N/A	N/A	CE	Input	Clock Enable
N/A	N/A	ASET	Input	Asynchronous Set to All 1’s
N/A	N/A	ACLR	Input	Asynchronous Clear to All 0’s
N/A	N/A	SSET	Input	Synchronous Set to All 1’s
N/A	N/A	SCLR	Input	Synchronous Clear to All 0’s

Table 24: Parameter Names Cross Reference

LogiBlox (.mod)	CORE Generator V1.5 (.log)	CORE Generator V2.1 or later (.xco)	Type	CORE Generator V2.1 Default setting
module MUX OPTYPE=TYPE_1 STYLE=NORMAL_GATES	N/A	SELECT Bit_Multiplexer		
symbol	N/A	component_name	String	blank
BUS_WIDTH	N/A	number_of_inputs	Integer	2
N/A	N/A	output_options	Keyword	registered
N/A	N/A	clock_enable	Keyword	false
N/A	N/A	ce_overrides	Keyword	sync_controls_override_ce
N/A	N/A	asynchronous_settings	Keyword	none
N/A	N/A	power_on_reset_value	0 or 1	0
N/A	N/A	synchronous_settings	Keyword	none
N/A	N/A	set_clear_priority	Keyword	clear_overrides_set
N/A	N/A	create_rpm	Keyword	false

Notes:

19. Check the respective datasheet for syntax, definition, and default value ofeach keyword.

Compatibility Guide: Multiplexer

Bus Multiplexer

Table 25: Functionality Comparison

CORE Generator V2.1 vs LogiBlox	CORE Generator V2.1 vs CORE Generator V1.5
• CORE Generator System V2.1 supports two types of implementation, BUFT-based and LUT- based, whereas LogiBlox supports Maximum Speed, Minimum Area, Normal Gates and Wired AND. LUT-based is equivalent to Normal Gates and BUFT-based is equivalent to Wired AND. • CORE Generator System V2.1 Multiplexer Select input is always Binary encoded as opposed to the two Encoding styles supported in LogiBlox (One Hot, Binary). • CORE Generator System V2.1 has a selectable registered or non-registered output as opposed to combinatorial only in the LogiBlox Multiplexer output.	• CORE Generator System V2.1 supports two types of implementation, BUFT-based and LUT-based, whereas CORE Generator System V1.5 supports only Normal Gates (Equivalent to LUT). • CORE Generator System V2.1 has a selectable registered or non-registered output as opposed to combinatorial only in CORE Generator System V1.5.

Table 26: Core Name Cross Reference

Xilinx Tool	Core Name	Core Location in the Tree
LogiBlox	Multiplexers	Multiplexers
CORE Generator System V1.5	2-1 Multiplexer, 3-1 Multiplexer, 4-1 Multiplexer	LogiCORE-> Basic Elements-> Multiplexers
CORE Generator System V2.1	Bus Multiplexer	Basic Elements -> Multiplexer

Table 27: Port Name Cross Reference

LogiBlox	COREGenerator V1.5	COREGenerator V2.1 or later	Direction	Description
MA[N:0].. MH[N:0]	D0[N:0] .. D3[N:0]	MA[N:0].. MH[N:0]	Input	Multiplexer input buses
O[N:0]	O[N:0]	O[N:0]	Output	Output for non-registered gate
N/A	N/A	Q[N:0]	Output	Output for registered gate
S[M:0]	S0, S1	S[M:0]	Input	Binary encoded select inputs
N/A	N/A	EN	Input	Output Enable (BUFT based)
N/A	N/A	CLK	Input	Clock
N/A	N/A	CE	Input	Clock Enable
N/A	N/A	ASET	Input	Asynchronous Set toAll 1’s
N/A	N/A	ACLR	Input	Asynchronous Clear toAll 0’s
N/A	N/A	AINIT	Input	Asynchronous Initialize
N/A	N/A	SSET	Input	Synchronous Set toAll 1’s
N/A	N/A	SCLR	Input	Synchronous Clear toAll 0’s
N/A	N/A	SINIT	Input	Synchronous Initialize

Table 28: Parameter Names Cross Reference

LogiBlox (.mod)	COREGenerator V1.5 (.log)	COREGenerator V2.1 or later (.xco)	Type	COREGenerator V2.1 Default setting
module MUX OPTYPE=TYPE_2	2-1, 3-1, 4-1 Multiplexer	SELECT Bus_Multiplexer		
symbol	Component_Name	component_name	String	blank
INPUT_BUSSES		number_of_input_buses	1 to 8	2
BUS_WIDTH	Port_Width	input_bus_width	Integer	16
STYLE = GATES		multiplexer_construction	Keyword	lut_based
		output_options	Keyword	registered
		output_enable	Keyword	false
		clock_enable	Keyword	false
		ce_overrides	Keyword	sync_controls_override_ce
		asynchronous_settings	Keyword	none
		async_init_value	Hex	0
		synchronous_settings	Keyword	none
		sync_init_value	Hex	0
		set_clear_priority	Keyword	clear_overrides_set
	Create_RPM	create_rpm	Keyword	true

Notes:
20. Check the respective datasheet for syntax, definition, and default value of each keyword.
21. STYLE = WIRED is equivalent to multiplexer-construction = buft-based.

Compatibility Guide: Multiplier

Dynamic Constant Coefficient Multiplier

Table 29: Funtionality Comparison

CORE Generator V2.1 vs LogiBlox	CORE Generator V2.1 vs CORE Generator V1.5
• N/A	• CORE Generator System V2.1 Dynamic Constant Coefficient Multiplier is a subset of the CORE Generator System V1.5 Constant Coefficient Multiplier. • CORE Generator System V2.1 supports reloadable constants as opposed to a fixed constant in CORE Generator System V1.5. • CORE Generator System V2.1 provides a selectable sign pin for the input data as opposed to a pre-defined signed or unsigned input in CORE Generator System V1.5.

Table 30: Core Name Cross Reference

Tool	Core Name	Location in the Tree
LogiBlox	N/A	N/A
COREGenerator System V1.5	Pipelined/Non-pipelined Constant Coefficient Multiplier	LogiCORE-> Math -> Multipliers -> Constant Coefficient Multipliers
COREGenerator System V2.1	Dynamic Constant Coefficient Multiplier	Math Functions -> Multipliers -> Constant Coefficient

Table 31: Port Name Cross Reference

LogiBlox	COREGenerator V1.5	COREGenerator V2.1 or later	Direction	Description
N/A	A[N:0]	DATAA[N:0]	Input	Parallel Data Input
N/A	N/A	SIGNEDA	Input	Dataa sign/unsigned status
N/A	N/A	DATAB[M:0]	Input	Constant Data Input
N/A	N/A	LOADB	Input	Reload internal coefficients with Datab
N/A	N/A	CE	Input	Clock Enable
N/A	C	C	Input	Clock for pipelined version only
N/A	PROD[M+N+1:0]	PROD[M+N+1:0]	Output	Parallel Data Output
N/A	N/A	BUSY	Output	High during reloadable time

Table 32: Parameter Names Cross Reference

LogiBlox (.mod)	COREGenerator V1.5 (.log)	COREGenerator V2.1 or later (.xco)	Type	COREGenerator V2.1 Default setting
N/A	Non-pipelined Constant Coefficient Multiplier or Pipelined Constant Coefficient Multiplier	SELECT Dynamic_Constant_Coefficient_Multiplier		
NA/	Component_Name	component_name	String	blank
N/A	A_Width	variable_a_bit_width	Integer	8
N/A	Signed_Input_Data	N/A	Boolean	true
N/A	Coef_Width	constant_coefficient_bit_width	Integer	8
N/A	Coefficient	constant_coefficient	Integer	0
N/A	Signed_Coefficient	constant_coefficient_sign	Boolean	false
N/A	N/A	hex_coefficient	Boolean	true
N/A	N/A	pipeline	Boolean	true
N/A	N/A	clock_enable	Boolean	true

Notes:

22. Check the respective datasheet for syntax, definition, and default value ofeach keyword.
23. COREGenerator V1.5 coefficient values are always defined as integer in the .log file
24. The pipeline parameter is not supported in COREGenerator V1.5 but instead two seperate cores are available: non-pipelined Constant Coefficient Multiplier and Pipelined Constant Coefficient Multiplier.

Compatibility Guide: Multipliers

Variable Parallel Multiplier

Table 33: Functionality Comparison

CORE Generator V2.1 vs. LogiBlox	CORE Generator V2.1 vs. CORE Generator V1.5
• N/A	• CORE Generator System V2.1 supports one type of implementation, whereas CORE Generator System V1.5 supports two types of implementation: Area Optimized and Speed Optimized. The unique implementation used in CORE Generator System V2.1 Parallel Multiplier satisfies both area and speed requirements. • CORE Generator System V2.1 Multiplier core does not have registered inputs which results in one less clock latency than that in the CORE Generator System V1.5. • CORE Generator System V2.1 supports combinatorial architecture or pipelined with or without output register whereas CORE Generator System V1.5 supports only fully pipelined multipliers. • CORE Generator System V2.1 supports optional Clock Enable, Asynchronous Clear/Set and Synchronous Clear/Set whereas CORE Generator System V1.5 always provides Clock and Clock Enable input.

Table 34: Core Name Cross Reference

Tool	Core Name	Location in the Tree
LogiBlox	N/A	N/A
COREGenerator System V1.5	Parallel multiplier: Area optimized	Logicore -> Math -> Multipliers
COREGenerator System V2.1	Variable Parallel Multiplier	Math Function -> Multipliers -> Parallel Multiplier

Table 35: Port Name Cross Reference

LogiBlox	COREGenerator V1.5	COREGenerator V2.1 or later	Direction	Description
N/A	A[N:0]	A[N:0]	Input	A Input
N/A	B[M:0]	B[M:0]	Input	B Input
N/A	P[M+N+1:0]	P[M+N+1:0]	Output	Output Data (Product)
N/A	C	CLK	Input	Clock
N/A	CE	CE	Input	Clock Enable
N/A	N/A	ASET	Input	Asynchronous Set to All 1’s
N/A	N/A	ACLR	Input	Asynchronous Clear to All 0’s
N/A	N/A	SSET	Input	Synchronous Set to All 1’s
N/A	N/A	SCLR	Input	Synchronous Clear to All 0’s

Table 36: Parameter Names Cross Reference

LogiBlox (.mod)	CORE Generator V1.5 (.log)	CORE Generator V2.1 or later (.xco)	Type	CORE Generator V2.1 Default setting
N/A	Component_Name	component_name	String	blank
N/A	A_Width	a_width	Integer	4
N/A	B_Width	b_width	Integer	4
N/A	N/A	pipelined_registers	Keyword	registered
N/A	N/A	output_registers	Keyword	registered
N/A	Signed	signed_type	Keyword	signed
N/A	N/A	clock_enable	Keyword	false
N/A	N/A	ce_overrides	Keyword	sync_controls_override_ce
N/A	N/A	asynchronous_settings	Keyword	none
N/A	N/A	synchronous_settings	Keyword	none
N/A	N/A	set_clear_priority	Keyword	clear_overrides_set

Notes:

25. Check the respective datasheet for syntax, definition, and default value of each keyword.