One Dimensional Parallel ROM-Based Correlator

Product Specification

XILINX®

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Features

- Data word size selectable from 4 to 128 bits
- Mask parameter allows data bits to be selectively ignored
- Cascadable to form correlator of any word-size
- Easily extendible to 2 dimensions
- High performance implementation using efficient look-up table design
- Uses Fast Carry logic for high speed
- Drop-in modules for the XC4000E, EX, XL, XV, and Spartan families

- Density and performance guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx Core Generator Tool

Functional Description

This module samples the N data-bits presented on its data-input port (DIN[n:0]) on every rising edge that occurs on the clock input (C). The width of the data-input port, N, is a user selectable parameter (WIDTH) that may vary between 4 and 128 bits, in multiples of 4 bits.

The module takes two additional user parameters, MATCH and MASK, each of which are expressed as N-bit binary values. The correlator's SUM output reflects the number of bits in the most recent data-word that match the bit pattern expressed by the MATCH parameter. For example, assuming a data-word size of 12-bits, if all 12 bits of data match the 12-bit MATCH parameter, the correlator's output returns the value 12. If any of the bits in the module's memory do not match their equivalent bits in the MATCH parameter, the output value is correspondingly smaller.
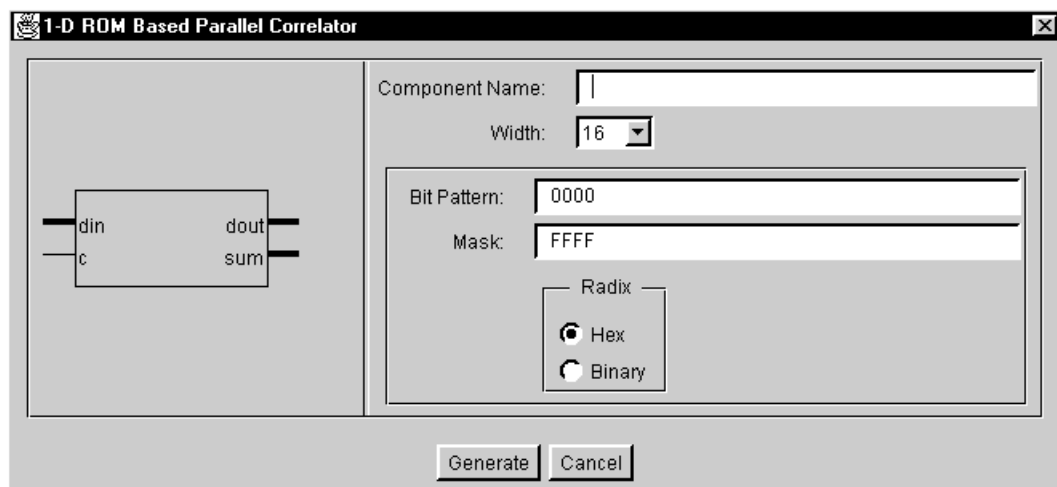

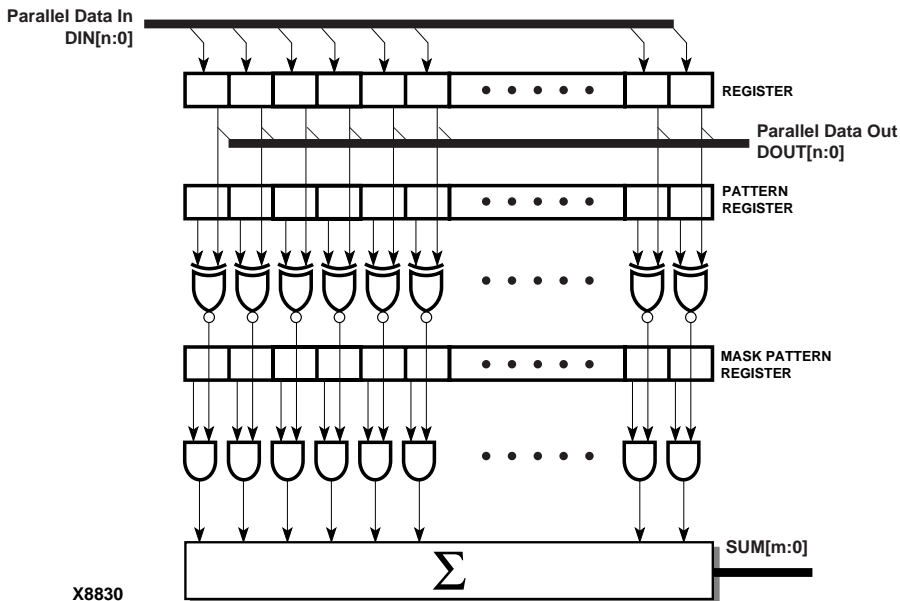**Figure 1: Parameterization Window**

Parallel Data In
DIN[n:0]

REGISTER

Parallel Data Out
DOUT[n:0]

PATTERN
REGISTER

MASK PATTERN
REGISTER

Σ

SUM[m:0]

X8830

Figure 2: Parallel Correlator Functional Block Diagram

Parallel Data In (4 to 128 bits) DIN [n:0] · · ·

Register

Flip Flop
Output
Available
DOUT [n:0]

LUT
4 word by 3 bit

LUT

· · ·

LUT

Correlation
Pattern in ROM

Latch

Adder

· · · **Registered Adder Tree**

Latch

Output
SUM [m:0]

 # Match Bits

· · ·

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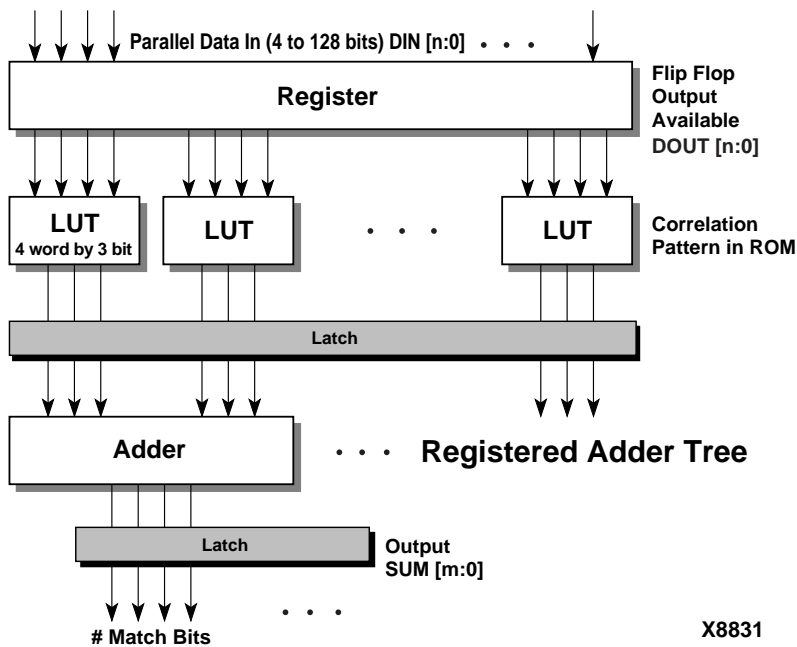
Figure 3: Core Generator Implementation of Parallel Correlator

Table 1: LUT Contents

Address	Data
0000	001 (1 bit matches)
0001	010 (2 bits match)
0010	000 (0 bits match)
0011	001 (1 bit matches)
0100	010 (2 bits match)
0101	011 (3 bits match)
0110	001 (1 bit matches)
0111	010 (2 bits match)
1000	010 (2 bits match)
1001	011 (3 bits match)
1010	001 (1 bit matches)
1011	010 (2 bits match)
1100	011 (3 bits match)
1101	100 (4 bits match)
1110	010 (2 bits match)
1111	011 (3 bits match)

The MASK parameter allows specific bits in the MATCH parameter to be excluded from the correlation equation. Those bits in the MASK parameter that are set to '1' indicate that the corresponding bits in the input data and the MATCH parameter should be compared, and if found identical, contribute to the correlator's SUM output. Those bits in the MASK parameter that are set to '0' indicate that the corresponding bits in the input data and the MATCH parameter should not be compared, and their match status should not affect the correlator's SUM output. See figures 1 and 2.

Data is loaded into the correlator on a rising clock edge and becomes instantly available at the data-output (DOUT) port. Correlators may be cascaded (by connecting the DOUT port of the first to the DIN port of the second) when multiple correlations must be performed on a time-series array of data. Larger correlators may be formed by splitting very large data words into smaller segments and presenting each to the DIN port of its own correlator. The overall correlation result is formed by summing the outputs of each correlator. (When cascading correlators in this fashion, make each correlator the same bit-width to ensure that the latency through each is identical, and the results arrive at their SUM outputs at the same instant.)

Pinout

Pin names for the schematic symbol are shown in Figure 5, and described in Table 2.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
DIN[n:0]	Input	Parallel Data In – Data input to correlator
C	Input	Data Clock – Data is captured and new output data is formed on rising clock transitions
DOUT[n:0]	Output	Parallel Data Out – Reflects current contents of correlator data register
SUM[m:0]	Output	Binary representation of the number of bits that match the correlation MATCH pattern excluding those bits identified in the MASK pattern.

Core Generator Parameters

The Core Generator parameterization window for this module is shown in Figure 1. The parameters are as follows:

Component Name: Enter a name for the output files generated for this module.

Correlation Width: Select the number of bits in the correlation window. May be any multiple of 4-bits in the range 4 to 128-bits.

Match Pattern: Enter the bit-pattern that the correlator should detect. The pattern may be expressed in hexadecimal or binary.

Mask Pattern: Enter the bit pattern that describes which bits in the Match pattern should be ignored. The pattern may be expressed in hexadecimal or binary. A '0' at any bit-position indicates that the corresponding bit in the match pattern should be ignored.

Radix: Indicate the base used to express the match and mask patterns.

Using Look-Up Tables for Implementing Correlators

The following example illustrates how the CORE Generator calculates the contents of its distributed look-up tables. The example shows a 4-bit correlator with an input match pattern of 1101 and a mask pattern of 1111 (include all bits).

Any N Bit correlator can be decomposed into (N/4) 4-Bit correlators. The LUTs contain all potential outputs for each 4-stage correlation. For example, the correlation pattern 1101 stores 4 at address D in the LUT (all four bits match) and 3 at addresses 5, 9, C, and F in the LUT (three bits match).
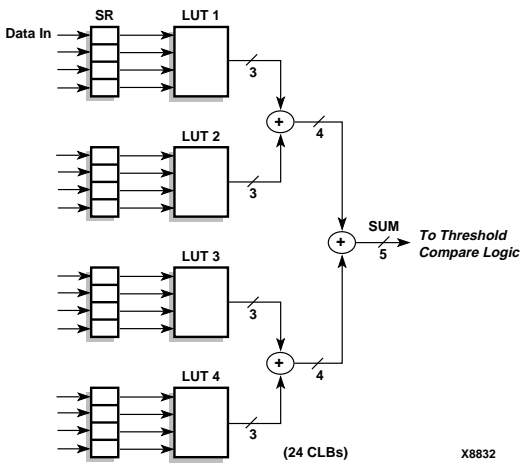
Figure 4: Combining 4-Input Sections

Combining 4-Input Correlator Sections

Each four-input correlator section can be combined by summing the outputs with an adder tree. The look-up tables are 16 words (4 address lines) by 3 bits wide each. The adder tree grows by one bit for each level and the resulting output is a binary number representing the number of matches in the input data word after the mask register has been applied.
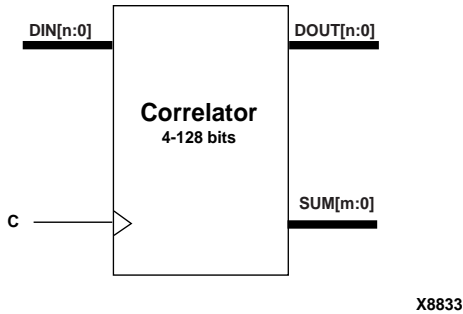

Figure 5: Parallel Correlator Schematic Symbol

Output Bit Width And Latency

The SUM output bus is M bits wide, where M is sufficient to express the largest value that can be calculated by the correlator. The largest value that the correlator will produce occurs when all bits in the input data window are identical to all bits in the MATCH parameter and all bits in the MASK parameter are '1's. At this time the correlator's output value will be M, the number of bits in the input data word. The out-put bitwidth is therefore $Log_2(M)+1$ rounded down to the previous whole number.

The correlator's latency is a function of input data word size, N. The function for determining the correlator's latency is as follows:

Table 3: Latency Table

N	Latency
<= 4	1
<= 8	2
<= 16	3
<= 32	4
<= 64	5
> 64	6

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Bit Width and CLB Count

Table 4 lists the number of CLBs required for example bit widths. The maximum speed is for XC4000E-1 devices.

Table 4: Bit Width versus CLB Count

Bit Width	CLB Count
4	4
7	11
8	14
9	16
10	17
11	19
12	20
13	22
14	24
15	26
16	25
17	29
20	36
32	54

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Mask	Hex/Binary String	
Bit_Pattern	Hex/Binary String	
Width	Integer	4 to 128 multiple of 4