ALLIANCE
Series Software

Synopsys Design Compiler
Implementation Flow

Module Generators

EDN

LogiBLOX

CORE Generator

3rd Party Schematic Simulator

May require user defined symbol if not part of a Xilinx provided interface.

.V
.VHD

.NGC= Xilinx Binary Netlist

NGC

.VEI
.VHI

VEO
VHO

Verilog & VHDL Instantiation

State Diagram Editor

Schematic Design Editor

HDL Editor

Synthesis & DesignWare Libraries

VHDL
Verilog

VHDL
Verilog

XNF
EDIF

VHDL
Verilog

EDN

Black Box Instantiation

Functional Simulation Flow

CORE Generator

LogiBLOX

UNIFIED

Gates

UniSim

VITAL & Verilog

SimPrim

VITAL, Verilog, Gates

HDL Test Bench

Command File or Test Vectors

VSS
VCS
or
3rd Party

SIMULATION

Timing Simulation Flow

VHDL
Verilog

SDF

EDIF

BIT
JEDEC

Reports

Xilinx

IMPLEMENTATION

Tools

Timing Requirements

SYNOPSYS
Design Compiler

DC2NCF

NCF

Timing Constraints

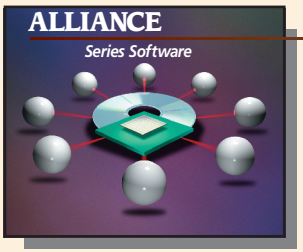
SEDIF

Synopsys EDIF

User Constraints File

EG

PN 0010418 01



Synopsys Design Compiler Information

Device Architecture Support

FPGA Product Family
Spartan
Virtex
XC4000X

CPLD Product Family
XC9500

Recommended Settings

Please refer to your A2.1i software installation and the example:
.synopsys_dc.setup
.synopsys_vss.setup
and the runscript files in
$XILINX/synopsys/examples

Xilinx Contacts and Technical Support

World Wide Web:
http://www.xilinx.com

North America
1-800-255-7778
hotline@xilinx.com
United Kingdom
44 1932-820821
ukhelp@xilinx.com

France
33 1-3463-0100
frhelp@xilinx.com
Japan
81 3-3297-9163
jhotline@xilinx.com

Synopsys Contacts and Technical Support

World Wide Web:
http://www.synopsys.com
United States
1-800-245-8005
support_center@synopsys.com

Guide Overview

1 Setup Design Compiler .synopsys_dc.setup file

Use the template **.synopsys_dc.setup examples** in the **$XILINX/synopsys/examples**. Add the correct information for your target die and speed grade. Modify the paths for your setup.

2 Create a compile script to read your input files

Use the example compile scripts in the **$XILINX/synopsys/examples** as a guide. Create a compile script to read all the HDL files for the design.

3 Synthesize the design by running the compile script with dc_shell or design_analyzer

Compile the design by running:
dc_shell -f runscript | tee run.log
or
design analyzer &
Either step will produce a .sedif file

4 Place and Route the .sedif file using the A2.1i software

Place and route the synthesized design via the **UNIX A2.1i commands**
or the
Design Manager GUI.

PN 0010418 01