Synopsys FPGA Compiler II Implementation Flow

Module Generators

LogiBLOX

CORE Generator

.V
.VHD

.NGC= Xilinx Binary Netlist

NGC

.VEI
.VHI

VEO
VHO

Verilog & VHDL Instantiation

State Diagram Editor

Schematic Design Editor

HDL Editor

VHDL Verilog

VHDL Verilog

EDIF

VHDL Verilog

EDN

Xilinx XNF Macros Library

Functional Simulation Flow

Timing Requirements

CORE Generator

LogiBLOX

UNIFIED

Gates

UniSim

VITAL, Verilog, Gates

SimPrim

VITAL, Verilog, Gates

HDL Test Bench

Command File or Test Vectors

VSS
VCS
or
3rd Party

SIMULATION

Timing Simulation Flow

VHDL Verilog

SDF

EDIF

BIT JEDEC

Reports

Xilinx

IMPLEMENTATION

Tools

XNF

FPGACompiler II

NCF

XNF

EDIF

Behavioral

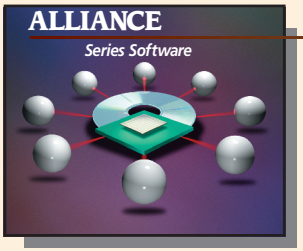
VHDL Verilog

EDIF for Virtex, VirtexE, Spartan II

User Constraints File

Functional Simulation Flow

PN 0010418 01



Synopsys FPGA Compiler II Information

Device Architecture Support

FPGA Product Family
Spartan
Virtex
XC4000X

CPLD Product Family
XC9500

Xilinx Contacts and Technical Support

World Wide Web:
http://www.xilinx.com

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Guide Overview

1 Create a project

Go to menu **File** → **New** and define a new project. All HDL files processed by FPGA Compiler II must be done through a project.

2 Add HDL files to project and analyze HDL files

After creating project, HDL design files can be added to the project. After adding the HDL design files, **FPGA *Compiler II*** will automatically analyze the HDL files.

3 Implement the design

Select the top-level **module/entity** in the **Design Sources** window and the **implement** button will be highlighted.
Click on the implement button and specify the target **die**, **speed grade** and **package**.
Strategies for synthesis can be specified during implementation.

4 Enter constraints

In the **Chips** window, **select the implementation**. Right-click on the selected implementation and select **Edit Constraints**. A window will appear where various constraints can be edited.
After entering constraints, save constraints by **closing the constraints window.**

5 Optimize the design

Click on the **optimize** button located next to the implement button to synthesize the design OR select the menu **Synthesis** → **Optimize Chip**

6 Place & Route an XNF or EDIF file with A2.1i

After optimization, write out the XNF or EDIF file by clicking on the **Export Netlist** button next to the implement button. **Place and Route** the XNF or EDIF file using **A2.1i implementation tools** with the Design Manager GUI or DOS shell based commands.