XILINX®

A2.1i FPGA Design Implementation Flow

Options | Main Flow

sedif, sxnf, edif, edn, edf, xnf, nmc, ncf

ucf → NGDBuild

ngd

MAP

map.ncd, map.ngm, pcf

PAR

ncd

BITGEN

bit

Static Timing Analysis

map.ncd/ ncd, pcf → TRCE → twr, mod, data

Timing Simulation

map.ncd, ncd, ngd, map.ngm, pcf → NGDAnno NGD2VER NGD2VHDL ← Simulation Options

NGDAnno NGD2VER NGD2VHDL → vhd, v, edn, sdf

Floorplanner

Floorplanner ↔ fnf

Floorplanner → mfp → MAP

ngd, map.ncd/ ncd, pcf → mfp

Pin Locking

ncd → PIN2UCF → ucf

FPGA Editor

ncd, pcf, nmc → FPGA Editor → ncd, pcf

FPGA Editor → NMC Physical Macro → NGDBuild

Multi-Pass Place and Route

No. of Place and Route Passes, Cost Table

map.ncd/ ncd, pcf

→ PAR

Graphical Constraints Editor

ngd → Graphical Constraints Editor ↔ ucf

Design Output Format

bit → PROMGEN → mcs, exo, hex

bit → Hardware Debugger

bit → JTAG Programmer

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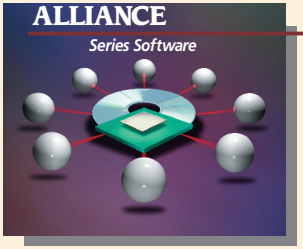

A2.1i FPGA Design Implementation Guide

Device Architecture Support

FPGA Product Family

Spartan
Virtex
XC4000X

Xilinx Contacts and Technical Support

World Wide Web:
http://www.xilinx.com

North America
1-800-255-7778
hotline@xilinx.com
United Kingdom
44 1932-820821
ukhelp@xilinx.com

France
33 1-3463-0100
frhelp@xilinx.com
Japan
81 3-3297-9163
jhotline@xilinx.com

Overview

1 Invoke the Design Manager

PC Invoke Design Manager
UNIX xilinx
Load the Design
File→New Project→Enter Input Design
Implement the Design
Design→Implement→Select target device, family, package, speedgrade.
Select "options" in Implement window
Edit Configuration, Implementation and Timing Simulation templates. Select RUN to implement the design.

2 Utilities and Tools

Utilities→Report Browser.
Browse the report of the various Implementation process.

Overview (Continued)

Utilities→Graphical Constraints Editor
Enter the Timing Constraints and I/O pin locations in Graphical Constraints Editor after the Translate(ngdbuild) process.

To Lock Pins
Implement Design, Select an implemented revision and Select Design→LockPins and generate pin locking constraints in UCF file format.

3 FPGA Programming

Tools→Hardware Debugger
Download your design to the device, verify the downloaded configuration. Display/Debug the internal states of the device.
Tools→PROM File Formatter
Create mcs, exo, or tek style files using created bit file.

4 Advanced FPGA Options

Tools→Floorplanner
Control the placement of your design into a target FPGA part using a drag and drop paradigm with the mouse pointer. Perform after MAP and PAR process.
Tools→FPGA Editor
Create, Display and Modify your designs before and after place and route. May also use to create hard macros.

Multi-Pass Place and Route
Implement design to mapping/PAR stage, Select the version of Implemented Design and Select Design→FPGA Multi-Pass Place and Route and choose the options for multipass place and route.
Tools→Timing Analyzer
Perform a timing analysis on a design using available timing constraints

Notes:
In the flow engine, to stop after a particular implementation process, Select Setup→stop after select a process stage. Use the stamp option in the trce command to generate a STAMP Model file (.mod) and a STAMP data file (.data) for board level static timing analysis.
Please refer to the Xilinx Synthesis and Simulation Design Guide for other options and commands for command line users.

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