GVA-220 DSP Hardware Accelerator

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Features

- 65 MHz maximum input A/D sample rate
- 30 MHz sample Bandwidth
- Each FPGA has access to both A/Ds
- Each FPGA has access to both D/As (via Local Bus)
- FPGA Logic Expansion (from 13K to 85K gates)
- Two Dedicated 64K X 16 SRAM for each FPGA
- 42-bit FPGA Local Bus with External Data Access
- Master Parallel, Master Serial configurable via Download Cable (Model DLC4)
- 120 MHz maximum output D/A sample rate
- Separate FPGA Power Plane for Power Measurement
- External 3.3V Jack for High Current FPGAs
- Programmable A/D Sample Clock
- On Board 120 MHz Clock Oscillator
- External High Stability Clock Input

General Description

The GVA-220 Digital Signal Processing Hardware Accelerator is designed for the implementation of complex DSP or other channel coding designs. This platform provides a highly flexible environment for the integration of various software and hardware DSP applications using the Xilinx XC4000XL/XLA and Spartan/SpartanXL families.

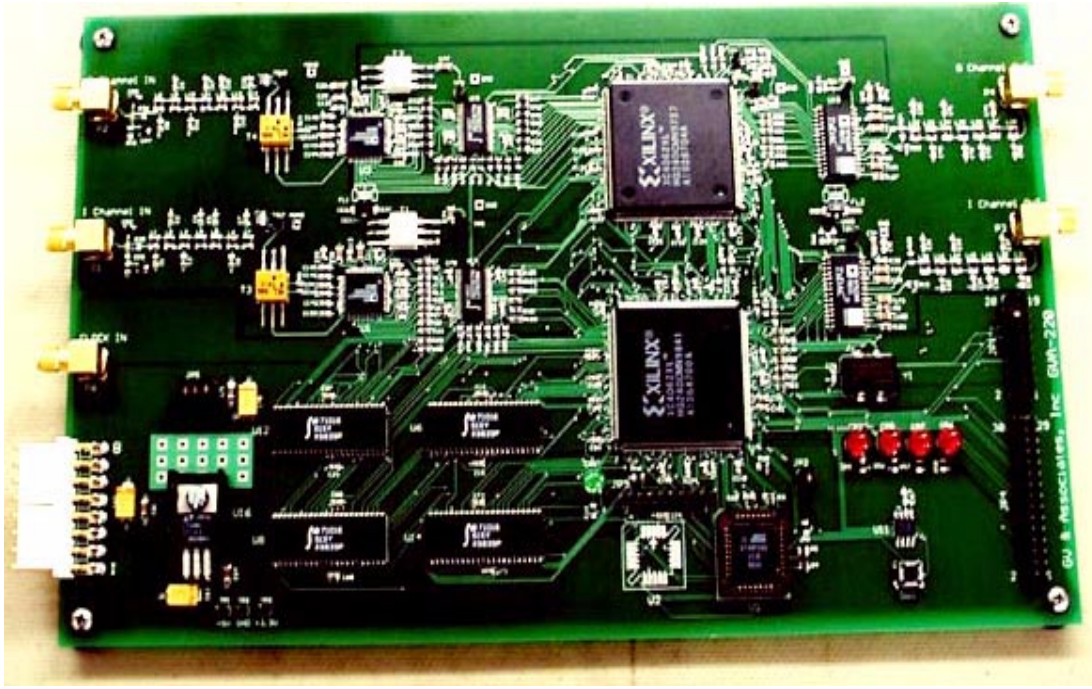

Figure 1: GVA-220 DSP Hardware Accelerator

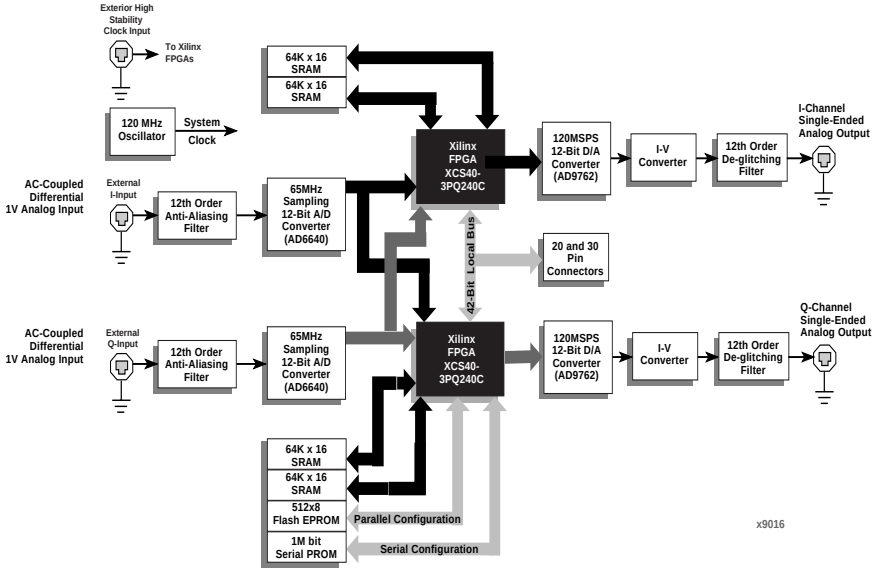

Figure 2: GVA-220 Spartan FPGA Block Diagram

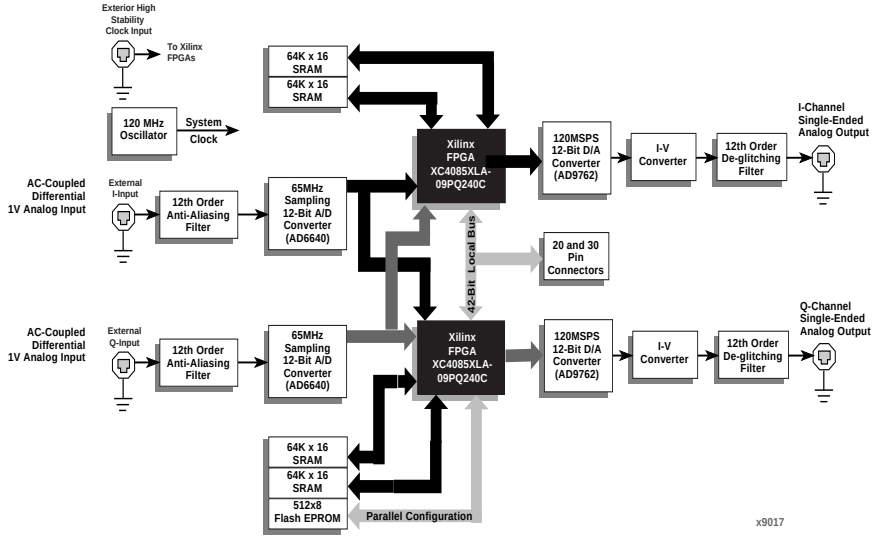

Figure 3: GVA-220 4000XL/4000XLA FPGA Block Diagram

The GVA-220 supports the following XIlinx PFGAs:

- XC4013XLA-09PQ240C
- XC4020XLA-09HQ240C
- XC4028XLA-09HQ240C
- XC4036XLA-09HQ240C
- XC4044XLA-09HQ240C
- XC4052XLA-09HQ240C
- XC4062XLA-09HQ240C
- XC4085XLA-09HQ240C
- XCS30XL-4PQ240C
- XCS40XL-4PQ240C
- XCS30-3PQ240C
- XCS40-3PQ240C

Functional Description

The platform's general configuration consists of an I channel and a Q channel which are passed through a 12th order low pass filter. The 12th order low pass filter band limits the input signals to a 30 MHz bandwidth. The signal rejection is -58 dB at 40 MHz. Next, the signals are digitized by a 12 bit A/D. The sample rate (maximum of 65 MHz) of the A/D is programmable as it is generated by the Xilinx FPGA using either the on-board clock or the external clock. The digitized signals are now ready to be processed by the customer's algorithm that is implemented in hardware by either of the two Xilinx FPGAs. Once the signals have been processed, a 120 MSPS D/A converts them back to an analog waveform. The processed data can also be sent to the external 36-bit data port. The processed analog waveforms are passed through a 12th order smoothing filter which is band limited to 30 MHz. The filtered analog signal is connected to a 50 ohm SMA output for viewing.

Each Xilinx FPGA has access to two 64K x 16-bit static RAMs that can be used for temporary data storage. These SRAMs can be configured as two independent 64K x 16-bit banks or as a single 64K x 32-bit bank. By using an internal multiplexer, the two SRAMs can also be configured as a single 128K x16-bit bank.

The I channel Xilinx FPGA can also access unused address space in the configuration EPROM and share that data with the Q channel Xilinx FPGA via the local bus. The two Xilinx FPGAs have a 42-bit local bus that allows for the direct transfer of data between the two devices and other external devices. Using the 42-bit local bus, the I and Q channel FPGAs can be configured to have an off-board interface to an external processor such as a TMS320C31 or other Digital Signal Processor. For non-specific clock requirements, an external clock source is available.

The GVA-220 Digital Signal Processing Hardware Accelerator is designed to support the Xilinx 4000XL, 4000XLA, Spartan and SpartanXL families.

Ordering Information

This product is available directly from GV & Associates. Please contact them for pricing and more information.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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