GVA-250 Virtex DSP Hardware Accelerator

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Features

- 65 MHz maximum input A/D sample rate
- 30 MHz sample Bandwidth
- Each FPGA has access to both A/Ds
- Each FPGA has access to both D/As (via Local Bus)
- FPGA Logic Expansion (20K to 800K gates)
- Two Dedicated 64K X 16 SRAM for each FPGA
- Up to 114,688 bits of internal Block RAM
- Four Delay Locked Loops (DLL)
- 55-bit FPGA Local Bus with External Data Access
- Master Parallel, Master Serial and Download Cable (Model DLC4) Configurable
- 120 MHz maximum output D/A sample rate
- Separate FPGA Power Plane for Power Measurement
- External 2.5V Jack for High Current FPGAs
- Programmable A/D Sample Clock
- On Board 120 MHz Clock Oscillator
- External High Stability Clock Input

General Description

The GVA-250 Digital Signal Processing Hardware Accelerator is designed for the implementation of complex DSP or other channel coding designs. This platform provides a highly flexible environment for the integration of various software and hardware DSP applications using the Xilinx Virtex FPGA family.

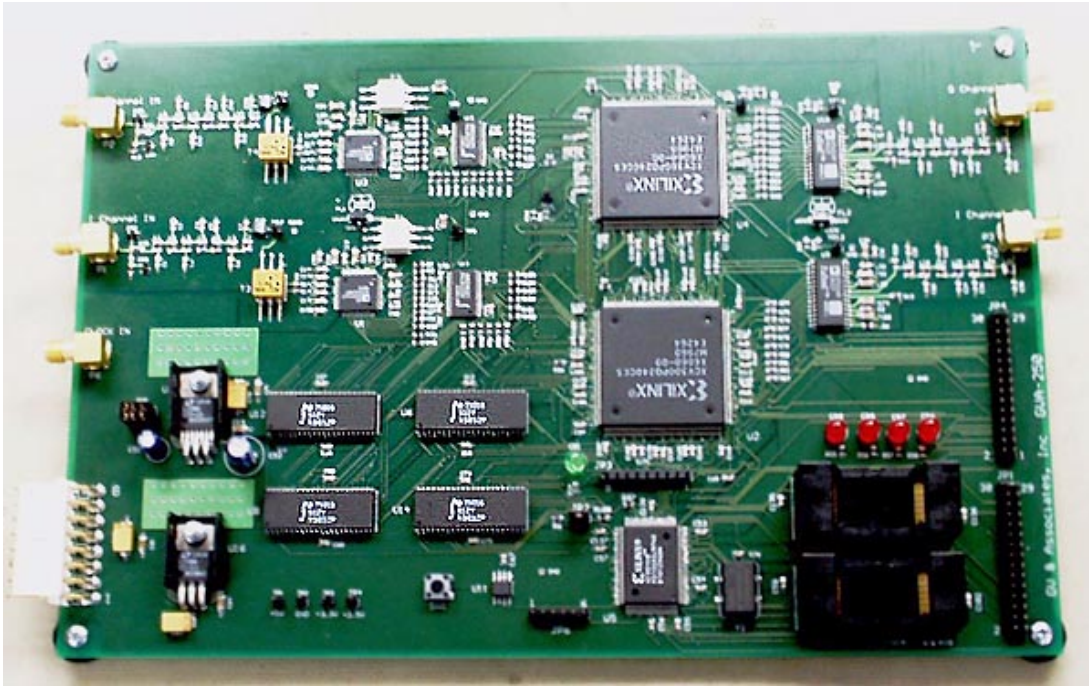

Figure 1: GVA-250 Virtex DSP Hardware Accelerator

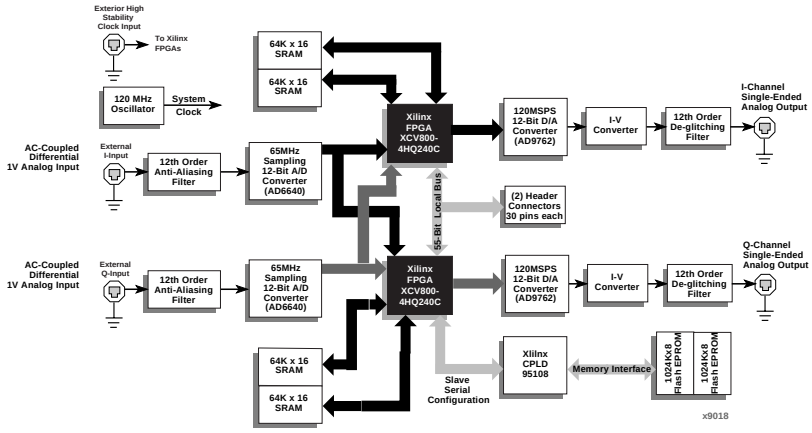

Figure 2: GVA-250 Virtex FPGA Block Diagram

The GVA-250 supports the following Xilinx FPGAs:

XCV50-4PQ240C

XCV100-4PQ240C

XCV150-4PQ240C

XCV200-4PQ240C

XCV300-4PQ240C

XCV400-4HQ240C

XCV600-4HQ240C

XCV800-4HQ240C

Functional Description

The platform's general configuration consists of an I channel and Q channel which are passed through a 12th order low pass filter. The 12th order low pass filter band limits the input signals to a 30 MHz bandwidth. The signal rejection is -58 dB at 40 MHz. Next, the signals are digitized by a 12-bit A/D. The sample rate (maximum of 65 MHz) of the A/D is programmable as it is generated by the Xilinx FPGA using either the on-board clock or external clock. The digitized signals are now ready to be processed by the customer's algorithm that is implemented in hardware by either of the two Xilinx FPGAs. Once the signals have been processed, a 120 MSPS D/A converts them back to an analog waveform. The processed data may also be sent to the external data port. The processed analog waveforms are passed through a 12th order smoothing filter which is band limited to 30 MHz. The filtered analog signal is connected to a 50 ohm SMA output for viewing.

Each Xilinx FPGA has access to two external 64K x 16-bit static RAMs that could be used for temporary data storage. These SRAMs can be configured as two independent 64K x 16-bit banks or as a single 64K x 32-bit bank. By using an internal multiplexer, the two SRAMs can also be configured as a single 128k x 16-bit bank. Each Xilinx FPGA supported has 32,768 to 114,688 bits of internal Block RAM.

The I channel Xilinx FPGA may also access unused address space in the configuration Flash EPROM and share that data with the Q channel Xilinx FPGA via the local bus. The two Xilinx FPGAs have a 55-bit local bus that allows direct transfer of data between the two devices and other external devices. Using the 55-bit local bus, the I channel and the Q channel FPGAs can be configured to have an off-board interface to an external processor such as a TMS320C31 or other Digital Signal Processor. For non-specific clock requirements, an external clock source is available. Each Xilinx FPGA has four Delay Locked Loops (DLL) for system clock synchronization.

Ordering Information

This product is available directly from GV & Associates. Please contact them for pricing and more information.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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