LogiCORE™

PCI Master & Slave Interfaces Version 1.2.0

May 25, 1997

Product Specification

XILINX®

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Features

- Fully 2.1 PCI compliant 32 bit, 33MHz PCI Interface
  - Master (Initiator/Target)
  - Slave (Target-only)
- Pre-defined implementation for predictable timing in Xilinx XC4000E FPGAs or HardWire (see *LogiCORE Facts* for listing of supported devices)
- Fully verified design
  - Simulated using VirtualChips™ PCI testbench
  - Tested in hardware (silicon proven)
- Configurable on-chip FIFO can be added for maximum burst speed (see *Xilinx Documents* section)
- Programmable single-chip solution with customizable back-end functionality
- Design Once™ - automatic conversion to HardWire for cost reduction
- Supported Initiator functions (PCI Master only)
  - Initiate Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Read Line (MRL) commands
  - Initiate I/O Read, I/O Write commands
  - Initiate Configuration Read, Configuration Write commands
  - Bus Parking
- Supported Target functions (PCI Master and Slave)
  - Type 0 Configuration Space Header
  - Up to 2 Base Address Registers (memory or I/O with adjustable block size from 16 bytes to 256 Mbytes, slow decode speed)
  - Parity Generation (PAR), Parity Error Detection (PERR# and SERR#)
  - Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Real Line (MRL), Memory Write, Invalidate (MWI) commands
  - I/O Read, I/O Write commands
  - Configuration Read, Configuration Write commands

LogiCORE™ Facts

Core Specifics	
Device Family	XC4000E
CLBs Used	152 - 268
IOBs Used[5]	53/51
System Clock f_{max}	0 – 33MHz
Device Features Used	Bi-directional data buses SelectRAM™ (optional user FIFO) Boundary scan (optional)

Supported Devices[1]/Resources Remaining		
	I/O[5]	CLB[2]
XC4013E PQ160[6]	-/76	308 - 424
XC4013E PQ208	107/109	308 - 424
XC4013E HQ240	141/143	308 - 424
XC4020E HQ208	107/109	516 - 632
XC4020E HQ240	141/143	516 - 632

Provided with Core	
Documentation	User's Guide PCI Interface Protocol Checklist V1.0 to V1.1 Comparison Ping Ref. Design Users Guide
Design File Formats	VIEW*logic* schematics XNF Netlist[3]
Constraint Files	TimeSpecs, RPMs, Guide files, sample synthesis script
Verification Tool	VIEW*logic* command files VHDL Testbench Verilog Testbench
Schematic Symbols	VIEWlogic, VHDL, Verilog
Evaluation Model	VHDL, Verilog Simulation Model[3]
Reference designs & application notes	Example design Ping Reference Design[4]
Additional Items	Reference book: PCI System Architectures

Design Tool Requirements	
Xilinx Core Tools	XACTstep 5.2.1/6.0.1
Entry/Verification Tools	For CORE generator: VHDL, Verilog, Schematic For changing source files: Workview Office V7.1.2 or V7.2

Notes: See next page.

LogiCORE™ Facts (cont.)

Support

Xilinx provides technical support for this LogiCORE product when used as described in the User's Guide or supporting Application Notes. Xilinx cannot guarantee timing, functionality, or support of the product if implemented in devices not listed above, or customized beyond that referenced in the product documentation, or if any changes are done in sections of the design marked as "DO NOT MODIFY".

Notes:
1. Speed grade is determined by PCI configuration and user back-end, see Figure 3.
2. The exact number of CLBs and depends on user configuration of the core and level of resource sharing with adjacent logic.
3. Available on Xilinx Home Page, in the LogiCORE PCI VIP Lounge: www.xilinx.com/products/logicore/logicore.htm
4. See heading "Ping Reference Design"
5. Master/Slave
6. Slave only

Features (cont.)

- 32-bit data transfers, burst transfers with linear address ordering
- Target Abort, Target Retry, Target Disconnect
- Full Command/Status Register

• Supported by Xilinx CORE Generator
- Web-based configuration
- Generation of proven design files

Applications

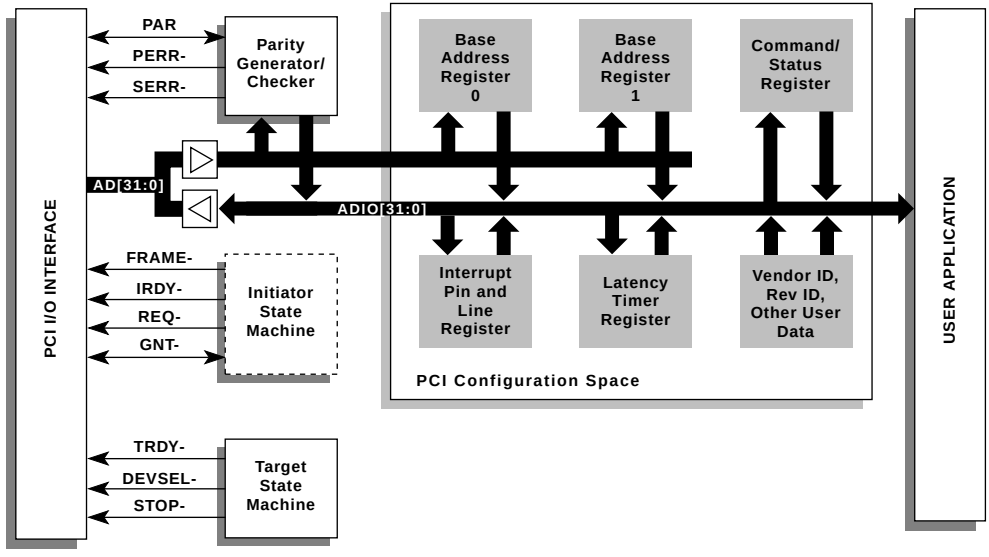
• Add-in boards such as graphic cards, video adapters, LAN adapters and data acquisition boards.
• Embedded applications within telecommunication and industrial systems.
• Other applications that need PCI

General Description

The LogiCORE™ Master and Slave Interfaces are pre-implemented and fully tested modules for Xilinx XC4000E FPGAs (see *LogiCORE Facts* for listing of supported devices). The pin-out and the relative placement of the internal Configurable Logic Blocks (CLBs) are pre-defined. Critical paths are controlled by TimeSpec's to ensure that timing is always met. This significantly reduces engineering time required to implement the PCI portion of your design. Resources can instead be focused on the unique back-end logic in the FPGA and the system level design. As a result, the LogiCORE PCI products can cut your development time by several months.

Xilinx XC4000E Series FPGAs enables designs of fully PCI-compliant systems. The devices meet all required electrical and timing parameters including AC output drive characteristics, input capacitance specifications (10pF), 7 ns setup and 0 ns hold to system clock, and 11 ns system clock to output. The *PCI Compliance Checklist XC4000E* has additional details (see the *Xilinx Documents* section). Other features that enable efficient implementation of a complete PCI system in the XC4000E includes:

• Select-RAM™ memory: on-chip ultra-fast RAM with synchronous write option and dual-port RAM option. Used in the PCI Interfaces to implement the FIFO.
• Individual output enable for each I/O



- Internal 3-state bus capability
- 8 global low-skew clock or signal distribution networks
- IEEE 1149.1-compatible boundary scan logic support

See *Xilinx 1996 Data Book* for more details.

The module is carefully optimized for best possible performance and utilization in the XC4000E FPGA architecture. Implemented in the smallest supported FPGA, XC4013, more than 50% of the FPGA's resources remain for integrating a unique back-end interface and other system functions into a fully programmable one-chip solution.

Xilinx DesignOnce™ service allows an automatic conversion to a low cost HardWire™ device for high-volume production.

Functional Description

The LogiCORE PCI Master Interface is partitioned into five major blocks, plus the user application, shown in Figure 1. Each block is described below.

PCI I/O Interface Block

The I/O interface block handles the physical connection to the PCI bus including all signaling, input and output synchronization, output three-state controls, and all request-grant handshaking for bus mastering.

Parity Generator/Checker

Generates/checks even parity across the AD bus, the CBE lines, and the PAR signal. Reports data parity errors via PERR- and address parity errors via SERR-.

Target State Machine

This block manages control over the PCI interface for Target functions. The states implemented are a subset of equations defined in "Appendix B" of the *PCI Local Bus Specification*. The controller is a high-performance state machine using state-per-bit (one-hot) encoding for maximum performance. State-per-bit encoding has narrower and shallower next-state logic functions that closely match the Xilinx FPGA architecture.

Initiator State Machine (PCI Master only)

This block manages control over the PCI interface for Initiator functions. The states implemented are a subset of equations defined in "Appendix B" of the *PCI Local Bus Specification*. The Initiator Control Logic also uses state-per-bit encoding for maximum performance.

PCI Configuration Space

This block provides the first 64 bytes of Type 0, version 2.1, Configuration Space Header (CSH) (see Table 1) to support software-driven "Plug-and Play" initialization and configuration. This includes Command, Status, and two Base Address Registers (BARs). These BARs illustrate how to implement memory- or I/O-mapped address spaces. Each BAR sets the base address for the interface and allows the system software to determine the addressable range required by the interface. Using a combination of Configurable Logic Block (CLB) flip-flops for the read/write registers and CLB look-up tables for the read-only registers results in optimized packing density and layout.

Table 1. PCI Configuration Space Header

31	16	15	0	
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Rev ID	08h
BIST	Header Type	Latency Timer	*Cache Line Size*	0Ch
Base Address Register 0 (BAR0)				10h
Base Address Register 1 (BAR1)				14h
Base Address Register 2 (BAR2)				18h
Base Address Register 3 (BAR3)				1Ch
Base Address Register 4 (BAR5)				20h
Base Address Register 5 (BAR5)				24h
Cardbus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved				34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch

Note:
Italicized address areas are not implemented in the LogiCORE PCI Interface default configuration. These locations return zero during configuration read accesses.

User Application with Optional Burst FIFOs

The LogiCORE PCI Interface provides a simple, general-purpose interface with a 32-bit data path and latched address for de-multiplexing the PCI address/data bus. The general-purpose user interface allows the rest of the device to be used in a wide range of applications.

Typically, the user application contains burst FIFOs to increase PCI system performance (An Application Note is available, please see the *Xilinx Documents* section). An on-chip read/write FIFO, built from the on-chip synchronous

dual-port RAM (SelectRAM™) available in XC4000E devices, supports data transfers in excess of 33 MHz.

Core Configuration

The LogiCORE PCI Interface can easily be configured to fit unique system requirements using Xilinx web-based CORE Generator or changing the Viewlogic schematics. Following customization is supported by the LogiCORE product and described in accompanying documentation.

- Initiator or target functionality (PCI Master only)
- Base Address Register configuration (1 - 2 Registers, size and mode)
- Configuration Space Header ROM
- Initiator and target state machine (e.g., termination conditions, transaction types and request/transaction arbitration)
- Burst functionality
- User Application including FIFO (back-end design)

Table 2. PCI Bus Commands

CBE [3:0]	Command	PCI Master	PCI Slave
0000	Interrupt Acknowledge	No[1]	Ignore
0001	Special Cycle	No[1]	Ignore
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	*Reserved*	*Ignore*	*Ignore*
0101	*Reserved*	*Ignore*	*Ignore*
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	*Reserved*	*Ignore*	*Ignore*
1001	*Reserved*	*Ignore*	*Ignore*
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Memory Read Multiple	Yes	Yes
1101	Dual Address Cycle	No[1]	Ignore
1110	Memory Read Line	Yes	Yes
1111	Memory Write Invalidate	No[1]	Yes

Note:
1. The Initiator can present these commands, however, they either require additional user-application logic to support them or have not been thoroughly tested.

Supported PCI Commands

Table 2 illustrates the PCI bus commands supported by the LogiCORE PCI Interface. The *LogiCORE™ PCI Interface Protocol Checklist (2.1)* has more details on supported and unsupported commands (see the *Xilinx Documents* section)

Burst Transfer

The PCI bus derives its performance from its ability to support burst transfers. The performance of any PCI application depends largely on the size of the burst transfer. A FIFO to support PCI burst transfer can efficiently be implemented using the XC4000E on-chip RAM feature, SelectRAM™. Each XC4000E CLB supports two 16x1 RAM blocks. This corresponds to 32 bits of single-ported RAM or 16 bits of dual-ported RAM, with simultaneous read/write capability. Table provides a summary of different FIFO sizes and performance in an XC4000E-2.

To reliably perform a burst transfer in a generic PCI system the LogiCORE Interface automatically inserts a wait state when it is supplying data to the PCI bus. Consequently, the LogiCORE Interface can accept data at 100% burst transfer rate and supply data at 50%. See Table 4 for a PCI bus transfer rates for various operations.

The resulting PCI bus bandwidth is shown in Figure 2.

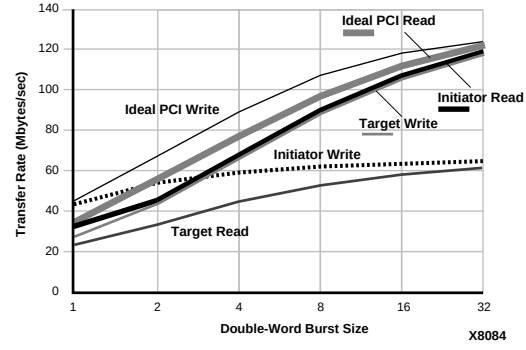


Figure 2. PCI Bus Bandwidth

Pinout

The LogiCORE™ PCI Master and Slave Interfaces support the PCI-SIG recommended pin-out for add-in cards. Tables 5 to 7 describe the signals and pin-out for the LogiCORE PCI Master and Slave Interfaces. See the *LogiCORE PCI Master and Slave Interface User's Guide* for a detailed signal description.

Table 3. XC4000E-2 Synchronous FIFO Modules

Depth x Width	# CLBs	Single Port Performance	Equivalent Dual-port Performance
16x16	23	65 MHz	130 MHz
32x8	28	50 MHz	100 MHz
64x8	48	50 MHz	100 MHz
16x32	48	50 MHz	100 MHz

Table 4. LogiCORE PCI Transfer Rates

Operation	Transfer Rate
Initiator Write (PCI ← LogiCORE)	3-2-2-2
Initiator Read (PCI → LogiCORE)	4-1-1-2
Target Write (PC I→ LogiCORE)	5-1-1-1
Target Read (PCI ← LogiCORE)	6-2-2-2

Note:
Initiator Read and Target Write operations have effectively the same bandwidth for burst transfer.

Table 5. Signal Description (internal signals)

Signal Name	Signal Description	Target	Initiator
Address/Data			
AD[31:0]	PCI Address/Data Bus	I/O	I/O
CBE[3:0]	Command/Byte Enable	In	I/O
PAR	PCI Parity Signal	I/O	I/O
Interface			
FRAME	Frame	In	I/O
TRDY	Target Ready	Out	I/O
IRDY	Initiator Ready	In	I/O
STOP	Stop	Out	I/O
DEVSEL	Device Select	Out	I/O
IDSEL	Initialization Device Select	In	In
LOCK	Lock	In	I/O
Interrupts			
INTD	Interrupt D	N/A	N/A
INTC	Interrupt C	N/A	N/A
INTB	Interrupt B	N/A	N/A
INTA	Interrupt A	OD	OD
Cache (not supported)			
SDONE	PCI SDONE	N/A	N/A
SBO	PCI SBO	N/A	N/A
Error Signals			
PERR	Parity Error	Out	I/O
SERR	System Error	OD	OD
Arbitration			
REQ	Request PCI Bus	N/A	Out
GNT	Grant PCI Bus	N/A	In
Boundary Scan			
TDI	Test Data Input	In	In
TMS	Test Mode Select	In	In
TCK	Test Clock	In	In
TDO	Test Data Output	Out	Out
Miscellaneous			
RST	Global Reset	In	In
CLK	PCI Clock	In	In

Note:
Signals marked N/A are not applicable or not supported. Signals marked OD are Open Drain output.

Table 6. Signal Description (internal signal)

Signal Name	Signal Description	Target	Initiator
Cycle Control			
FRAME-	Frame	Out	Out
IRDY-	Initiator Ready	Out	Out
TRDY-	Target Ready	Out	Out
STOP-	Stop Transaction	Out	Out
DEVSEL-	Device Selected	Out	Out
Bus Control			
BASE_HIT	Base Address Hit	Out	Out
ADDR_VLD	Address Valid	Out	Out
DATA_VLD	Data Valid	Out	Out
CNFG_VLD	Configuration Valid	Out	Out
S_WRDN	Slave Write/Read Dir.	Out	Out
PCI_CMD[15:0]	PCI Bus Command	Out	Out
S_CBE[3:0]	Slave Comm/Byte Enable	Out	Out
Address/Data			
ADDR[31:0]	Latched Address Bus	Out	Out
ADIO[31:0]	Address/Data Bus	I/O	I/O
PERR-	Data Parity Error	In	In
User Control			
READY	Ready	In	In
TERM	Terminate Transaction	In	In
T_ABORT	Target Abort	In	In
SRC_EN	Source Data Enable	Out	Out
INTR-	Interrupt	In	In
KEEPOUT	Keep Out	In	In
Initiator Only Functions			
REQUEST	Request Transaction	N/A	In
M_CBE[3:0]	Master Comm/Byte Enable	N/A	In
M_WRDN	Master Write/Read Dir.	N/A	In
COMPLETE	Complete Transaction	N/A	In
TIME_OUT	Latency Timer Timeout	N/A	Out
State Bits (Initiator)			
M_DATA	Data Transfer State	N/A	Out
DR_BUS	Bus Parked	N/A	Out
M_ADDR-	Addr. State/Bus Parking	N/A	Out
I_IDLE	Initiator Idle State	N/A	Out
State Bits (Target)			
IDLE	Target Idle State	Out	Out
B_BUSY	PCI Bus Busy	Out	Out
S_DATA	Data Transfer State	Out	Out
BACKOFF	TERM Asserted	Out	Out
FREE	Free State	Out	Out
LOCKED	Locked State	Out	Out
Status Output			
CSR[39:0]	Extended Comm/Status	Out	Out

Note:
Signals marked I/O are using internal tri-state.

Table 7. LogiCORE PCI Pinout

PCI Signal	PQ160	PQ/HQ208	HQ240
AD31	147	192	225
AD30	148	193	226
AD29	149	195	228
AD28	150	196	229
AD27	152	197	230
AD26	153	198	231
AD25	154	199	232
AD24	155	200	233
AD23	158	6	4
AD22	3	7	5
AD21	4	10	8
AD20	5	11	9
AD19	8	12	10
AD18	9	13	11
AD17	11	15	15
AD16	12	16	16
AD15	30	33	41
AD14	31	34	42
AD13	32	35	43
AD12	33	36	44
AD11	34	38	48
AD10	35	39	49
AD9	36	40	50
AD8	45	41	51
AD7	47	60	66
AD6	49	61	67
AD5	50	63	69
AD4	52	64	70
AD3	53	65	71
AD2	54	66	72
AD1	55	68	76
AD0	56	69	77
CBE3	156	201	236
CBE2	14	18	18
CBE1	28	32	36
CBE0	46	59	65
PAR	26	30	34
FRAME-	16	20	24
TRDY-	18	22	26
IRDY-	17	21	25

PCI Signal	PQ160	PQ/HQ208	HQ240
STOP-	22	24	28
DEVSEL-	21	23	27
IDSEL	157	203	238
LOCK-	23	27	31
INTA			
PERR-	24	28	32
SERR-	25	29	33
REQ	N/A	31	35
GNT	N/A	19	23
TDI	6	8	6
TMS	13	17	17
TCK	7	9	7
TDO	121	159	181
RST-	83	109	123
CLK	2	4	2

Timing Specification

The XC4000E family, together with the LogiCORE PCI products enables design of fully compliant PCI systems. The choice of FPGA speed grade for your PCI application is determined by the PCI configuration and your back-end design as illustrated in Figure 3. Factors affecting your back-end designs include loading of hot signals coming directly from the PCI bus, gate count and floor planning. Table 8 shows the key timing parameters for the LogiCORE PCI Interfaces that must be met for full PCI compliance.

Figure 3. Choice of Speed Grade

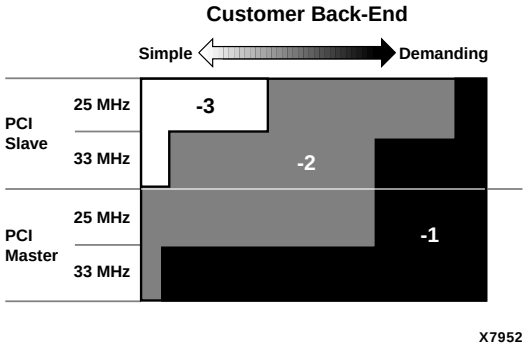


Table 8. Timing Parameters [ns]

Parameter	Ref.	PCI Spec.		LogiCORE PCI, XC4000E-2/1	
		Min	Max	Min	Max
CLK Cycle Time		30	∞	30[1]	∞
CLK High Time		11		11	
CLK Low Time		11		11	
CLK to Bus Signals Valid[4]	T_{ICK-OF}	2	11	2[2]	9.4[3]
CLK to REQ# and GNT# Valid[4]	T_{ICK-OF}	2	12	2[2]	9.4[3]
Tri-state to Active		2		2[2]	
CLK to Tri-state			28		28[1]
Bus Signal Setup to CLK (IOB)	T_{PSU}		7		6[3]
Bus Signal Setup to CLK (CLB)			7		7[1]
GNT# Setup to CLK	T_{PSU}		10		6[3]
Input Hold Time After CLK (IOB)	T_{PH}		0		0[3]
Input Hold Time After CLK (CLB)			0		0[2]
RST# to Tri-state			40		40[2]

Notes:
1. Controlled by TimeSpecs, included in product
2. Verified by analysis and bench-testing
3. Advanced speed grade data
4. IOB configured for Fast slew rate

Verification Methods

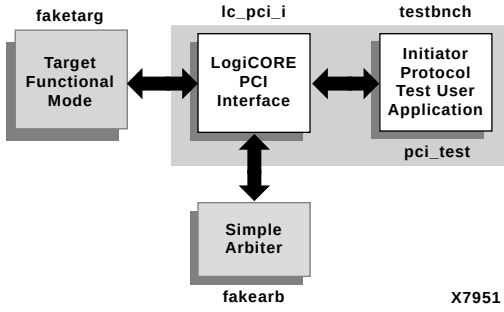
The LogiCORE PCI Interfaces have been extensively simulated using the VirtualChips VHDL PCI test bench from Phoenix Technologies, Ltd. (not included with the LogiCORE™ PCI products). The Interface has also been verified in hardware in the XC4013E-2 PQ208C FPGA.

Included with the LogiCORE™ PCI Master and Slave Interface is an example design and a VIEW*logic* based PCI protocol test bench that verifies the PCI interface functions according to the test scenarios specified in the *PCI Local Bus Specification* see Figure 4. This test bench consists of 28 test scenarios, each designed to test compliance to a specific PCI bus operation. Refer to the *LogiCORE PCI Interface Protocol Checklist* for a complete list of supported test scenarios (see the *Xilinx Documents* section).

Ping Reference Design

The Xilinx LogiCORE PCI “PING” Application Example, delivered in VHDL and Verilog, has been developed to provide an easy-to-understand example which demonstrates many of the principles and techniques required to successfully use the LogiCORE™ PCI macro in a System On A Chip solution.

Figure 4. PCI Protocol Testbench



Recommended Design Experience

The LogiCORE PCI interface is pre-implemented allowing engineering focus at the unique back-end functions of a PCI design. Regardless, PCI is a high-performance system that is challenging to implement in any technology, ASIC or FPGA. Therefore, we recommend previous experience with building high-performance, pipelined FPGA designs using Xilinx implementation software, Floorplanner, TIMESPECs, and guide files. The challenge to implement a complete PCI design including back-end functions varies depending on configuration and functionality of your application. Contact your local Xilinx representative for a closer review and estimation for your specific requirements.

Table 9. Part Numbers

Product	Part Number	Supplier
LogiCORE™ PCI Master (Intiator/Target)	LC-DI-PCIM-C	Xilinx, Inc.
LogiCORE™ PCI Slave (Target Only)	LC-DI-PCIS-C	Xilinx, Inc.

Ordering Information

Table 9 shows the part numbers for the LogiCORE™ products. Before placing an order, please read and sign the attached LogiCORE™ license agreement and fax it to Xilinx at +1 408-879-4780. For pricing and availability please contact your local Xilinx sales office.

Related Information

Recommended Design Centers

Listed below are design centers and design consultants that have experience with the LogiCORE PCI products.

HighGate Design
12380 Saratoga-Sunnyvale Road, Suite 8
Saratoga, CA 95070-3090, USA
Phone: +1 408-255-7160
Fax: +1 408-255-7162
E-mail: highgate@highgatedesign.com
URL: www.highgatedesign.com

Memec Design Services
1819 S. Dobson Rd., Ste. 203
Mesa, Arizona 85202, USA
Phone: +1 602-491-4311
Fax: +1 602-491-4907
E-mail: info@memecdesign.com
URL: www.memecdesign.com

Comit Systems
1250 Oakmead Pkwy, Suite 210
Sunnyvale, CA 94088, USA
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Fax: +1 408-988-2133
E-mail: preeth@comit.com
URL: www.comit.com

PCI Special Interest Group (PCI-SIG) Publications

The PCI-SIG publishes various PCI specifications and related documents such as *PCI Local Bus Specification*, *PCI Compliance Checklist* and *PCI System Design Guide*.

PCI Special Interest Group
2575 NE Kathryn St #17
Hillsboro, OR 97124
Phone: +1 800-433-5177 (inside the US)
+1 503-693-6232 (outside the US)
Fax: +1 503-693-8344
Office hours: 8:30am - 4:00pm PST
E-mail: info@pcisig.com
URL: www.pcisig.com

Xilinx Documents

More PCI related information is available on Xilinx Web: www.xilinx.com/products/logicore/logicore.htm.

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