LogiCORE™ Comb Filter

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XILINX®

DSP CORE Generator

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Features

- Multiplier-free filter yields efficient implementation
- All zeros, no poles
- Input data widths from 2 to 32 bits
- Variable length feed-forward path selection (configurable delay) from 1 to 17 samples
- Registered outputs
- Sections can be cascaded
- 2's complement input data
- Uses fast carry logic for high speed
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Can be combined with an Integrator core to build integrating and decimating filters as described by Hogenauer.

Functional Description

The Comb filter provides a standard differentiator with variable length feed-forward delays from 1 to 17 incoming sample periods. The subtractor takes the feed-forward delayed input data and subtracts it from the data input to give a registered output that is one bit wider than the input.

Multiple Comb Filter stages can be cascaded by connecting the output of the first stage to the input of the second stage and parameterizing the proper bit widths to allow for bit growth through the multiple adder stages. The data output from the last stage can be truncated (the least significant bits not connected) to carry the desired amount of precision to the next signal processing block.

Latency for this block is equal to the number of feed-forward delays plus one for the output register.

The Comb filter transfer function, $H_c(z) = 1\text{-}z^{-M}$, has M roots which map as zeros (nulls) on the unit circle of the complex Z plane. The corresponding frequency response exhibits nulls at $f_k = (f_s/M)k$, where:

f_s = sample frequency
M = feed-forward path delay samples
k = 0, 1, 2, 3, …, M

The amplitude-frequency response resembles the teeth of a comb, and the cascading of Comb filters produces sharper teeth. Because a one-bit word growth may occur in each filter stage, the succeeding stages must grow in word length, or a scaling and truncation regimen is required to maintain constant word size in all stages.

This all-zero Comb filter, in tandem with single pole recursive filters, can, through pole-zero cancellation, produce selective frequency responses such as low pass, band pass, etc. This is a viable filter design technique and is known as frequency sampling [1]. An outstanding example of this technique is to cascade several Comb filter stages in series with an equal number of single pole integrators (poles are at f=0). The result is a multiplier-free, high order decimating (or interpolating) filter [2].

1. L. R. Rabiner and B. Gold, *"Theory and Application of Digital Signal Processing."* Prentice-Hall, 1975, pp. 48-50.
2. E. B. Hogenauer, *"An Economical Class of Digital Filters for Decimation and Interpolation."* IEEE Trans. On Acoustics, Speech, and Signal Processing, Vol. ASSP-29, April 1981, pp. 155-162.

Pinout

Signal names for the schematic symbol are shown in Figure 1 and described in Table 1.

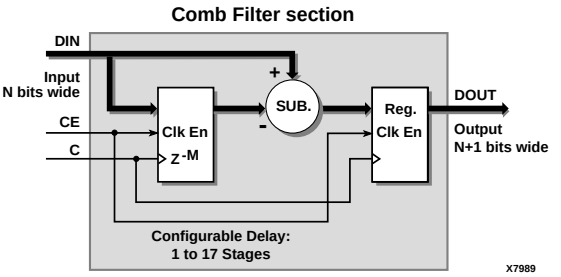

Figure 1. Block Symbol and Schematic Diagram

Table 1. Core Signal Pinout

Signal	Signal Direction	Description
DIN	Input	Serial Data In – for correlation
CE	Input	Clock Enable – active high
C	Input	Clock – data is clocked into the delay element on the rising edge
DOUT	Output	Comb filter output

CORE Generator Parameters

The CORE Generator accepts the parameters entered through the dialog box and creates the specific design from the values entered using a parameterized VHDL recipe. VHDL instantiation code and a schematic symbol are created along with the netlist for the design.

The CORE Generator dialog box for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name:** Enter a name for the component.
- **Data Width:** Select an input filter width from the pull-down menu. The valid range is 2-31.
- **Delay Length:** Select the number of delay stages from the pull-down menu. The valid range is 1-17.

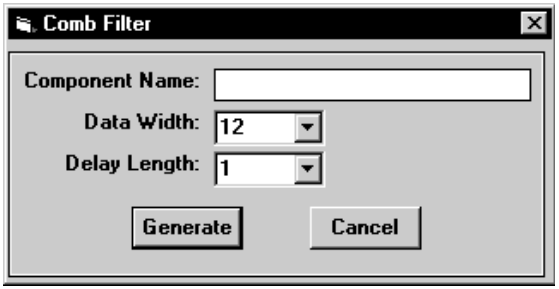

Figure 2. CORE Generator Dialog Box

Core Resource Utilization

The following equations show the number of CLBs used in the XC4000 family based on the input data width.

Number of CLBs where N = Input Data Width:

Even N:

CLBs = N + 1 If delay = 1 or 2
CLBs = N + 2 If delay = 3, 4, or 5
CLBs = N + 4 If delay = 6 or more

Odd N:

CLBs = N + 2 If delay = 1 or 2
CLBs = N + 4 If delay = 3, 4, or 5
CLBs = N + 6 If delay = 6 or more

Ordering Information

This macro comes standard with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to dsp@xilinx.com.