Parallel Multipliers – Area Optimized

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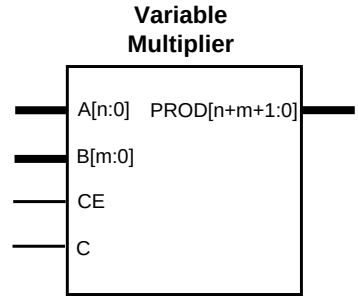

Figure 1: Core Schematic Symbol

Features

- Parallel Multipliers with parameterizable data widths
- Area optimized design
- Independently adjustable input variable widths from 6 to 32 bits
- Full precision outputs
- Two's complement signed and unsigned data formats
- Registered inputs and outputs
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Pipelined design for increased throughput
- Clock Enable - freezes internal pipeline operation
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This parameterized module is a high-speed parallel implementation that multiplies an N-bit wide variable by an M-bit variable and produces an N+M bit result.

An area-efficient, high-speed algorithm is used to give an efficient, tightly packed design. Each stage is pipelined for maximum performance.

A clock-enable is available with which each internal pipelined stage may be halted. Partially completed results are stored internally when CE is taken Low, and the multiplier resumes normal operation when CE returns High.

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A[n:0]	Input	PARALLEL DATA IN - A operand.
B[m:0]	Input	PARALLEL DATA IN - B operand.
C	Input	CLOCK - with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
CE	Input	CLOCK ENABLE - when active high, allows data to propagate between internal pipeline stages. When inactive all activity within the module ceases.
PROD[m+n+1:0]	Output	PARALLEL DATA OUT - product.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **A Width**: Select an input bit width from the pull-down menu for the input A. The valid range is 6 to 32.
- **B Width:** Select an input bit width from the pull-down

menu for the input B. The valid range is 6 to 32.

- **Signed:** Representation for both input variables.

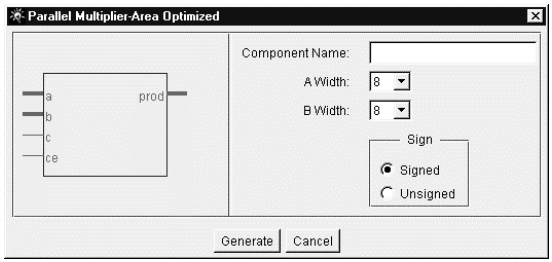

Figure 2: Parameterization Window

Multiplier Latency

Data is buffered on the input and output of the multiplier cores. The total latency (number of clocks required to get the first output) is a function of the width of the **B** variable only.

Table 2: Multiplier Latency

B Data Width	Latency (# Clocks)
6 to 8 bits	4
9 to 16 bits	5
17 to 32 bits	6

Core Resource Utilization

Table 3 shows the resource utilization for sample bit widths.

All the variable multipliers are built to fit in a rectangular or square matrix of N rows by M (or M-1) columns.

Multiplier Trade-offs

Two different implementations of parallel multipliers trade area for speed. The area efficient designs consume about one-fourth less CLB resources than the high speed designs in the 4000E family.

The additional routing resources in the 4000EX and 4000XL families will increase the performance for the area efficient designs. In addition, both structures will benefit from the overall performance increase derived from the 4000XL .35 micron process technology. For the 8x8, 12x2, and 16x16 multipliers compare Figure 3 versus Table 3 to see the performance gained with the 4000XL technology.

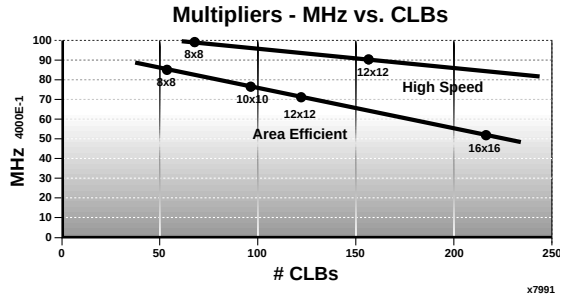

Figure 3: Trade-offs of Area Versus Speed Optimization for Multipliers

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Table 3: Parallel Multiplier - Area Optimized Characterization Data

A Width	B Width	CLB Count	Area Required for RPM² (Rows, Columns)	4000XL-08 (Advanced) MHz	4000XL-09 MHz	4000XL-3 MHz	Spartan -4 (Advanced) MHz
8	8	54	8,7		99	65	88
8	12	94	8,12		92	61	81
8	16	121	9,15		91	60	74
8	24	201	10,24		83	56	
8	30	252	12,30	86	79	52	
12	8	76	12,7		87	57	71
12	12	130	12,12		80	53	69
12	16	167	12,15		78	52	63
12	24	273	12,24		73	48	
12	30	342	14,30	78	70	46	
16	8	98	16,7		76	50	62
16	12	166	16,12		71	47	61
16	16	213	16,15		70	46	56
16	24	345	16,24		67	44	
16	30	432	16,30	70	63	41	
24	8	142	24,7		62	40	
24	12	238	24,12		60	39	
24	16	305	24,15		57	37	
24	24	489	24,24		55	36	
24	30	612	24,30	60	54	35	
30	8	175	30,7	59	54	35	
30	12	292	30,12	58	53	34	
30	16	374	30,15	55	50	33	
30	24	597	30,24	53	48	31	
30	30	747	30,30	50	46	29	

Notes: 1. To achieve the performance documented in this table, it may be necessary to specify a TIMESPEC (timing specification) PERIOD constraint appropriate to meet the documented frequency.
2. The RPM dimensions shown provide guidance for selecting a device with the approprirate CLB array size.

Parameter File Information

Component Name	Type	Notes
Component_Name	String	
A_Width	Integer	6 - 32
B_Width	Integer	6 - 32
Signed	Boolean	True/False