M8237 DMA Controller

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Features

- Multimode Direct Memory Access (DMA) controller
- Functionally compatible to Intel 8237
- Four independent DMA channels
- Independent auto-initialization of all channels
- Directly expandable to any number of channels
- Memory-to-memory transfers
- Memory block initialization
- Enable/disable control of individual DMA requests
- Address increment/decrement selection control for all channels
- High performance transfers up to 1.6 MBytes/second with 5 MHz
- End of process input to terminate transfers
- Software DMA request
- Programmable polarity control for DMA Request and DACK signals

Applications

- Multi-mode Programmable, multi-channel DMA
- Support Controller for Microprocessor based systems

AllianceCORE™ Facts

Core Specifics	
Device Family	XC4000E
CLBs Used	392
IOBs Used	37[1]
CLKIOBS used	1
System Clock fmax	8 MHz
Device Features Used	Global buffers

Supported Devices/Resources Remaining		
	I/O	**CLBs**
XC4036EX HQ240-4	156[1]	904

Provided with Core	
Documentation	Core Design Document Designer's Application Note
Design File Formats	.ngd, XNF netlist Verilog Source RTL (available extra)
Constraint Files	.cst file, xactinit.dat
Verification Tool	Test Vectors
Schematic Symbols	None
Evaluation Model	None
Reference designs & application notes	FPGA Design Document included
Additional Items	None

Design Tool Requirements	
Xilinx Core Tools	Alliance 1.3
Entry/Verification Tool	Verilog RTL/Verilog XL Simulator

Support
Support provided by Virtual IP Group, Inc.

Note:
1. Assuming all core signals are routed off-chip.

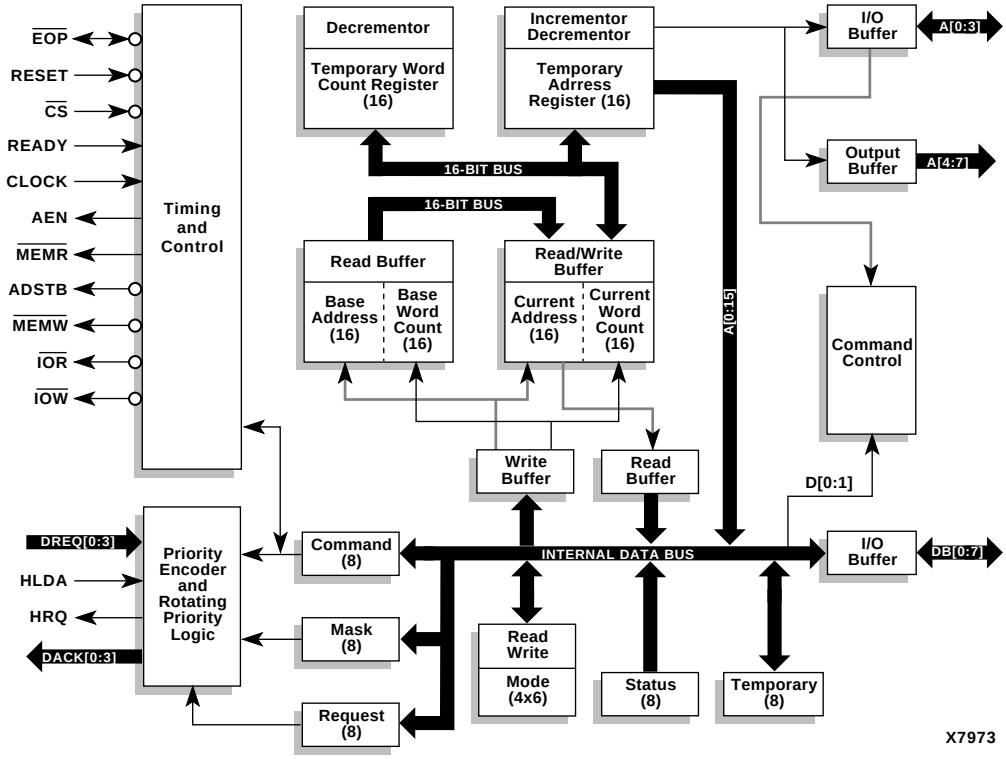

Figure 1: M8237 DMA Controller Block Diagram

General Description

The M8237 core is a 4 channel programmable DMA controller that can be interfaced with a standard microprocessor. All four DMA channel operations are independently programmable by the microprocessor during initialization. The core is functionally compatible with the standard 8237 chip.

Functional Description

The M8237 DMA Controller core is partitioned into modules as shown in Figure 1 and described below.

Timing Control Block

The Timing Control block generates internal timing and external control signals for the M8237. It also generates DMA bus cycle timing based on internal state cycles using the clock.

Program Command Control Block

The Program Command Control block decodes commands given to the M8237 by the microprocessor prior to servicing a DMA request. It also decodes the Mode Control word used to select the type of DMA service.

Priority Encoder Block

The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

Register Block

The M8237 contains 344 bits of internal memory in the form of registers. Table 2 lists these registers and shows size of each.The registers are independently addressable and are separate for each DMA channel except a few which are common.

Core Modifications

Multiple cores can be integrated to provide additional channels. Modifications can be done to reduce number of channels.These modifications are performed by Virtual IP Group, Inc. for additional cost.

Pinout

The pinout has not been fixed to specific FPGA I/O flexibility with the user application. A pinout is suggested for use with a user constructible evaluation board for this is in the FPGA Design Document included with the core. Signal names are

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Timing and Control Signals		
/EOP	Input	End Of Process input to stop DMA service; active low.
RESET	Input	Reset: clears command mode, status, request, temporary registers and first/last flip flop; sets mask register; active high.
/CS	Input	Chip Select to select M8237 as an I/O allowing CPU to communicate on the data bus; active low.
READY	Input	Ready, used to extend memory read and write pulses from M8237 to accommodate slower memories or I/O peripheral devices.
CLOCK	Input	Clock input.
AEN	Output	Address Enable signal used to disable other system bus drivers during DMA cycle; active high.
/MEMR	Output	Memory Read output from selected memory during a DMA read transfer or for memory to memory read cycle; active low tristate.
ADSTB	Output	Address Strobe, strobes up Upper address nibble; per address byte into an external latch during DMA cycle; active high.
/MEMW	Output	Memory Write output to write data on selected memory during DMA write transfer or for memory to memory write cycle; active low tristate.
/IOR	Input	I/O Read input control line used by CPU to read registers; active low.
/IOW	Input	I/O Write input control line used by CPU to write to registers; active low.
Priority Logic Signals		
DREQ[0:3]	Input	DMA Request [0:3], individual asynchronous channel request lines used by peripheral devices to obtain service. Programmable polarity; DREQ must be maintained until corresponding DACK line goes active.
HLDA	Input	Hold Acknowledge, tells M8237 that CPU has relinquished control of system bus, active high.
HRQ	Output	Hold Request given to CPU to request control of system bus.
DACK[0:3]	Output	DMA Acknowledge, notifies Address Enable signal used peripherals when DMA cycle is granted. Polarities are programmable.
Address/Data Signals		
A[0:3]	In/Out	Lower address nibble used by CPU to address registers for reading or writing; M8237 outputs lower 4 bits of output address during DMA service.
A[4:7]	Output	Upper address nibble; M8237 outputs upper 4 bits of output address during DMA service.
DB[0:7]	In/Out	Data bus used by CPU to write to and read from internal registers and to read memory to memory read cycle data. During DMA service 8 most significant address bits are output and strobed into an external latch by ADSTB.

Table 2: Internal Registers

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

provided in the block diagram shown in Figure 1 and described in Table 1.

Verification Methods

The core has been tested in house developed test vectors that are provided with the core.

Recommended Design Experience

Knowledge of DMA interfaces in a microprocessor based systems is required. The user must be familiar with HDL design methodology, instantiation of Xilinx netlists in a hierarchical design environment and usage of Xilinx development tools.

Available Support Products

FPGA Evaluation Board

The FPGA Design Document included with the core gives directions for constructing a general purpose FPGA evaluation daughter board that can be plugged into a standard part socket on the target system through a flat cable.

Ordering Information

This product is available from Virtual IP Group, Inc. Please contact them for pricing and additional information.

Related Information

Refer to Specification Document for programming of this core for a typical system application. The user should refer to the Designer's Application Note for integrating this with other cores. Both documents are included with the core.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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