The Reed-Solomon Solution - Customer Tutorial

Xilinx at Work in Hot New Technologies
February 2000

Agenda

- Introduction
- Reed-Solomon Overview
- Reed-Solomon Applications
- Spartan-II IP Solutions for Reed-Solomon
- Summary

Introduction

- Spartan-II FPGAs
  - 100,000 system gates at under $10
  - Extensive features: Block RAM, DLL, Select I/O
  - Vast IP portfolio
  - **Provide Density, Features, Performance at ASIC prices**

A Spartan-II FPGA Based Programmable Reed-Solomon Solution Competes Effectively Against Stand-Alone ASSPs

Reed-Solomon Concept, Terminology, Architecture and Features

Noise Happens

- Data Transmission and Storage are Fundamental Functions in most Electronic Systems
- In an Ideal Communication Medium
  - Errors do not come into play during transmission
- In the Real World
  - Noise causes data corruption
  - Error-correcting coding systems are required

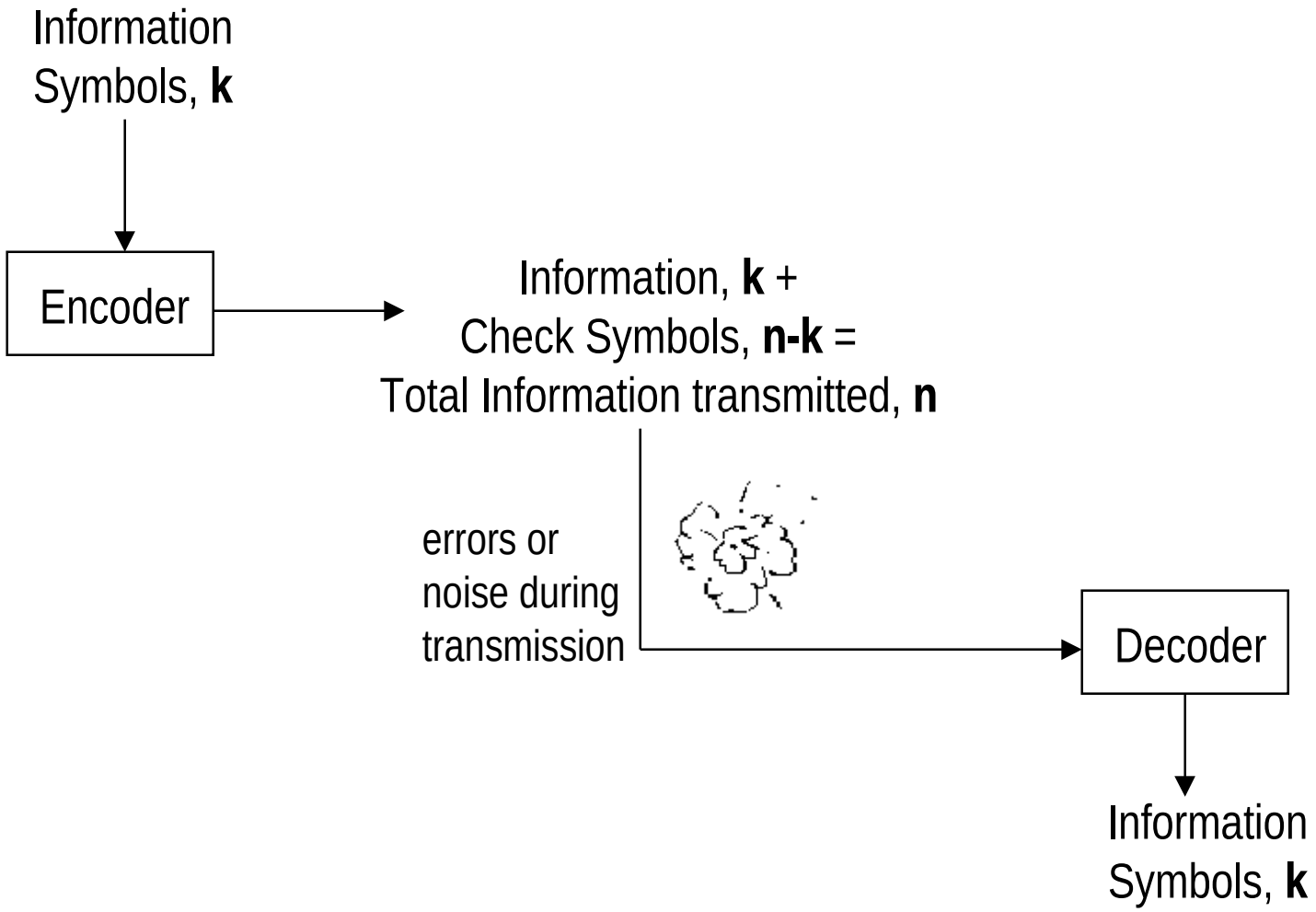
Error Control Coding

- Forward Error Correction (FEC)
  - Redundancy is added before transmission/storage
  - Any errors introduced are detected and corrected
- Convolution Codes - Viterbi
  - This procedure is used to correct random errors
- Block Codes - Reed-Solomon
  - Data processing occurs one block at a time
  - This procedure is used to correct burst errors

Reed-Solomon - Concept

- Reed-Solomon
  - An error-correcting coding system that corrects multiple errors, especially burst-type errors in communication systems
  - Transmitter
    - Data is encoded to be corrected in an event it acquires errors
  - Receiver
    - Uses the appended encoded bits to determine errors
    - Corrects the errors upon reception of the transmitted signal

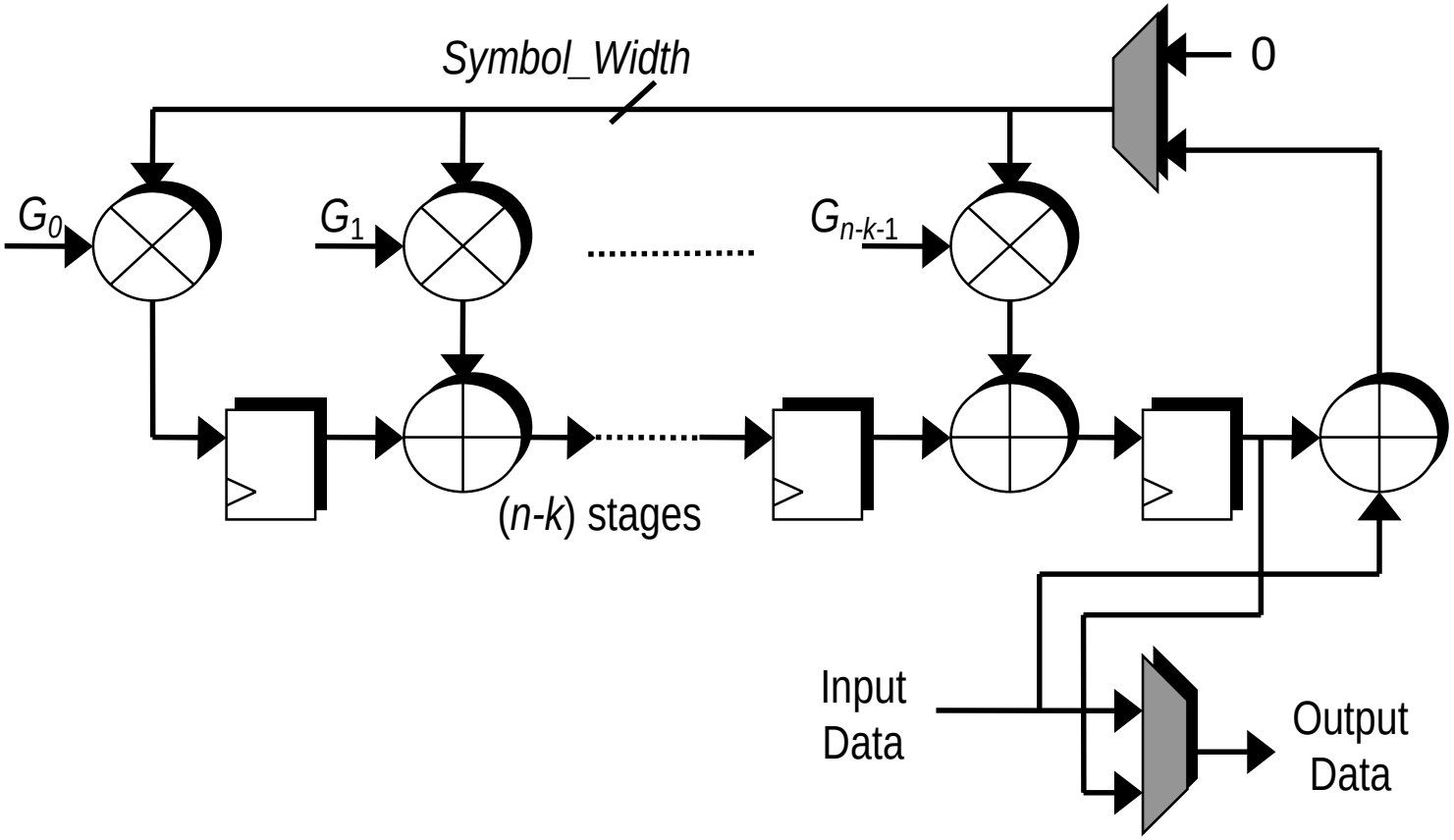
Reed-Solomon Encoder/Decoder



Reed-Solomon - Terminology

- *Symbol_Width* = Number of Bits per Symbol
- *Code word* = the Block of *n* Symbols
- RS(*n*, *k*) code
  - *n* = Total Number of Symbols per Code Word
  - *k* = Number of Information Symbols per Code Word
- *Code Rate* = *k* / *n*
- Shortened Codes - Code Word $< 2^{Symbol\_Width} - 1$
- *r* = (*n* - *k*) = Number of Check Symbols
- *t* = (*n* - *k*) / 2 = Maximum Number of Symbols with Correctable Errors

Encoder Architecture

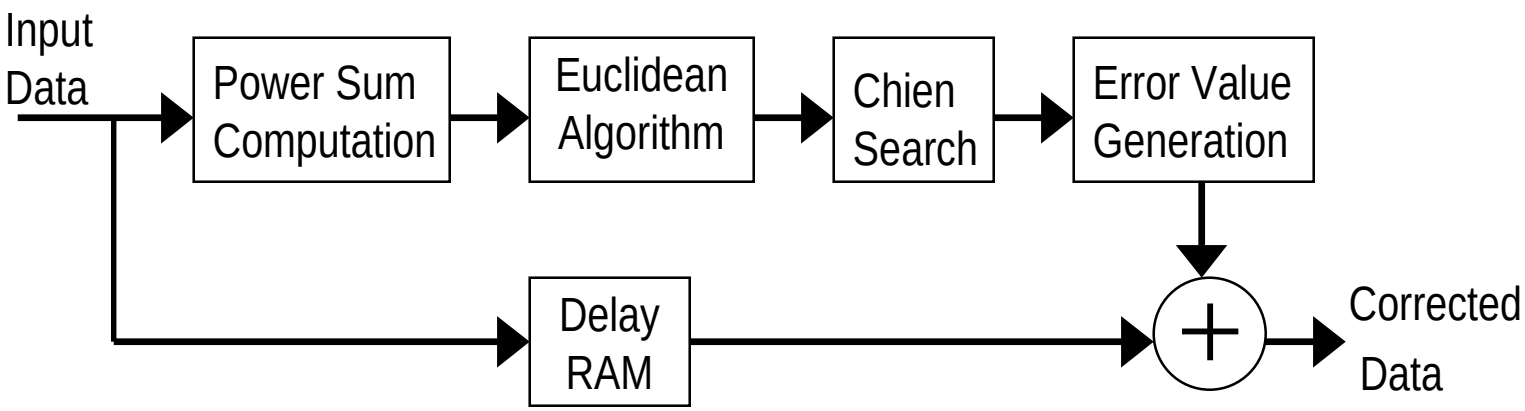


Block Diagram of the Reed-Solomon Encoder

Encoder Features

- Fully Synchronous, Bit-Parallel Systematic Encoder
- Supports Several Standards and is Customizable (“roll-your-own”)
  - Bits per symbol ($3 \leq Symbol\_Width \leq 12$)
  - Symbols per code word ($n \leq 4095$)
  - Check symbols per code word ($n\text{-}k \leq 256$)
  - Field polynomial
  - Generator polynomial (*Generator_Start* & *h*)
- Spartan-II Product Family
  - RPM mapping and placement technology has been optimized
  - Allows web-based configuration and downloading

Decoder Architecture



Block Diagram of the Reed-Solomon Decoder

Decoder Features

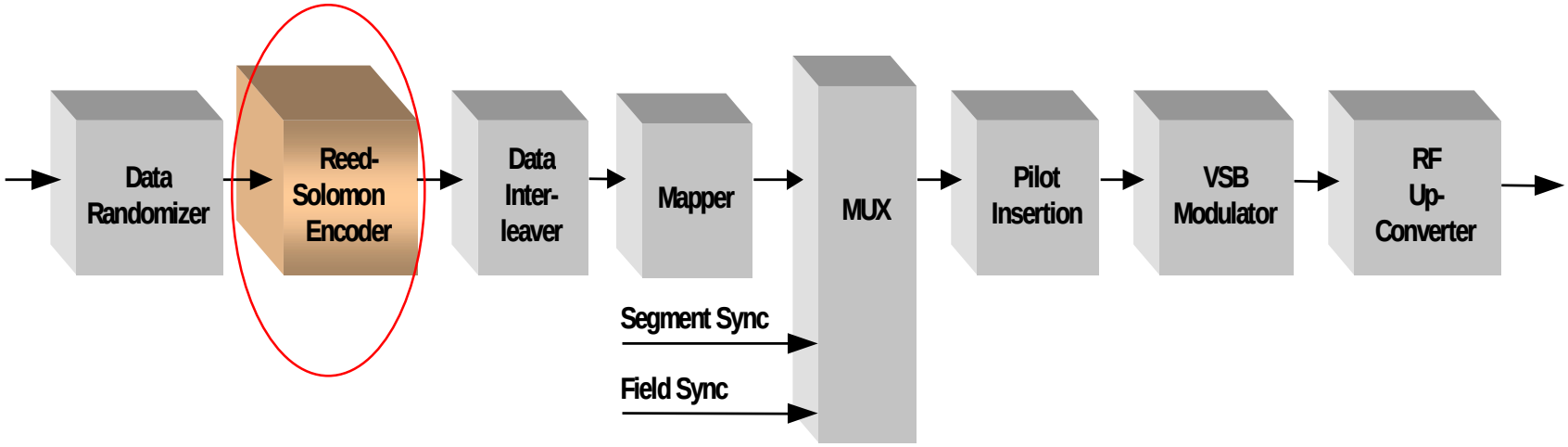
- Fully Synchronous, Bit-Parallel Decoder
- Parameterizable:
  - Symbol width (3 to 12 bits)
  - Symbols per code word (≤ 4095)
  - Check symbols per code word (≤ 128)
  - Field polynomial
  - Generator polynomial
- Supports Discrete or Continuous Input Data
- Supports Erasure Decoding
- Spartan-II Product Family
  - RPM mapping and placement technology has been optimized

Reed-Solomon Applications

Reed-Solomon Applications

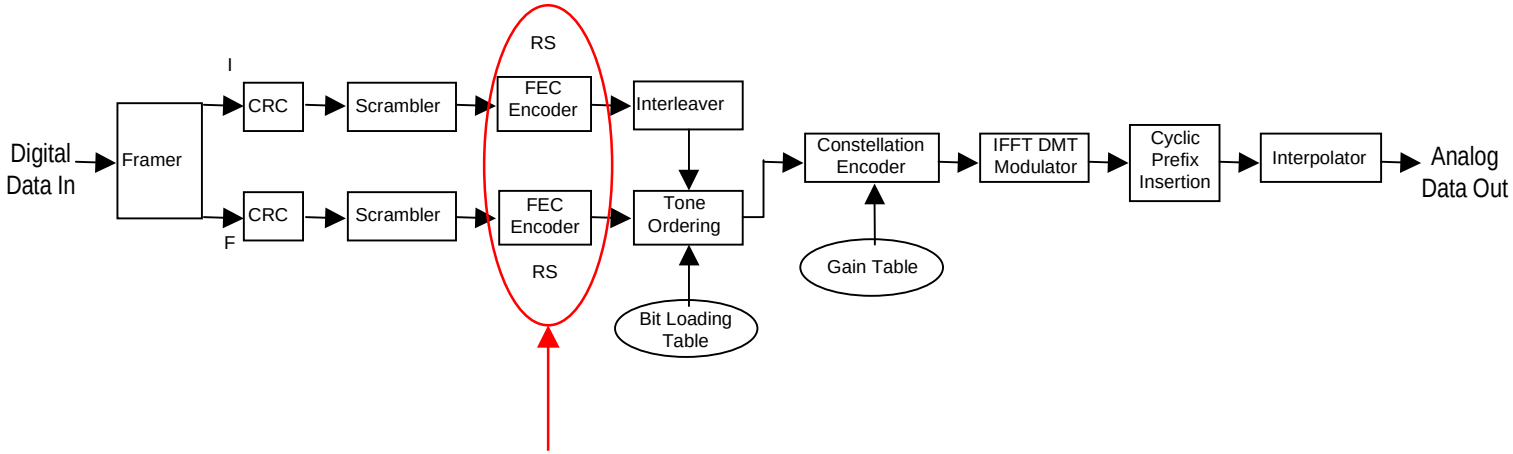
- Modem Technologies
  - xDSL, Cable modems
- CD, DVD Players
- Digital Audio and Video Broadcast
- HDTV/Digital TV
- Data Storage and Retrieval Systems
  - Hard-Disk Drives, CD-ROM
- Wireless Communications
  - Cell Phones, Base Stations
- Wireless Enabled PDAs
- Digital Satellite Communication and Broadcast
- RAID Controllers with Fault-Tolerance

Digital TV



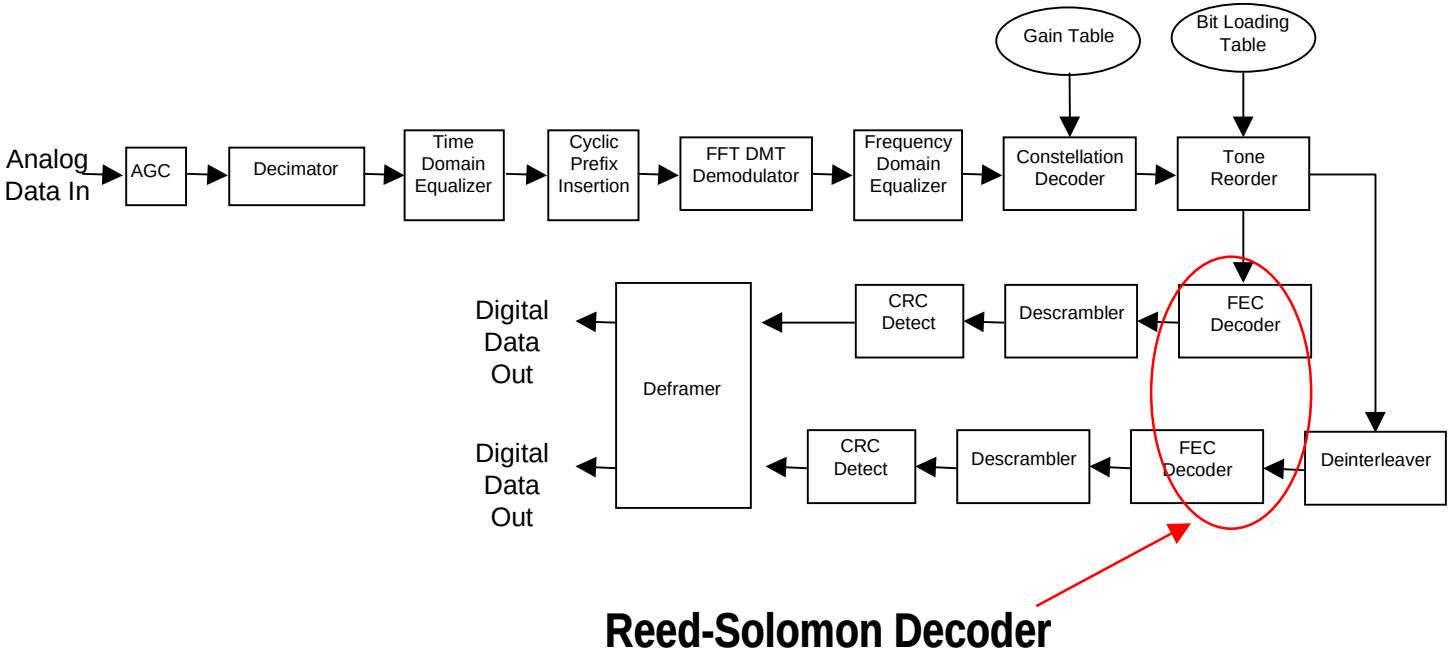
- The Digital Television Reed-Solomon Encoder
  - Implements encoding for error correction of symbol streams with Reed-Solomon block error correction codes
  - Uses Digital Video Broadcasting (DVB) standard for Satellite, Terrestrial and Cable

Transmitter of an ADSL Modem



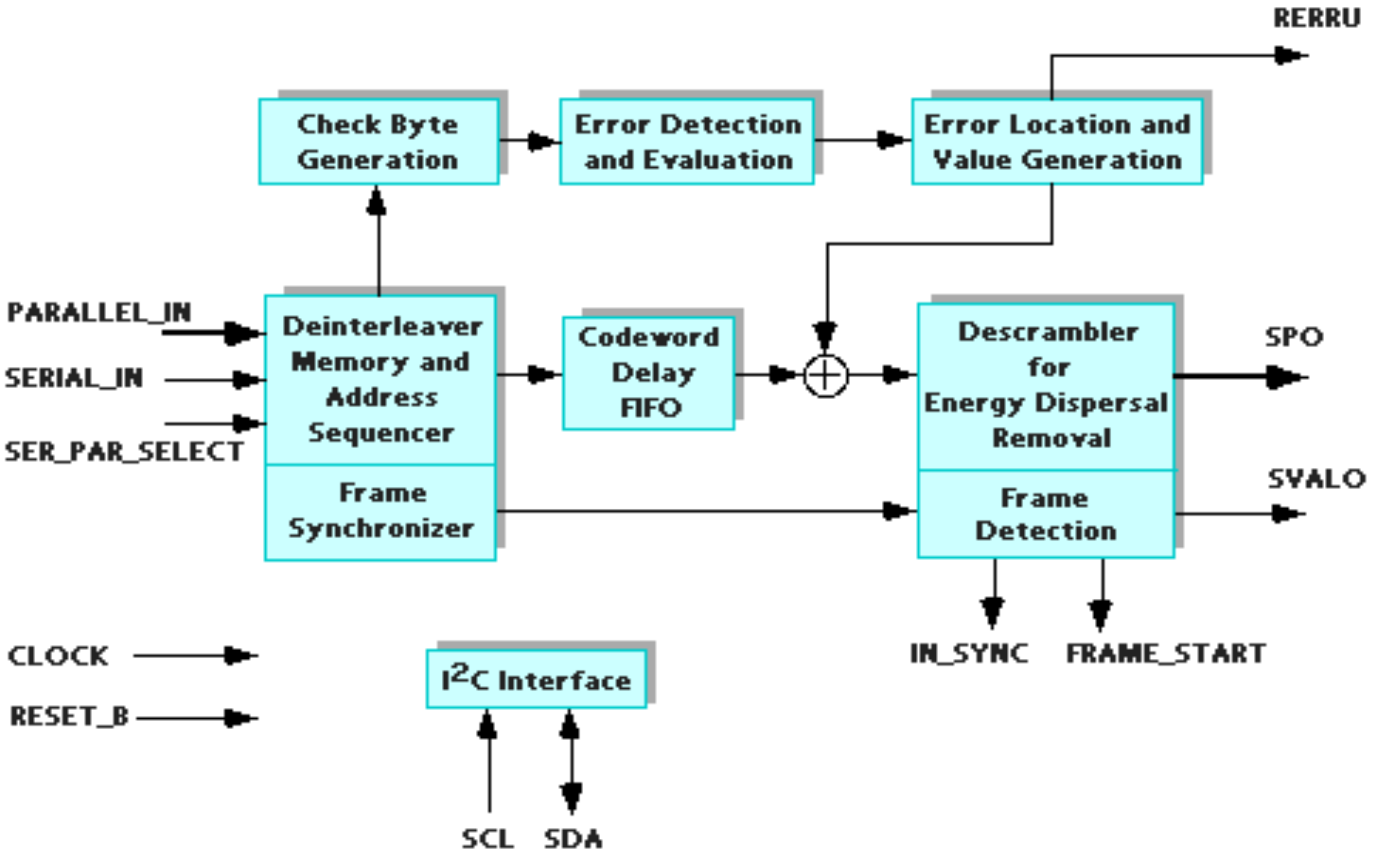
- The ADSL Modem
  - Transmitter employs the Reed-Solomon Encoder
  - Receiver employs the Reed-Solomon Decoder

Receiver of an ADSL Modem



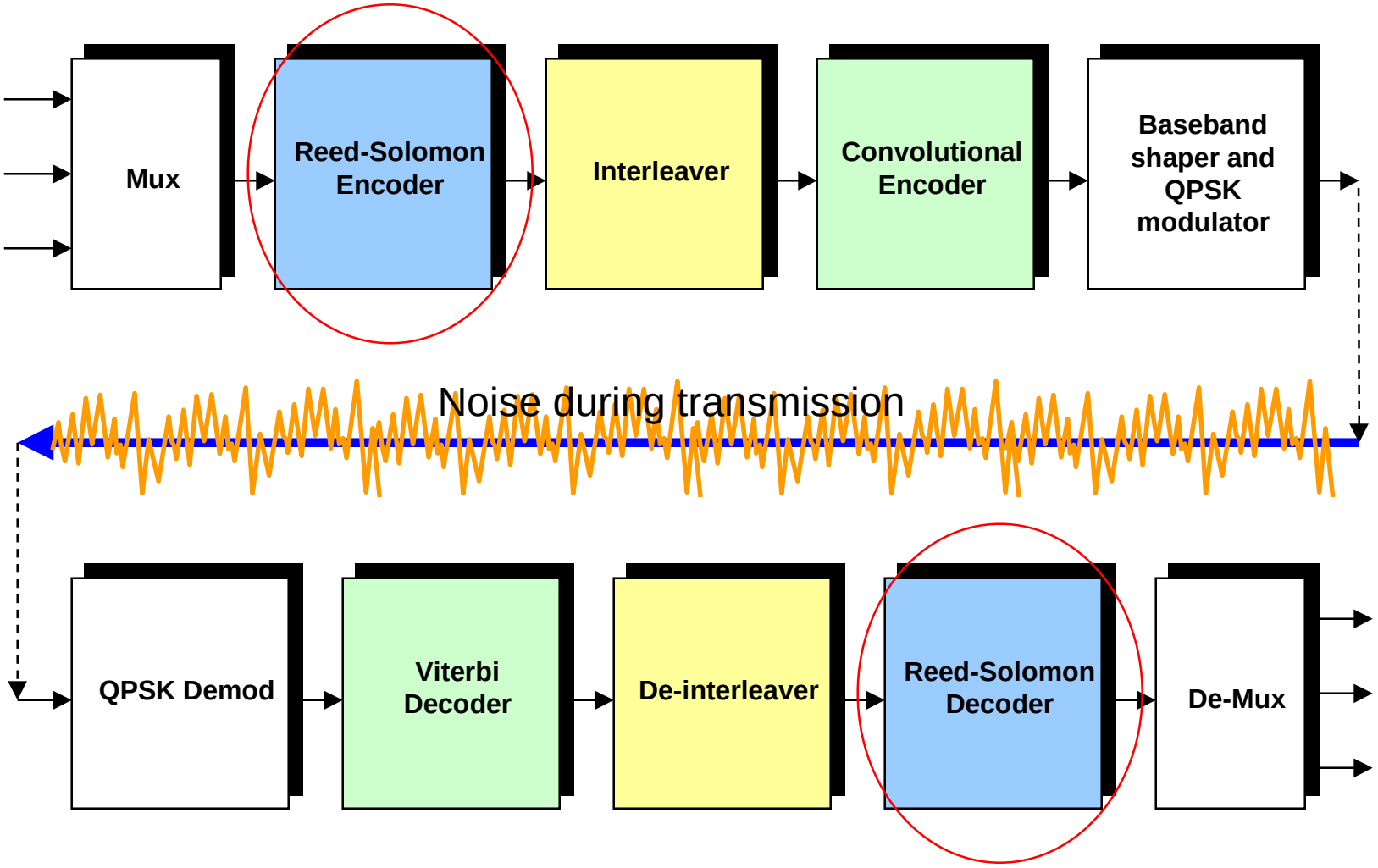
- The ADSL Modem Reed-Solomon Encoder and Decoder
  - Performs Forward Error Correcting (FEC) code to mitigate effects of bit error bursts in receive bit stream
  - Increases the ADSL system's reliability

Reed-Solomon Decoder for Digital TV



Satellite and Cable Set-Top System - Block Diagram (courtesy Motorola, Inc.)

Digital Video Broadcast (DVB) - Satellite



Spartan-II Reed-Solomon IP Solutions

Spartan-II + Reed-Solomon IP = Programmable Reed-Solomon Solution

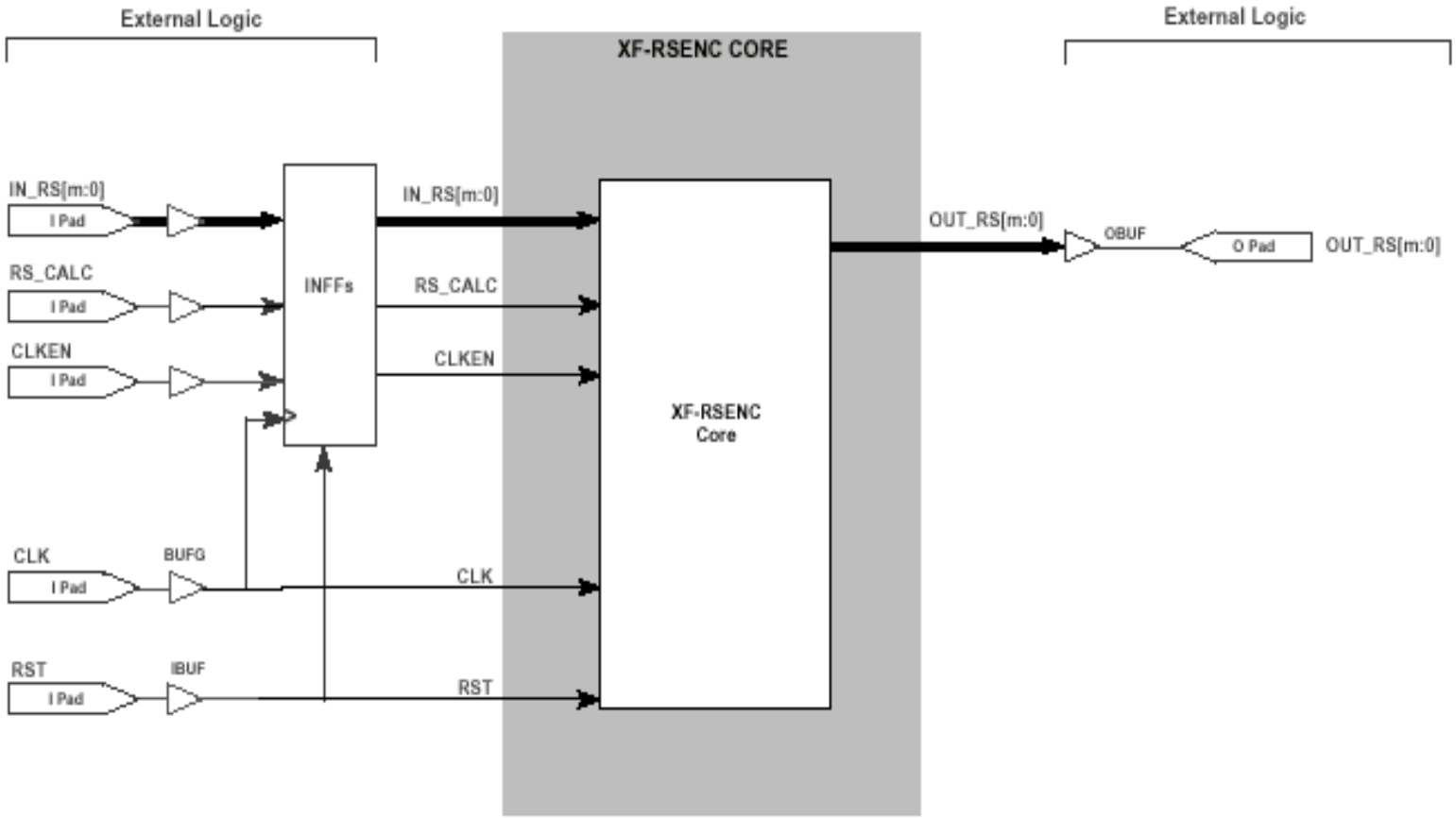
- Xilinx Reed-Solomon is Provided Through LogiCORE Program by
  - Integrated Silicon Systems, Ltd.
    - Reed-Solomon Encoder core
    - Reed-Solomon Decoder core

Xilinx Reed-Solomon

- Reed-Solomon Solutions are also Provided by the Following AllianceCORE Partner
  - Memec Design Services
    - XF-RSENC Reed-Solomon core - Encoder
    - XF-RSDEC Reed-Solomon core - Decoder

Memec Design Services

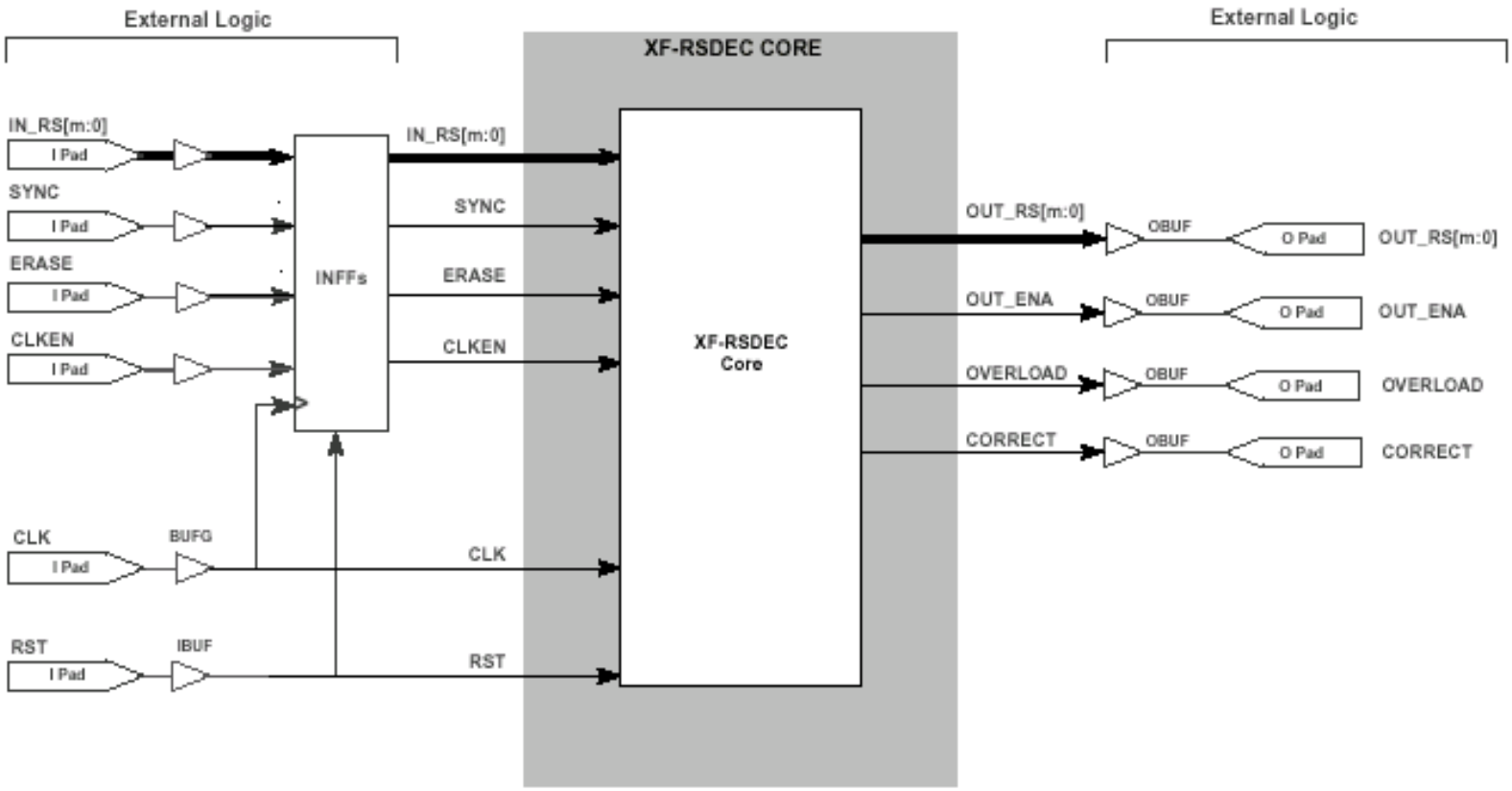
Xilinx Reed-Solomon



XF-RSENC Core with External Logic - Reed-Solomon Encoder

Memec Design Services

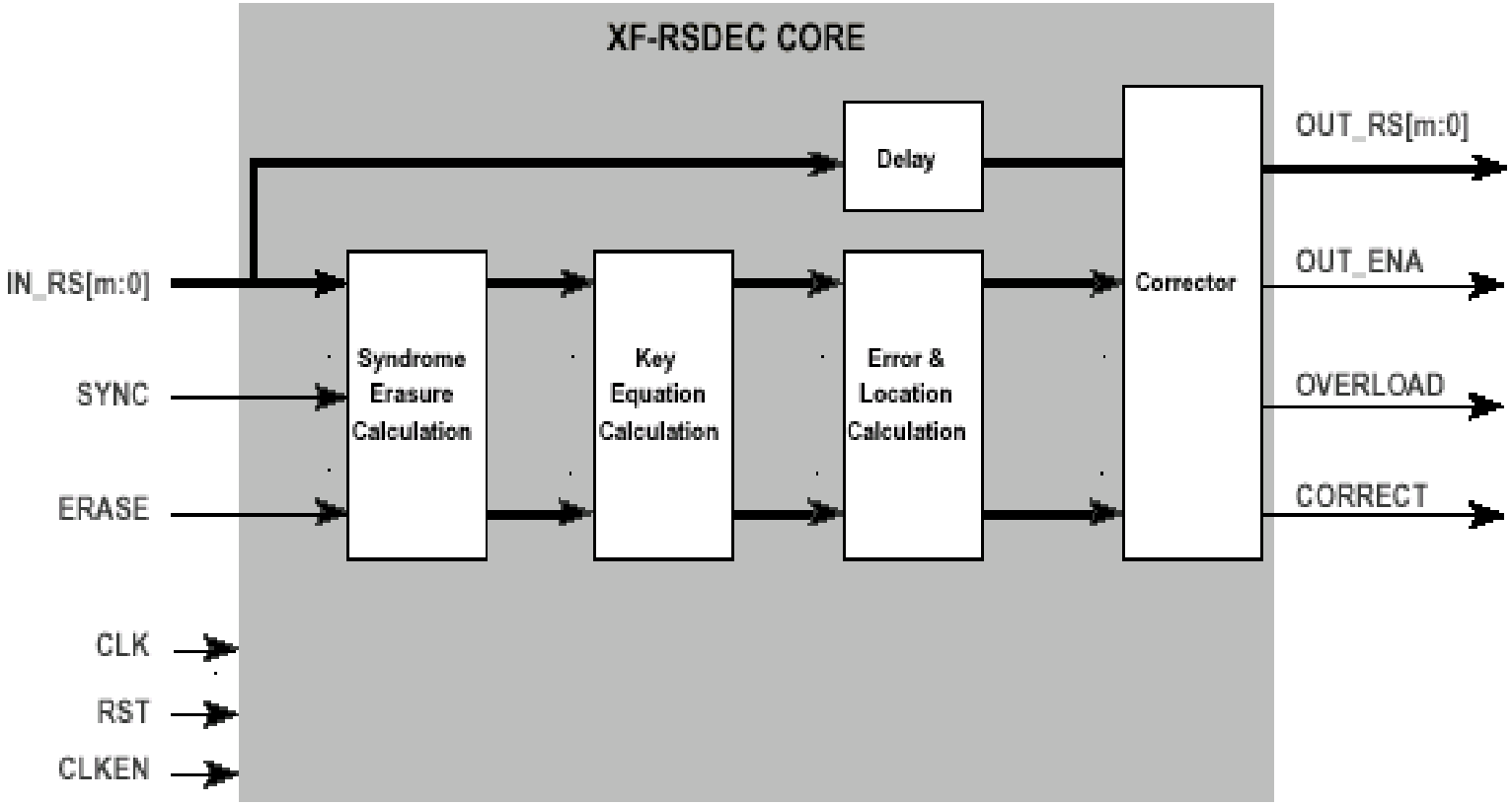
Xilinx Reed-Solomon



XF-RSDEC Core with External Logic - Reed-Solomon Decoder

Memec Design Services

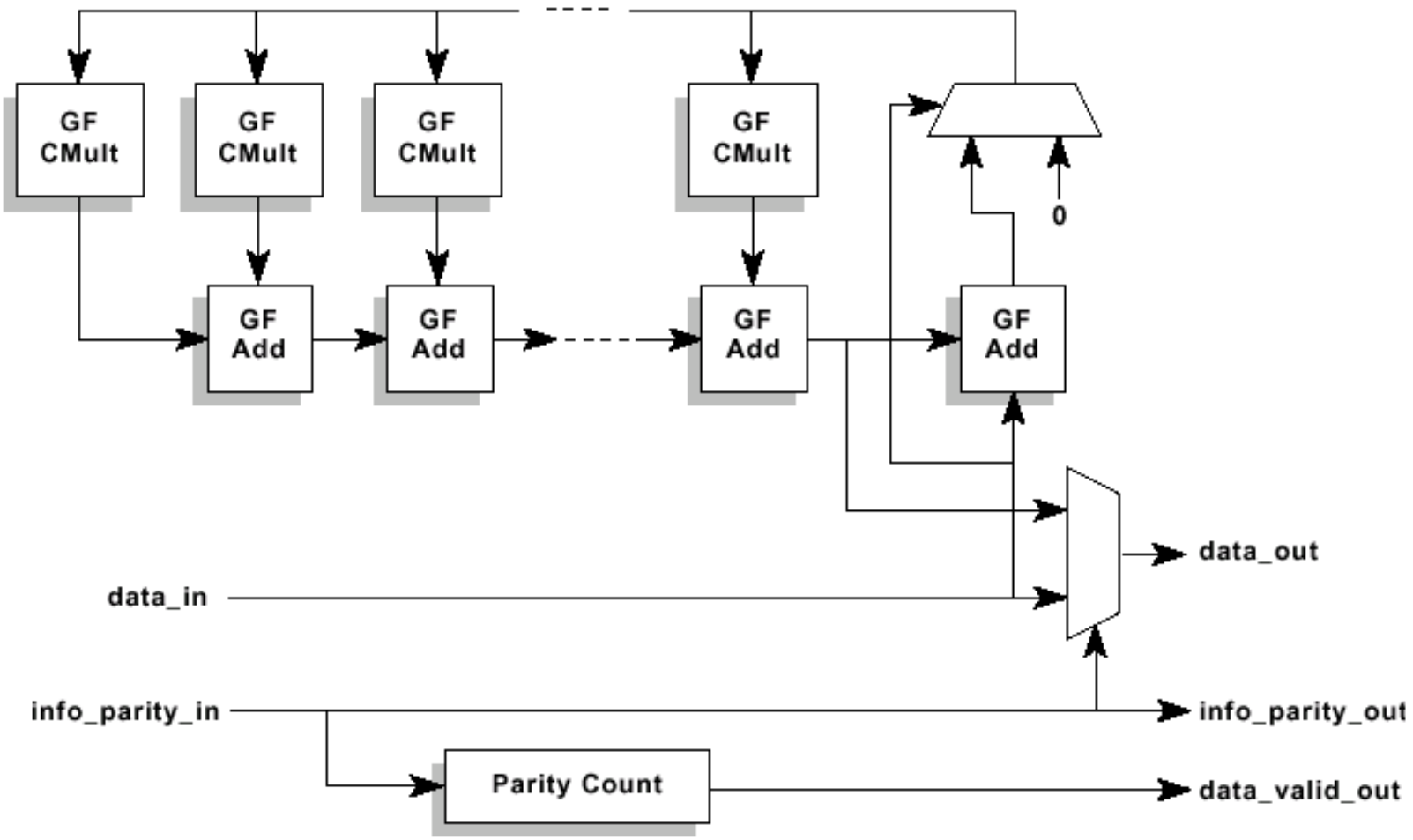
Xilinx Reed-Solomon



XF-RSDEC Core - Reed-Solomon Decoder Block Diagram

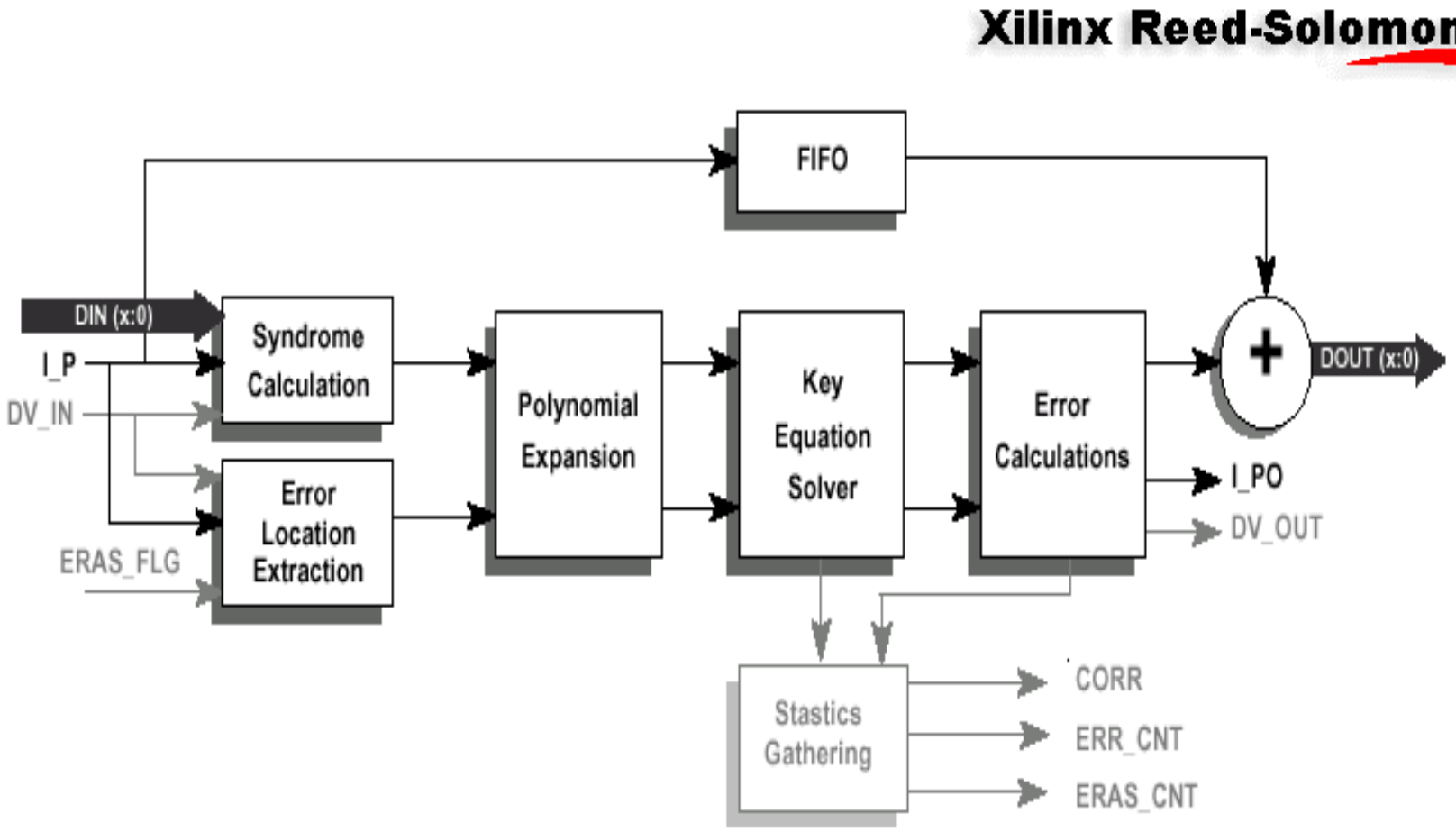
Integrated Silicon Systems

Xilinx Reed-Solomon



Reed-Solomon Encoder Block Diagram

Integrated Silicon Systems



Reed-Solomon Decoder Block Diagram

Spartan-II Reed-Solomon IP Solutions

Xilinx Reed-Solomon

- Encoder and Decoder Cores
  - Available Separately
- Web-Based Configuration and Download
  - Supports many Reed-Solomon coding standards and “roll-your-own”
  - Receive customized core in minutes (via email)
  - Generate unlimited number of cores (site licensing)
- Both Cores can be considered as Black Boxes
- RPM Technology
  - Used for predictable performance and fast implementation times
- The Xilinx Decoder Core is Half the Size of Altera’s Offering
- Automatically Configured from User Parameters
  - Supports all major coding standards and custom implementations
- Can be Optimized for Area or Speed
- Incorporates Xilinx Smart-IP Technology for Design Predictability

Xilinx Smart-IP Technology

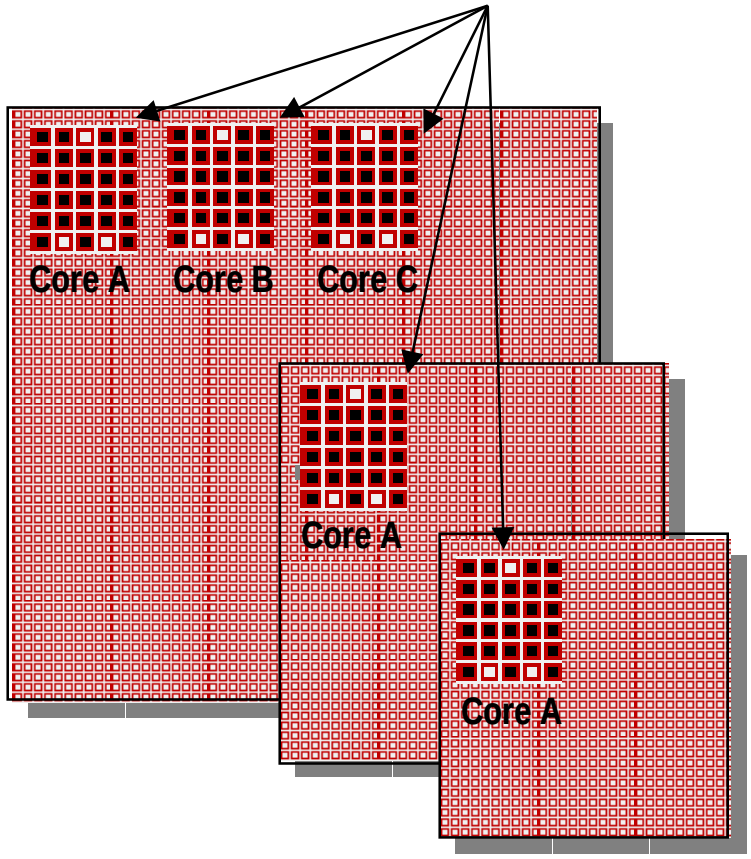
Features

- FPGA Architecture tailored to cores
  - Segmented routing
  - Distributed & block memory
- Pre-defined core placement & routing

Customer Benefits

- Performance independent of:
  - Core placement
  - Number of cores used
  - Surrounding user logic
  - Device size
  - EDA tools

Consistent performance



Reed-Solomon ASSPs

- The Reed-Solomon Spartan-II Solution Competes Against ASSPs Successfully
- Some of These ASSPs are:
  - Motorola Semiconductor
  - Conexant Systems, Inc.
  - LSI Logic, Inc.
  - Broadcom Corporation
  - AHA

The Spartan-II Competitive Advantage

Features	Typical Reed-Solomon ASSPs	Reed-Solomon in Spartan-II
Polynomial	Fixed	Parameterizable
Symbol Width	Fixed	Parameterizable
Block Length	Programmable (3 - 255)	Parameterizable (3 - 4095)
Correctable Errors	Programmable (1 - 10)	Parameterizable (1 - 64)
Erasure Handling	Fixed	Parameterizable
Maximum Throughput	12.5 Mbytes/sec	Decoder: 62 Mbytes/sec Encoder: 108 Mbytes/sec
Latency	1181 cycles	418 cycles
Cost (in 250k units)	$20	9.95*

* With Reed-Solomon configuration comparable to listed Typical ASSP example. The price is based on 250KU resale price for XC2S100

- The Reed-Solomon Spartan-II Solution is Priced below ASSP Prices
  - Encoder and Decoder Solution = $9.95
  - Encoder Solution = $3.95

The Spartan-II Solution has a Clear Competitive Advantage over Stand-Alone ASSPs

Programmable ASSP - Value

- Benefits
  - Time to Market
  - Flexibility
    - Product Customization to meet customer needs
    - Adapt to Specification Updates
    - Feature Upgrades
    - Low risk evaluation of new market segments
  - Field Upgradability
    - Hardware and Software upgradability opens new applications
  - Efficiently Address Lower Volume Strategic Applications
  - Distribution and Inventory Management

Spartan-II + Soft IP = Programmable ASSP

Programmable ASSP Advantages

- Accommodate Specification Changes
  - Multiple standards and specification changes are accommodated
- Testing and Verification
  - What if the stand-alone ASSP does not perform as expected?
  - Being re-programmable, risk aversion is a tremendous value-add
- Xilinx On-line - Field Upgradability
  - Remote update of Software and Hardware
  - Results in increased lifetime for a product
  - Enable product features per end-user needs
- Issues in Creating a Stand-Alone ASSP
  - Choosing the right ASSP
  - Product customization
  - Development cost and amortization
  - Spartan-II family has amortized cost by selling to the traditional PLD marketplace

Summary

- Reed-Solomon Solutions are Widely Used in a Range of Data Transmission and Storage Applications for Error Correction
- The Spartan-II Family has Significant Strengths to Penetrate the Programmable Reed-Solomon Marketplace:
  - Features
  - Performance
  - Scalability and Flexibility
  - Cost Effectiveness

A Programmable Reed-Solomon Solution Competes Effectively Against Stand-Alone ASSPs