Soft-Decision Viterbi Decoder

January 10, 2000 Product Specification

CAST

CAST, Inc.

24 White Birch Drive
Pomona, New York 10907 USA
Phone: +1 914-354-4945
Fax: +1 914-354-0325
E-Mail: info@cast-inc.com
URL: www.cast-inc.com

Features

- Supports Spartan™-II, Virtex™, and Virtex™-E devices
- Soft Decision Decoder
- Trace-back method for survivor memory
- Supports BPSK modulation
- The following parameters can be configured to meet your needs:
  - Soft decision word length
  - Constraint length (K)
  - Data rate (by changing the number of ACS cells)
  - The length of the trace-back
  - Coding rate (R), also punctured coding rates available
  - Coding polynomial

Applications

- Wireless telecommunications
  - Digital cellular phones
  - Wireless LANS
  - Satellites, Satellite ground stations
- Consumer electronics
  - CD players
  - HDTVs
  - Set-top Boxes

AllianceCORE™ Facts

Core Specifics	
Supported Family	Virtex
Device Tested	V50-6
CLB Slices	241
Clock IOBs	1
IOBs[1]	9
Performance (MHz)	63
Xilinx Core Tools	M1.5i
Special Features	Block RAMs
Provided with Core	
Documentation	Core documentation
Design File Formats	EDIF Netlist, VHDL RTL available extra
Constraints File	decoder.ucf
Verification	VHDL testbench
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
1076 Compliant VHDL Simulator, Verilog Simulator	
Support	
Support provided by CAST, Inc.	

Note:
1. Assuming all core I/Os are routed off-chip.

Example Implementation in the AllianceCORE Facts table is obtained using the parameters shown in Table 1 below.

Table 1: Example Implementation Parameters

Coding Rate (R)	1/2
Constraint Length (K)	7
Soft-decision Word Length	3
Trace-Back Length	55
Number of ACS Element	4

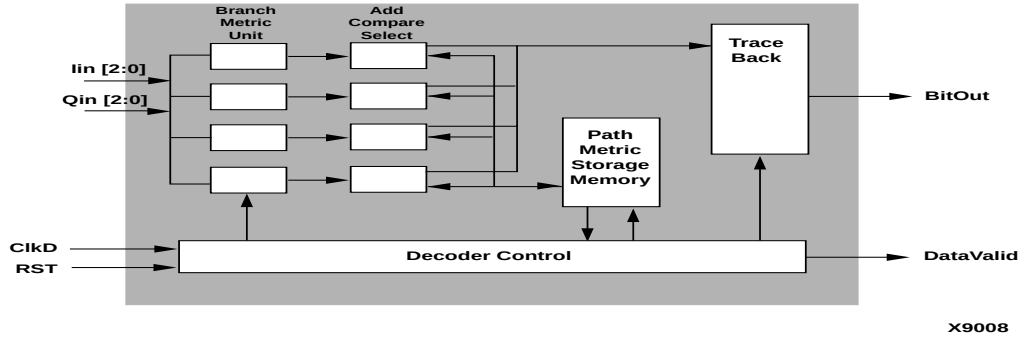

Figure 1: Soft-Decision Viterbi Decoder Block Diagram

General Description

A Viterbi decoder performs a maximum likelihood detection of 1-bit data transmitted over a channel with inter-symbol interference (ISI). The 1-bit data to be transmitted is encoded with an n-bit convolutional code in the convolutional encoder. Figure 2 shows the simplified data path from the Convolutional Encoder to the Viterbi Decoder.

The source code version of the core, available at extra cost, allows for easy adaptation to a wide variety of applications. The Viterbi Decoder netlist can also be delivered with customized parameter settings differing from those in Table 1. (see *Ordering Information*).

Functional Description

The Soft-Decision Viterbi Decoder core is partitioned into modules as shown in figure 1 and described below:

Branch Metric Unit (BMU)

The Branch Metric Unit calculates the Euclidean distance between the incoming data, and the transition in Trellis. This distance is used in ACS to find the minimum path.

Add Compare Select (ACS)

The Add-Compare-Select (ACS) unit calculates path metrics to find the minimum path. The ACS unit has a RADIX-2 architecture.

Path Metric Storage Memory

This consists of memory to store all the old values of the metric path of the soft-decision Viterbi decoder.

Decoder Control

This block contains control logic such as state machines and controls operations such as data loading, enables, and other internal operations of the Soft-Decision Viterbi decoder.

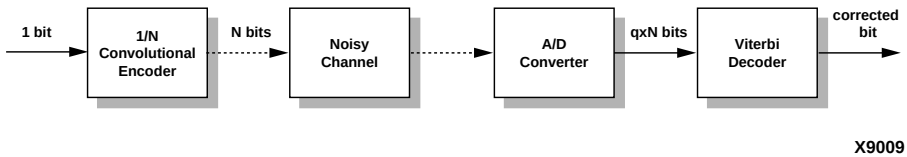

Figure 2: Datapath from Encoder to Decoder

Trace Back

This block stores the new decisions coming from the ACS block and finds the correct path in the memory.

Core Modifications

The Viterbi Decoder core can easily be customized to include:

- Bit error rate (BER) monitor
- Change the modulation type to QPSK
- Microprocessor interface can be added to allow more flexibility
- Burst and continuous data support
- Different number of BMU and ACS units

Please contact CAST directly for any required modifications.

Pinout

The pinout of the Viterbi Decoder core has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1, and described in Table 2.

Verification Methods

The core model has been extensively tested using various settings of the parameters. A special encoder circuit is used as a testbench for full testing of the decoder.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
Iin[2:0]	Input	I input to the decoder
Qin[2:0]	Input	Q input to the decoder
ClkD	Input	Decoder clock
RST	Input	Asynchronous reset, active high
BitOut	Output	Decoded data out
DataValid	Output	Data ready signal

Ordering Information

The Viterbi Decoder is available for purchase directly from CAST, Inc. For the EDIF Netlist format a setting for the parameters has to be submitted before the netlist can be provided. Ask CAST, Inc. for details. The Viterbi core is licensed from Hantro Products Oy.

Related Information

A. B. Carlson, *Communications Systems*, McGraw-Hill, 1986

E. A. Lee, D. G. Messerschmitt, *Digital Comunication*, Boston, MA Kluwer Academic Publishers, 1988

G.D. Forney, Jr., “*The Viterbi Algorithm”*, Proc. IEEE, vol. 61, pp. 268-277, March 1973

G. Fettweis, H. Meyr, “High-Speed Parallel Decoding: Algorithm and VLSI-Architecture”, IEEE Comm. Magazine, pp. 46-55, May 1991

G. Feygin, P.G.Gulak, "Architectural Tradeoffs for Survivor Sequence Memory Management in Viterbi decoders", IEEE Trans. Commun. Tech., vol. 41, no. 3, March 1993

R. Cypher, C.B.Shung, "Generalized Trace-Back techniques for Survivor Memory Management in the Viterbi Algorithm", Journal of VLSI Signal Processing, 5, 85-94 (1993)

Motorola, "*Convolutional Encoding and Viterbi Decoding Using the DSP56001 with a V.32 Modem Trellis Example”*, Motorola Inc. 1989

B. Sklar, "*Digital Communications, Fundamentals and Applications*", Prentice Hall International Inc. 1988

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

Viterbi Implementation Request Form

To: **CAST, Inc.**
FAX: **+1 914-354-0325**
E-mail: **info@cast-inc.com**

From: _____

Company: _____

Name: _____

Address: _____

Country: _____

Phone: _____

Fax: _____

E-mail: _____

CAST, Inc. will customize and deliver a Xilinx optimized netlist for the specific Viterbi Decoder implementation you require. Please fill out and fax or email this information to CAST so they can provide you with an accurate response to, and quote for your requirements.

Implementation Issues

1. Coding rate (R): _____

2. Constraint Length: _____

3. Number of soft input bits: _____

4. Length of trace-back: _____

5. Data rate:_____

6. Coding polynomial: _____

7. Bit error rate (BER) monitor required? _____

8. Modulation type: BPSK or QPSK? _____

Business Issues

9. Indicate timescales of requirement:
   _____ date for decision
   _____ date for placing order
   _____ date of delivery

10. Indicate your area of responsibility:
    _____ decision maker
    _____ budget holder
    _____ recommender

11. Has a budget been allocated for the purchase?
    Yes _____ No _____

12. What volume do you expect to ship of the product that will use this core? _____

13. What major factors will influence your decision?
    _____ cost
    _____ customization
    _____ testing
    _____ implementation size

14. Are you considering any other solutions?