XF9128 Video Terminal Logic Controller

November 9, 1998

Product Specification

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Features

- Compatible with Xilinx CORE Generator tool
- Software & function compatible with industry standard CRT 9128
- Built-in video shift register
- External character generator in configuration ROM
- Bi-directional smooth scroll capability
- Visual attributes include reverse video, intensity control, underline, and character blank
- Separate HSYNC, VSYNC and VIDEO outputs
- Composite Sync (RS170 compatible) output
- Absolute (RAM address) cursor addressing
- Software enabled non-scrolling 25th data row available with 25 data row/page display
- Non-interlaced display format
- Separate display memory bus eliminates contention problems
- Fill (erase) screen capability
- Standard 8-bit microprocessor data bus interface
- Wide graphics with six independently addressable segments per character space
- Thin graphics with four independently addressable segments per character space
- Additional optional video parameters (contact MDS for details and availability):
  - Dots per character block (6-8)
  - Raster scans per data row (6-12)
  - Characters per data row (32, 48, 64, 80)
  - Horizontal blanking (8-64 characters)
  - Horizontal sync front porch (0-7 characters)
  - Horizontal sync duration (1-64 characters)
  - Horizontal sync polarity
  - Two values of vertical blanking
  - Two values of vertical sync duration (1-16 scan lines)
  - Vertical sync polarity
  - External 128-character 5x8-dot font
  - Character/cursor underline position
  - Scan row and column for thin graphics entity segments

AllianceCORE™ Facts

Core Specifics		
Device Family	XC4000E/XL	Spartan
CLBs Used Core Core+Ext logic	 190 190	 196 196
IOBs Used Core[1] Core+Ext logic	 80 61	 80 61
System Clock f_{max}	14 MHz[2]	
Device Features Used	Global Clock Buffers	
Provided with Core		
Documentation	User's Guide, Application Notes, Implementation Instructions	
Design File Format	.ngo netlist Viewlogic source files available extra	
Constraint Files	None	
Verification Tool	Simulation vectors for ViewLogic's ViewSim or Workview Office	
Symbols	ViewLogic	
Evaluation Model	None	
Reference Designs & Application Notes	Sample design for ViewLogic	
Additional Items	Warranty by MDS Netlist only version available on enCORE CD-ROM	
Design Tool Requirements		
Xilinx Core Tools	Alliance/Foundation 1.4	
Support		
Support provided by Memec Design Services.		

Notes:
1. Assuming all core signals are routed off-chip.
2. 4 MHz maximum recommended clock speed to meet industry standard specifications.

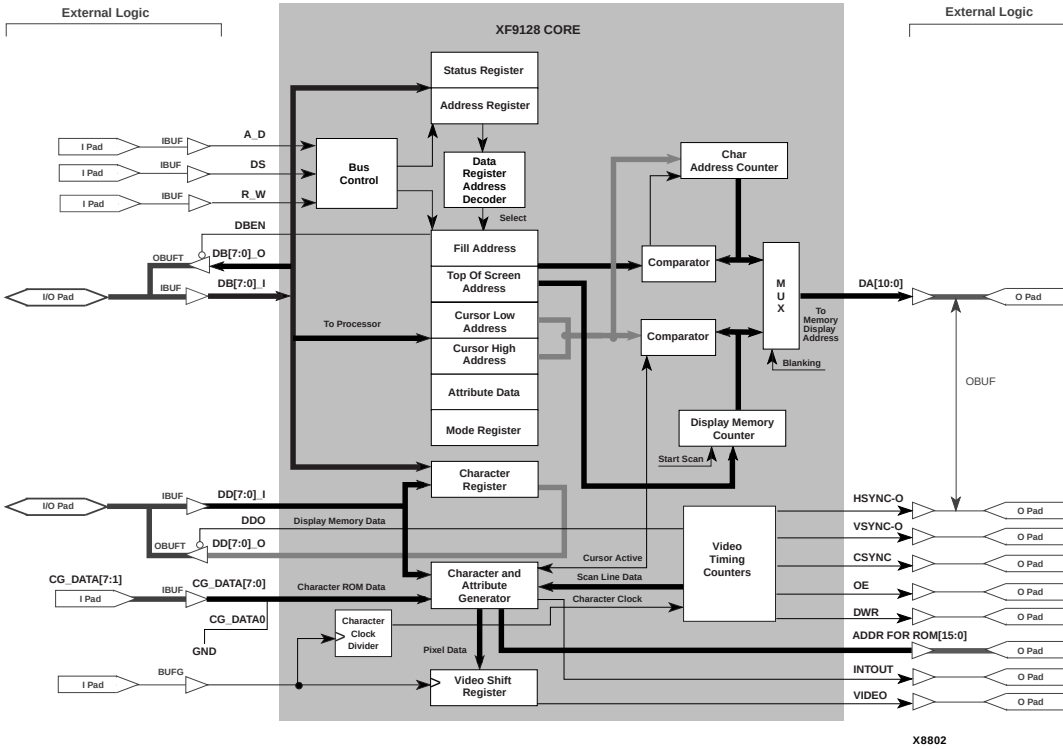

Figure 1: XF9128 Video Terminal Logic Controller Block Diagram

- Scan rows and columns for wide graphics entity elements.
- Data rows per page (8, 10, 12, 16, 20, 24, or 25)

Applications

- ASCII terminal controllers
- Replacement for obsolete Video Terminal Logic Controllers
- Integration of video terminal control logic into an FPGA with other system logic

General Description

The XF9128 Video Terminal Logic Controller (VTLC) core is a programmable video display controller that combines video timing, video attributes, alphanumeric and graphics generation, smooth scroll, and screen buffer interface functions.

The XF9128 VTLC incorporates many of the features required in building a low-cost, yet versatile, display interface. An external programmable 128-character font provides a full-ASCII character set. Wide graphics allow plotting and graphing capabilities while thin graphics and visual attributes can make the display of forms straight forward.

The VTLC core regulates the data flow with data strobe (DS-) and read/write (R_W-) enable signals for use with various microprocessors. The VTLC provides two independent data buses: one bus that interfaces to the processor, and one that interfaces to the display memory. Data is transferred to the display memory from the processor through the XF9128, eliminating contention problems and the need for a separate row buffer.

Pre-programmed constants for critical video timing simplify programming, operation, and improve reliability. A separate non-scrolling status line (enabled or disabled by the processor) is available for displaying system status.

MDS cores are designed with the philosophy that no global elements should be embedded within the core itself. Global elements include any of the following components: STARTUP, STARTBUF, BSCAN, READBACK, Global Buffers, Fast Output Primitives, IOB Elements, Clock Delay Components, and any of the Oscillator Macros. MDS cores only contain resources present in the CLB array. This is done to allow flexibility in using the cores with other logic. For instance, if a global clock buffer is embedded within the core, but some external logic also requires that same clock, then an additional global buffer would have to be used.

In any instance, where one of our cores generates a clock, that signal is brought out of the core, run through a global buffer, and then brought back into the core. This philosophy allows external logic to use that clock without using another global buffer.

A result of this philosophy is that the cores are not self-contained. External logic must be connected to the core inorder to complete it. MDS cores include tested sample designs that add the external logic required to complete the functionality. This datasheet describes both the core and the supplied external logic.

Functional Description

The XF9128 is partitioned into numerous functional blocks as shown in Figure 1, and as described below. Refer to the XF9128 Video Terminal Logic Controller User's Guide for detailed technical information. The User's Guide is available, directly from MDS.

XF9128 VTLC Internal Registers

Addressing of the internal VTLC data registers of the XF9128 is accomplished by using A_D- and R_W- select inputs qualified by the DS- strobe.

Bus Control

The Bus Control block decodes the control signals from the microprocessor to direct data to/from the registers in the VTLC.

Character Clock Divider

This is the divider which counts the number of dots per character to generate Character Clock.

Status Register

When reading the STATUS register, the DONE bit (DB7 of STATUS Register) will represent the current status of the CHARACTER register.

Address Register

Writing a byte to the ADDRESS register will select the specified register the next time the processor writes to or reads the VTLC data registers.

Data Registers:

- FILADD (Fill Address): This register contains the RAM address of the character following the last address to be billed.
- TOSADD (Top of Screen Address): This register contains the RAM address of the first character displayed at the top of the video monitor screen.
- CURLO (Cursor Low): This register contains the eight lower order address bits of the RAM cursor address.
- CURHI (Cursor High): This register contains the three higher address bits of the RAM cursor address (DA10, DA9, DA8).
- ATTDAT (Attribute Data): This register specifies the visual attributes of the video data and the cursor presentation.
- MODE: The AUTO INCREMENT bit in this register specifies whether or not the display memory character address is automatically incremented by the VTLC after every read/write of the CHARACTER register. *Note: the visible cursor position is not affected.*
- CHARACTER: This register allows access to the display memory for both type transfers and FILL operations.
- CHARACTER SET: Using the DB[7:0] data bus I/O pins and the mode select bit in the ATTDAT register, the user can address 128 characters, a six segment "wide graphics" and a four segment "thin graphics" entity.

Character and Attribute Generator

This block modifies character cells as directed by the attribute data associated with each character.

Video Shift Register

This block is simply the high-speed shift register that generates the serial video stream.

Fill Address Comparator

This comparator defines the boundaries of memory area to be filled with a particular character.

Cursor Active Comparator

This comparator compares the Cursor Address registers to the Display Memory Counter and informs the Character and Attribute Generator block when the Display Memory Counter is equal to the Cursor Address Register.

Character Address Counter

This counter is used in conjunction with Display Memory Counter to generate the address for display memory.

Dot Clock Divider

This is the primary scaler for the crystal frequency which generates DOT Clock.

Display Memory Counter

This counter is initialized by the Top Of Screen Address Register and counts through a full screen of data.

Video Timing Counters

These counters generate horizontal sync, vertical sync, and composite sync. They also generate Write Timing for the display memory.

MUX

The MUX controls the source of address to the display memory.

Core Modifications

The XF9128 is designed to meet or exceed the AC Specifications of the industry standard CRT 9128. However, in most cases the Timespecs can be tightened significantly. In all cases, post-route timing analysis should be performed to verify performance. Implementation and other customization are available through Memec Design Services.

Pinout

The XF9128 may be implemented internally with the user's design or as stand-alone logic. Table 1 describes the signal names.

Core Assumptions

The character generator ROM and the ROM that contains the XF9128 core configuration bitstream can be the same ROM. The FPGA loads itself from the ROM using master-parallel mode and then the XF9128 core uses the same ROM for the character look-up table.

Verification Methods

Basic functional simulation has been performed on the XF9128 using ViewSim. (Simulation vectors used for verification are provided with the core).

Recommended Design Experience

Users should be familiar with ViewLogic, Workview Office schematic entry, and Xilinx design flows. Users should also have experience with microprocessor systems.

Ordering Information

The XF9128 Video Terminal Logic Controller core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire gate arrays. Please contact Memec for pricing and more information.

Information furnished by Memec Design Services is believed to be accurate and reliable. Memec Design Services reserves the right to change specifications detailed in this data sheet at any time without notice, in order to improve reliability, function or design, and assumes no responsibility for any errors within this document. Memec Design Services does not make any commitment to update this information.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A_D-	Input	**Address/Data**:Determines whether data is read from, or written to address or status register, or a data register.
DS-	Input	**Data Strobe**: Causes data to be transferred between host microprocessor and XF9128 core. R_W- signal determines whether transfer is a read or write cycle.
R_W-	Input	**Read/Write**: Determines whether host microprocesor is reading data from or writing data into XF9128 (high for read, low for write).
DBEN-	Output	**Data Bus Enable**: Enables OBUFTs for DB:[7:0]_O.
DB[7:0]_O	Output	**Processor or Data Bus**: 8-bit processor output data bus.
DB[7:0]_I	Input	**Processor or Data Bus**: 8-bit processor input data bus.
DD[7:0]_O	Output	**Display Data Out**: 8-bit output to Display Memory.
DD[7:0]_I	Input	**Display Data In**: 8-bit input from Display Memory.
DDO-	Output	**Display Data Enable**: Enables the OBUFT's for DD[7:0]_O.
CG_DATA[7:0]	Input	Data from external character ROM.
DOT_CLK	Input	**Dot Clock**: All video timing is referenced to this input.
DA[10:0]	Output	**Display Memory Address**: 11-bit address bus to external Display Memory SRAM.
HSYNC-O	Output	Horizontal Sync signal to display.
VSYNC-O	Output	Vertical Sync signal to display.
CSYNC	Output	**Composite Sync**: Used to generate an RS170 compatible composite VIDEO signal for output to a composite VIDEO display.
OE-	Output	**Output Enable**: Drives output enable of external Display Memory SRAM.

Table 1: Core Signal Pinout (Cont)

Signal	Signal Direction	Description
DWR-	Output	**Display Memory Write Strobe**: Drives write strobe of external Display Memory SRAM.
ADDR_FOR_ ROM[15:0]	Output	Address from external character ROM.
INTOUT	Output	**Intensity Output**:: Intensity level modification attribute bit (synchronized withvideo data output).
VIDEO-	Output	**Video Output**: Digital waveform used to develop VIDEO and composite VIDEO signals to display. Polarity is: High = Black Low = White

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
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