SpartanÔ -II FPGAs:
A Product Backgrounder

Philosophy

Since the beginning of the programmable logic industry, programmable logic devices (PLD) have been viewed as being expensive, slower, and less feature rich than comparable ASICs. Despite these shortcomings, PLDs have witnessed explosive growth due to the inherent advantage of programmability that provides the digital designer tremendous flexibility and allows much faster time-to-market over ASICs. Due primarily to the time-to-market advantages, PLDs have typically been used for prototyping or low volume production where volumes did not warrant the use of an ASIC.

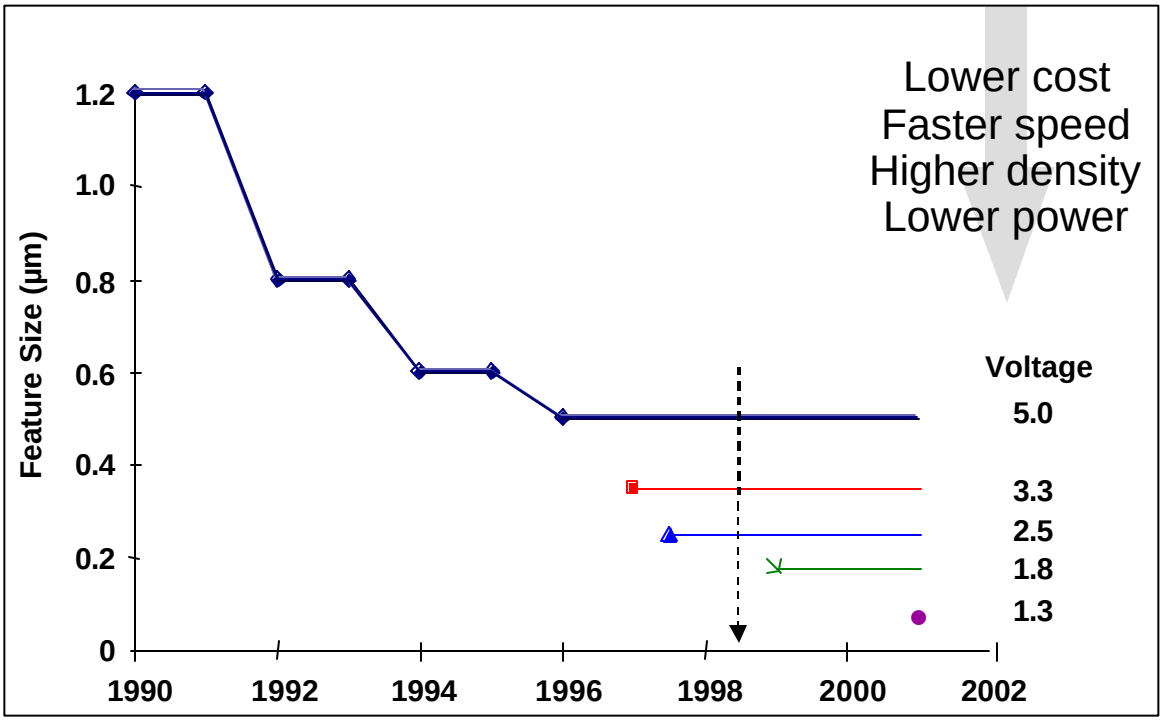
The Spartan FPGA series introduced by Xilinx in January 1998 changes the old paradigm. The Spartan families are chartered to penetrate designs and markets where ASICs typically reign. Markets such as digital modems, printers/faxes, portable audio players (such as MP3), set-top boxes, and POS terminals are examples of high volume designs that have utilized the benefits of the Spartan families. Designed for cost optimization, performance and features, the Spartan series was the first programmable logic family to provide the right mix of feature, price and performance to appeal to the traditional ASIC designer.

The Process Edge

Programmable logic in the past was relegated to using fabrication processes that were one to two generations behind ASICs. In the early 1990's, silicon fabrication companies realized that PLD's were excellent technologies to use for stressing and debugging new processes. As a result, programmable logic was now able to leverage the advantages of advanced process technologies enabling higher densities, smaller die size, and ultimately lower cost. Another phenomenon was also afoot. Programmable logic finally reached a point of bond pad limitation. Bond pad limitation occurs when the number of bond pads (the physical input/output locations on a die)

dictate the size of the silicon die. ASICs had reached this point earlier. This was a significant milestone as it put PLD's on equal footing with ASIC's with regards to silicon cost. For a bond-pad limited semiconductor device, the silicon drives approximately 50 percent of the total device cost.

The backend cost (packaging and test) drive the other 50% of device cost. Since programmable logic is a standard product, Xilinx Inc. maintains a pricing edge over ASIC suppliers by leveraging the higher volumes it drives with its back-end suppliers versus the lower volume and specialized runs that ASIC back-end suppliers must contend with.



The Spartanä -II Family

New products generally fall into one of two of categories: evolutionary or revolutionary. While it is very easy to follow a trend and produce a product with more bells and whistles (evolutionary), it is very difficult to create a product that sets a new standard and changes the paradigm of an industry. The Spartan (5 V family) and Spartan-XL (3.3V family) set the new benchmark for cost and performance in the PLD industry. The revolutionary Spartan-II product family, available now, will again create a new standard in the programmable logic industry for density, feature integration, and performance at cost points previously unthinkable.

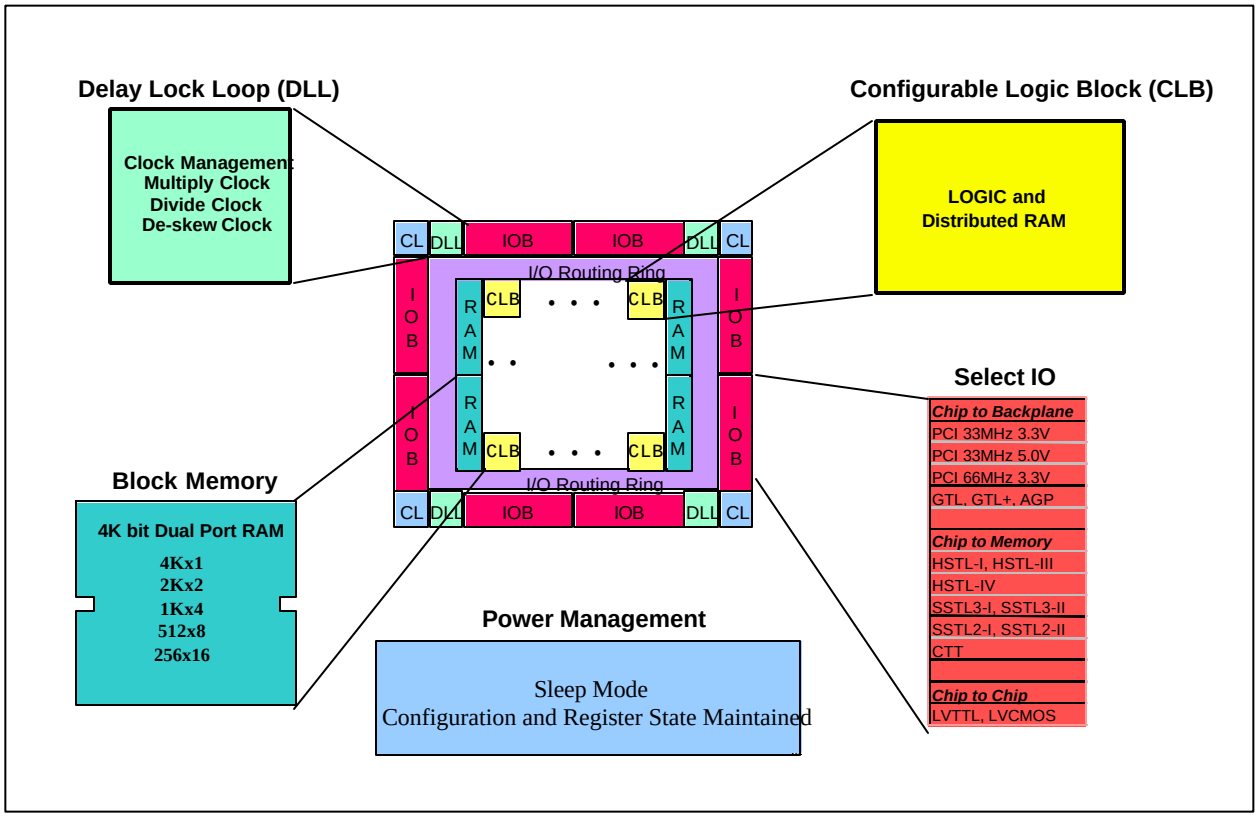
Fabricated on a leading 0.18 µm, six-layer metal process, the Spartan-II family uses the most advanced process technologies available today. The family's core voltage operation is 2.5 V and incorporates I/O technology allowing it to be tolerant to 3.3 and 5 V.

The Spartan-II family stays true to its lineage's charter of providing a compelling solution as an ASIC replacement device family. With the introduction of the Spartan-II family , Xilinx now casts a greater net over addressable logic design going after popular application specific standard products (ASSP) devices. (For more information regarding how the Spartan-II family addresses traditional ASIC and ASSP designs, refer to: The Spartan-II family – The Complete Package)

Device	XC2S15	XC2S30	XC2S50	XC2S100	XC2S150
System Gates	15K	30K	50K	100K	150K
Logic Cells	432	972	1728	2700	3888
Block RAM Bits	16,384	24,576	32,768	40,960	49,152
Block RAM Blocks	4	6	8	10	12
DLL's	4	4	4	4	4
I/O Standards Supported	17	17	17	17	17
Max I/O	82	132	176	196	260
Packages 14x14mm	VQ100	VQ100			
20x20mm	TQ144	TQ144	TQ144	TQ144	
12x12mm	CS144	CS144			
28x28mm		PQ208	PQ208	PQ208	PQ208
17x17mm			FG256	FG256	FG256
23x23mm				FG456	FG456

Integrated Features

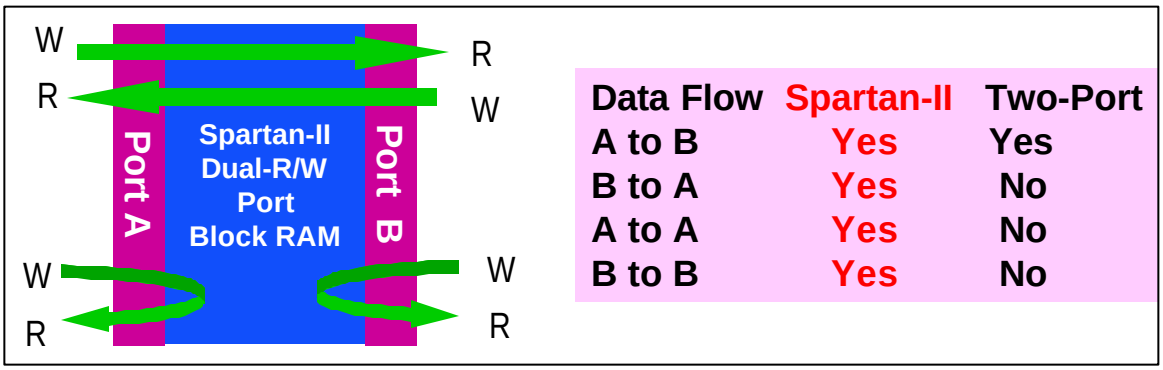
The Spartan-II family is about low cost and fast time-to-market but more importantly, the integration of powerful new system-level features that provide a very compelling solution for today's system-level designer. Spartan-II FPGAs incorporate delay lock loops (DLLs), Block RAM, distributed RAM, programmable I/Os of the Select I/O™ feature, ultra-high performance, and aggressive power management. All of the features found in ASICs and ASSP devices may now be found in the Spartan-II family at price points that either meet or beat its counterparts. Spartan-II FPGAs will also sport an impressive stable of highly complex cores (intellectual property) enabling designers to further leverage the time-to-market benefits that a programmable solutions provide at no cost penalty.



Spartan-II family Architecture

Memory

On-chip memory has become vital to most designs done today. From buffering data between two dissimilar buses to providing storage locations of constants for high performance DSP functions, memory implementation on the device is now an absolute requirement for programmable logic devices. The Spartan-II family provides designers maximum flexibility when integrating memory on chip. Xilinx pioneered the capability of distributed memory (also found on Spartan and Spartan-XL families), which efficiently implements wide/shallow FIFO memories or scratch pad memory locations. The family also incorporates block RAM (in block of four Kbits) which efficiently implement memory configurations such as wide/deep FIFOs, single port RAM, and True Dual Port RAMs. Unlike competing two-port architectures, Xilinx provides designers true dual port RAM operation, implementing high-speed access and write times.



Data Flow	Spartan-II	Two-Port
A to B	Yes	Yes
B to A	Yes	No
A to A	Yes	No
B to B	Yes	No

Spartan-II Family Dual Port Memory

Delay Lock Loops

One of the most exciting features that Spartan-II family offers is the integration of delay lock loops (DLLs). This new feature offers a wealth of new options to the digital designer. DLLs perform the same tasks as traditional phase lock loops (PLLs) but are more robust and do not create the noise interference commonly seen with PLLs.

The Spartan-II DLLs allow the designer to multiply or divide the incoming clock on chip as well as drive multiple clocks on the board. The DLL feature also allows the designer to de-skew the clock on chip, ensuring all nodes on the device are synchronized and do not suffer from excessive set-up and hold times.

Powerful new possibilities may now be realized with the DLL feature. For instance, it is now possible to architect a design to use a smaller number of gates. By increasing the clock frequency on chip and performing many more clock cycles per board clock period, a design may need to use only a fraction of the gates that normally would be required. This will leave gates on the device free for other functionality, effectively increasing the efficiency a designer may realize with the Spartan-II family.

With four DLLs per device, the Spartan-II family provides a sufficient number or DLLs with which designers may perform multiple functions. For example, one DLL may be used to de-skew the clock on chip, one for multiplying the clock for accelerated performance on chip, two DLLs to drive clocks to various devices on the board—all at the same time.

A crystal and Spartan-II device may provide all the clock management that a designer may need for their board design!

Select I/O^{Ô}

The Spartan-II family has incorporated powerful new input/output standards that drive high performance designs today. From SSTL (-1, -2, -3) to HSTL (-1, -2) to AGP to GTL and GTL+, and PCI, the family can easily accommodate the most demanding I/O requirements. The integration of these standards into the Spartan-II family now allow the elimination of costly bus transceivers that take up valuable board real estate and precious financial resources.

In fact, the Spartan-II family supports up to 17 of the most popular and demanding I/O standards. The family supports all high-speed memory interfaces that are currently found in the marketplace today.

The I/Os for the Spartan-II family are 5 V and 3.3 V tolerant for interfacing with older generation technology on the board. This is a significant advantage for the family as competing architectures are unable to support 5 V tolerance.

Support for high-speed interfaces details another important fact: I/O performance. The I/O performance is significantly increased over the Spartan (80 Mhz) and Spartan-XL (100 Mhz) to a blazing 200 Mhz.

Power Management

Power consumption is an important issue, especially for portable or hand-held designs. The Spartan-II family extends power management features that were first established with the Spartan-XL family, which is having a power down pin available on each device. Once activated, the device goes into a low power (sleep mode) in which power consumption is reduced significantly. When the pin is de-asserted, the device comes back into full power mode and retains its configuration as well as register states.

Pricing

The Spartan-II family has been created from the ground-up in keeping with the Spartan Series philosophy to provide industry-leading features, density, and performance at price points that match or beat ASICs and ASSP devices. The family has been able to achieve a milestone long sought after and promised by the programmable logic industry but now only realized by the Spartan-II family—10,000 gates for $1.00USD. This is found in the XC2S100™ device, the 100,000 gate device which will resale at just under $10 (250,000 units and higher). Below is a complete listing of high volume prices available for the Spartan-II family at introduction.

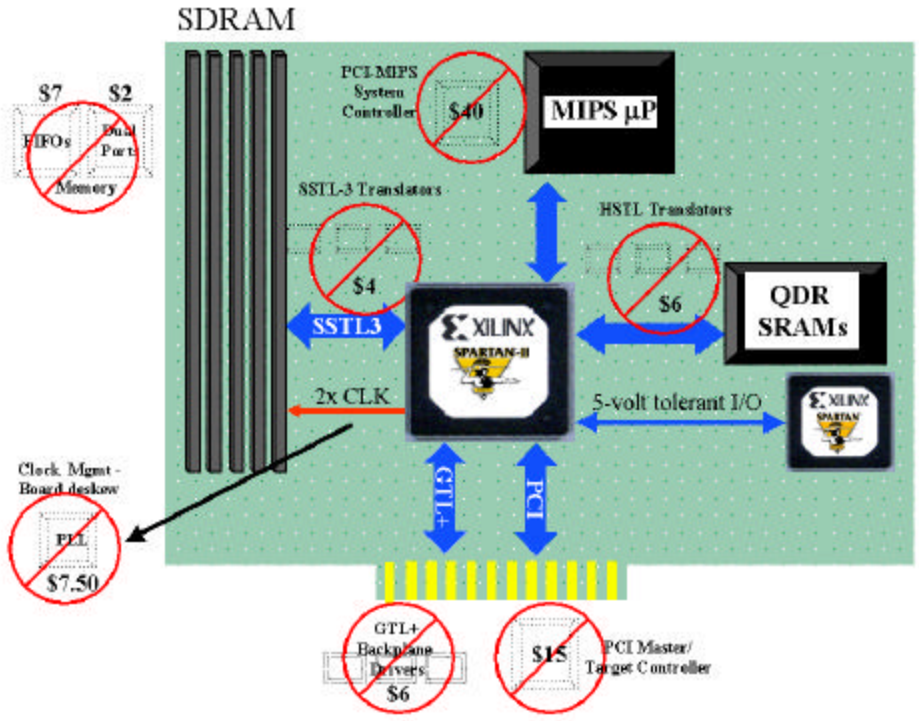
Xilinx Spartan II	
Product	Hi Volume Price*
XC2S15	$3.95
XC2S30	$4.95
XC2S50	$7.95
XC2S100	$9.95
XC2S150	$12.95

*250Ku Resale price, slowest speed/cheapest package (end CY2000)

Spartan-II Family Pricing

Spartan-II: The Value

Previously mentioned are the details of many features and benefits that the Spartan-II family brings to the marketplace. Below, is a board diagram detailing the appeal of the family.



Using some HSTL translators as well as the clock management device brings a combined cost of $13.50 (high volume prices for each). Both of these functions may be integrated into the XC2S100 Spartan-II device for $10. Clearly, the Spartan-II device is lower priced than the two discrete solutions combined, but the design has yet to implement logic or utilize the memory of the device. Assume the design requires a PCI master/target controller as well. The combined discrete solution is now $15 + $6 + $7 = $28. The Spartan-II solution, combining all three functions is still $10, almost two-thirds less than the discrete solution with room to spare for more logic integration. The Spartan-II solution also uses less board real estate, is lower power, and provides higher reliability (by virtue of fewer components on the board).

In summary, the Spartan-II family offers the high volume ASIC/ASSP designer the most cost effective, flexible solution enabling the fastest time-to-market with the lowest possible risk

For more information regarding how the Spartan-II family addresses traditional ASIC and ASSP designs, please refer to: The Spartan-II family – The Complete Package