An editor's glance at the XC9500XL ISP CPLD family

Xilinx Ships First 0.35-micron 3.3-volt FLASH CPLDs

Leadership Speed, Cost, and Reliability Enable New Markets

The in-system programmable XC9500XL family is the first 3.3-volt CPLD family to offer substantially higher speed and lower cost than equivalent 5-volt devices. These features open new applications currently out of reach of CPLDs, such as communications and computing market segments, as well as penetrate new markets in consumer and automotive applications. The XC9500XL family has the fastest pin-to-pin performance, smallest die size, and highest level of in-system reliability of any CPLDs currently available. It is expected to further accelerate the CPLD industry technology switch to double-polysilicon FLASH technologies from the older single-polysilicon EEPROM technologies.

Process:

- highly scalable FastFLASH technology to 0.25-micron and 0.18-micron feature-sizes
- the first mainstream CPLDs to be shipping on a 0.35-micron feature-size technology
- FastFLASH technology employs 0.35-micron rules for the 4-layer metal as well as drawn transistor lengths, with 0.25-micron (L_{eff})

XC9500XL Product Features:

- first 3.3-volt CPLD product to deliver the highest available reliability characteristics available to JTAG ISP devices
  - ~ 20-year data retention and 10,000 endurance cycles—qualities normally associated with FLASH memory
  - ~ data retention that's twice as long and 100 times more reliable than other JTAG ISP CPLDs
- Highest performance: 4 nanoseconds pin-to-pin speed and 200 MHz system frequency
- Leading-edge CSP for small hand-held consumer applications; allows increased user programmability with the highest reliability at the lowest cost
- Ultra wide block fan-in of 54, for superior pin-locking characteristics
- Most product-terms per macrocell of 90
- Leading-edge I/O flexibility and compatible with 5-volt, 3.3-volt, and 2.5-volt signals
  - ~ input hysteresis on all pins and bus-hold circuitry for simple bus interfaces
- Most complete JTAG boundary-scan support with 8 instructions
- Fast concurrent programming times

Product availability:	**Macro cells**	**Maximum I/Os**	**Pin-to-pin delay (t_{PD})**	**System frequency (f_{SYS})**	**Price ***	**price per macrocell**
XC9536XL-10 (PC44)	36	34	4 ns	200 MHz	$1.20	$0.03
XC9572XL-10 (PC44)	72	72	5 ns	178 MHz	1.85	0.03
XC95144XL-10 (TQ100)	144	117	5 ns	178 MHz	5.65	0.04
XC95288XL-10 (TQ144)	288	168	6 ns	151 MHz	11.95	0.04

* Pricing for 100,000-plus unit quantities in mid-1999

Package options:

44-pin PLCC; 100-pin and 144-pin TQFP; 352-pin BGA; 208-pin PQFP; 48-pin and 144-pin CSP

Software support:

The XC9500XL family is supported in the Foundation and Alliance Series Software version 1.5. Device programming can be done with the supplied cable, and embedded controller, or automatic test equipment.