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Real RapidIO Core Enables Terabit Networks

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One of the major challenges in building terabit-capable systems is improving the performance system interconnect — the speed at which various components such as microprocessors, memory, and peripherals communicate with each other. However, with the RapidIO architecture you can boost system throughput significantly by eliminating chip-to-chip communication bottlenecks. As the industry's first RapidIO solution, the Real RapidIO core is the latest in a series of high performance LogiCOREs fully supported through the Xilinx Platform FPGA SystemIO™ solution. You can combine the advantages of the Platform FPGA and the RapidIO architecture to build high performance optical networks, gigabit and terabit routers, and network servers. This week, Abhijit Athavale, the Solution Marketing Manager for System Interfaces Solutions at Xilinx, discusses the capabilities of this new core.

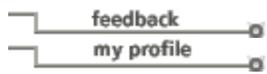
Q: What is RapidIO Interconnect? The RapidIO specification defines a technology that can support throughputs exceeding 10 Gbps by using high clock rates, LVDS signaling, and source synchronous clocking. It is a low latency, memory-address based protocol that supports multi-processor architectures, is scalable, reliable, and transparent to application software.

Q: What are the key features of the new Real RapidIO IP Core? The Real RapidIO Physical Interface, a fixed netlist solution for creating the RapidIO interconnect, is a pre-implemented and tested module for the latest, high-density Virtex™-II Platform FPGAs, offering:

- as an 8-bit LVDS port with 64-bit internal data path, 250 MHz clock, and 500 Mbps per pin pair throughput. The Virtex-II FPGAs meet all required electrical and timing parameters including setup, hold, and clock to output time, as well as AC output drive characteristics stated in the 250 MHz RapidIO AC specification.
- Time-To-Market Advantage — Xilinx Smart-IP™ Technology ensures the highest predictability, repeatability, and flexibility in LogiCORE™ designs. By pre-defining the pinout and relative placement of the internal logic, and by controlling critical paths with a constraints file to assure a predictable timing result, your product development time is significantly reduced.

Q: How is the interoperability of the RapidIO solution ensured? The Real RapidIO core has been verified with v1.4 RapidIO Bus Functional Models provided by the RapidIO Trade Association. Members include Alcatel, Cisco, Ericsson, EMC, IBM, and Nortel. Xilinx has also teamed with Motorola, a founding member of the RapidIO Trade Association, for RapidIO product validation.

For more information on the RapidIO solution, see: www.xilinx.com/rapidio.



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