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System Ace: Configuration Solution for Xilinx FPGAs

By: Eric Thacker, Xilinx, Inc.

Design techniques for electronic systems are constantly changing. In industries at the heart of the digital revolution — telecommunications, networking, and wireless communications — this change is especially acute. Functional integration, dramatic increases in complexity, new standards and protocols, and increased time-to-market pressures have bolstered both the design challenges and the opportunities in architecting modern electronic “boxes.” One trend driving these changes is the increased integration of core logic with previously discrete functions to achieve higher performance and more compact board designs. Traditionally, ASICs have been the vehicle for such integration but now, with their advanced system capabilities, programmable logic devices (PLDs), especially field programmable gate arrays (FPGAs), have begun to take on this role in system design.

Trends in FPGA Usage

Until recently, PLDs had been used primarily as “glue logic,” tying various system functions together and acting as programmable high-speed interface logic. In these instances, FPGA usage was usually limited to one or two chips per system. Now, however, the new generation of FPGAs, with their integration of specialized functionality and expansion of performance and capabilities, are being used as the core of advanced electronic systems. This increasing role of FPGAs at the heart of system development has been spurred in part by Xilinx Platform FPGA efforts to integrate specialized functions and high-performance application and interface circuitries into the FPGA fabric. The flexibility and increase in capabilities of the FPGA relative to ASICs, especially given the pressures of greatly compressed product development cycles, has accelerated the use in systems of multiple FPGAs as their core logic. In addition, the average density of FPGAs designed into new systems is growing rapidly. According to Dataquest, average individual FPGA design-in density grew 113% in 1999 and 67% in 2000.

The increased usage of FPGAs has led to a growing focus on designing for FPGA configuration. When only one or two FPGAs were used in a system requiring only one configuration bitstream, a dedicated configuration PROM was a fast and simple configuration solution. In those cases, the board space cost taken up by the PROM was offset by the speed and ease of implementing a PROM-based solution. As the number of FPGAs per system and the need for flexibility in configuration grows, using multiple dedicated PROMs becomes unwieldy. In such a case, it is sometimes more efficient to have centralized source for configuration of all FPGAs. Traditionally, designers have often used an embedded solution using on-board commodity Flash controlled by a microprocessor or PLD. When a microprocessor is used, configuration data is pulled directly from system memory over the memory bus and fed to the FPGA chain via JTAG. Alternatively, PLDs paired with commodity Flash can be used to configure FPGA chains, supplying bitstream data either serially or in parallel using an 8-bit word for faster configuration speeds.

Such embedded FPGA configuration options are often complex design challenges requiring valuable development bandwidth. System engineers must devote design time and effort to developing and testing the microcode for having the microprocessor control configuration. In addition, using the microprocessor to manage general system startup and FPGA configuration simultaneously can delay startup times. There is also a danger of bus contention with the FPGAs competing with other resources for microprocessor and memory access. Embedded solutions also require extra board space for the additional memory used for configuration storage. If Boundary Scan (JTAG) is used for board test or FPGA programming, separate trace lines and scan-chain-control chips may also be required. In designs using FPGAs and CPLDs as configuration controllers, designers must still add an additional packaged part to the board simply to convert FPGA clocks to address increments and, in serial mode, to serialize the data. The FPGA also requires a separate PROM to configure it as the controller.

System ACE Technology

Given the options described above and the growing need for configuration flexibility, designers using multiple FPGAs that need large numbers of configuration bits and enhanced configuration flexibility were faced with a need to make a tradeoff: Use a self-contained, pre-engineered multi-PROM solution at the expense of board space or devote engineering development and debug time to design a customized, space-efficient, flexible configuration solution. To meet the need for a space-efficient, pre-engineered, high-density configuration solution for multi-FPGA systems, Xilinx has

developed the System Advanced Configuration Environment (System ACE™) family of configuration solutions.

The System ACE series is designed to meet the growing need for flexible, high-density storage and configuration control. This series combines Xilinx expertise in configuration control logic with industry expertise in high-density, low-cost data storage to provide a complete platform for meeting any configuration need. All System ACE product lines support multiple-bitstream management, FPGA microprocessor cores, and system reconfiguration/update over a network. They also provide an easily scalable and reusable configuration platform, a built in interface to a system processor, and the ability to centralize configuration for the entire system, simplifying debug and minimizing board space. The three product lines in the System ACE series are System ACE CF (CompactFlash), System ACE MPM (Multi-Package Module), and System ACE SC (Soft Controller).

System ACE CF

The first member of this family, System ACE CF, using standard memory based on the CFA CompactFlash standard, is a very flexible, high-density, two-piece configuration solution comprising the ACE Flash™ module and the ACE Controller™ chip. The ACE Flash interface can accommodate removable CompactFlash modules, currently ranging from 64 Mbits to over 1 Gbit, or IBM Microdrives, currently ranging from 2 Gb to 8 Gb, all with identical form factor and board space requirement. For perspective, individual Virtex™-II FPGAs require from 300 Kbits to 29.0 Mbits of configuration data, meaning you can configure over 250 of the largest members of the Virtex-II family with one System ACE CF solution. The use of CompactFlash gives system designers access to low-cost, high-density Flash in a very efficient footprint that does not change with density or new product generations. Thus designers have the flexibility to change the density of ACE Flash as needed without any board redesign. Because CompactFlash is a removable medium, making changes or upgrades to the memory contents or density can be done simply by exchanging removable modules or by programming in system.

The ACE Controller chip has built-in control logic with a variety of specialized interfaces. This chip is the interface to the ACE Flash, the FPGA chain, an external test environment, and a system microprocessor. The default configuration mode takes bitstreams from the memory module and configures a chain of FPGAs via Boundary Scan. There is also a Boundary Scan test and programming interface to aid with system prototyping and debugging.

There are three main advantages to the System ACE CF solution: system configuration management, upgrade management, and flexible file management.

System Configuration Management

System ACE CF is the first pre-engineered configuration solution to provide both the bit density and the control logic to manage configuration for all FPGAs within a system from one centralized location. Centralizing configuration management minimizes board space, simplifies design modifications (either during prototyping or in the field), and opens the door for system microprocessors to take a more interactive role in managing re-configuration to increase system flexibility. In systems with multiple boards connected through a backplane, one System ACE module can be used per board to manage each board's FPGA configuration. If one Boundary Scan chain connects all FPGAs across multiple boards through the backplane, just one System ACE module can be used to configure all FPGAs across these boards.

System ACE CF also allows for storage of multiple bitstreams at one time in one location. This allows one board design to serve multiple purposes. For example, if slight variations of an FPGA-based system are being shipped to different markets (e.g., to accommodate different interface, broadcast, or electrical standards), designers can design a single system for all these markets with the only difference being which bitstream inside the CompactFlash is used for system configuration.

Upgrade Management

The System ACE CF solution also greatly simplifies upgrading FPGA-based systems; all that is required is that a new or changed bitstream be stored in the ACE Flash module. Because it is centralized, System ACE CF allows designers to update their entire system simply by changing the contents of one ACE Flash module, either through physical removal or in-system re-programming, making updating and debugging much easier. Whether for a prototyping board in a lab or an installed system in the field, manually reconfiguring an FPGA-based system using the removable System ACE CF requires little effort.

In-system programming can be accomplished either via cable or a network interface. Network reconfiguration of System ACE CF memory eliminates the need for a direct interface by enabling users to update or debug their systems remotely by transmitting a new bitstream over a network (e.g., internet or wireless WAN). In addition, the ability to store multiple bitstreams and have the microprocessor activate any bitstream at any time allows system administrators to maintain access to previous versions of system configuration for use in the event that a problem with a newly transmitted configuration is discovered

Flexible File Management

The file structure of the ACE Flash module simplifies the storage and management of multiple bitstreams. This multiple bitstream capability empowers designers to use a single ACE Flash card to run multiple BIST patterns, run PCI applications, or store multiple bitstream variations on a single design (e.g., versions for North America, Europe, Japan, and China). Also, designers using Xilinx FPGAs with Empower!TM embedded processors can store the FPGA configuration bits and the processor microcode in the same source, with System ACE CF handling the initialization of both the FPGA cells and the delivery of microprocessor initialization software. System ACE CF can also store multiple applications that are used by the processor core and deliver them as needed. Designers also have the flexibility to store related files in the memory module, such as release notes, revision history, user guides, FAQs, or any other supporting files. The microprocessor interface also enables the utilization of unused ACE Flash capacity for purposes other than bitstream storage, e.g., generic system scratchpad memory.

Designers can use ACE Flash supplied by Xilinx (128 Mb or 256 Mb) or any standard CompactFlash modules available from a variety of third-party suppliers. IBM Microdrives can also be used. The ACE Controller comes in a 144-pin TQFP package.

System ACE MPM

System ACE MPM is a single-package solution containing a packaged FPGA and PROM for configuration control and a packaged AMD Flash for configuration storage. A single-package solution simplifies manufacturing and board design while reducing the number of part numbers that must be managed for configuration. Xilinx offers the System ACE MPM in 16-, 32-, and 64-Mbit densities.

Like other members of the System ACE series, System ACE MPM uses a form of standard Flash memory as the storage medium. This makes available any advances in cost, voltage, performance, or density that occur in the standard Flash market. The use of an FPGA as the configuration controller makes available any advances in I/O performance or interface voltage and guarantees future FPGA compatibility.

One hallmark of the System ACE MPM solution is the support of multiple configuration modes and performance up to 152 Mbps. System ACE MPM can configure FPGAs in two ways: Slave serial (1 bit) for a one, two, four, or eight FPGA chains, and SelectMAP (8 bit) for up to four FPGAs. This multiple-mode support gives customers the flexibility to design their boards to maximize system performance while minimizing board space and/or trace lines.

System ACE MPM configuration control technology is the first Xilinx configuration solution to support bitstream compression. Bitstream compression enables users to reduce the density of configuration storage density for a given FPGA chain. For example, the Virtex-II 8,000-gate FPGA requires over 26 Mb of configuration data. Without compression, designers would have to use a 32-Mb System ACE MPM to configure this FPGA. Compression could reduce the size of the bitfile to a size that would fit in the 16-Mb System ACE MPM, reducing the cost of the total solution. The amount of compression varies with the characteristics of a design's bit pattern.

System ACE SC

System ACE SC is a downloadable version of the System ACE MPM controller, offering all the same capabilities — implemented in a stand-alone FPGA — without the integrated single-package form factor. With System ACE SC, you connect a configuration-dedicated FPGA on your board to an AMD memory Flash chip for configuration storage. Using the downloaded bitstream to configure the configuration FPGA gives you a complete, pre-engineered configuration solution for all the other Virtex and Spartan™ FPGAs in your system.

Software

System ACE software integrates seamlessly with existing Xilinx programming software and uses a standard file management structure allowing for drag-and-drop file manipulation on ACE Flash from any Windows' PC environment. Unix versions will also be available.

With increased usage of multiple FPGAs as the core logic of modern electronic systems, having a pre-engineered, flexible, and robust configuration solution is of growing importance. System ACE technology frees systems engineers from the need to design an FPGA configuration system and allows them to focus their design effort on maximizing system performance and achieving faster time to market.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/25/01	1.0	Initial Xilinx release.