Packaging and Thermal Characteristics

Package Information NEW!

This section contains the following information:

- **Inches and Millimeters**
- **Dimensions for Xilinx Quad Flat Packs**
- **Suggested Board Layout of Soldered Pads for BGA Packages**
- **Recommended PCB Design Rules**
- **Cavity Up or Cavity Down**
- **Clockwise or Counterclockwise**
- **Summary of Thermal Resistance for Packages**

Inches vs. Millimeters

The JEDEC standards for PLCC, CQFP, and PGA packages define package dimensions in inches. The lead spacing is specified as 25, 50, or 100 mils (0.025", 0.050" or 0.100").

The JEDEC standards for PQFP, HQFP, TQFP, and VQFP packages define package dimensions in millimeters. These packages have a lead spacing of 0.5 mm, 0.65 mm, or 0.8 mm.

Because of the potential for measurement discrepancies, this Data Book provides measurements in the controlling standard only, either inches or millimeters. (See Table 1 for package dimensions.)

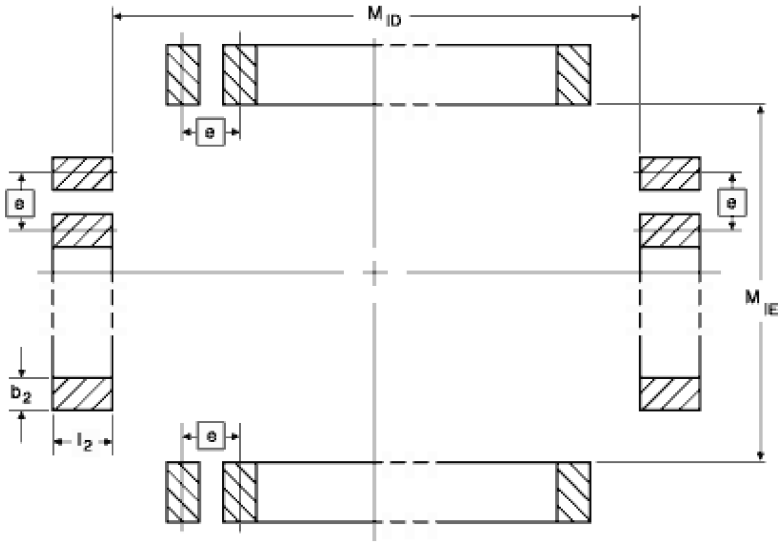

Figure 1: EIA Standard Board Layout of Soldered Pads for QFP Devices

Table 1: Dimensions for Xilinx Quad Flat Packs(1)

Dim.	VQ44	VQ64	PQ100	HQ160 PQ160	HQ208 PQ208	VQ100 TQ100	TQ144	TQ176	HQ240 PQ240	HQ304
MID	9.80	9.80	20.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
MIE	9.80	9.80	14.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
E	0.80	0.50	0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50
B2	0.4-0.6	0.3-0.4	0.3-0.5	0.3-0.5	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4	0.3-0.4
I2	1.60	1.60	1.80 (2)	1.80	1.60	1.60	1.60	1.60	1.60	1.60

Notes:
1. Dimensions in millimeters.
2. For 3.2 mm footprint per MS022, JEDEC Publication 95.

Suggested Board Layout of Soldered Pads for BGA Packages

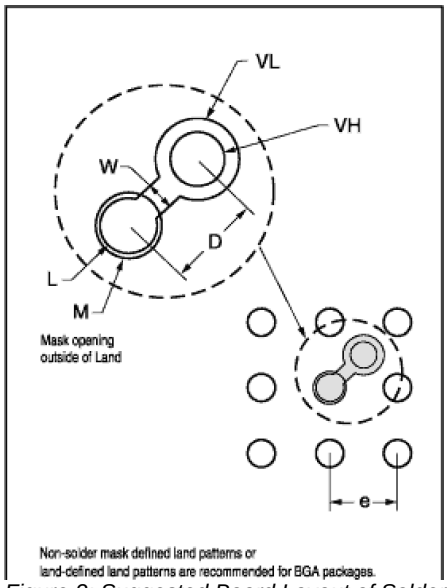

Figure 2: Suggested Board Layout of Soldered Pads for BGA Packages(1)

Table 2: Recommended PCB Design Rules

	FG256	FG456	FG676	FG680	FG860	FG900	FG1156	FF896	FF1152	FF1517
Component land Pad Diameter (SMD)(2)	0.45	0.45	0.45	0.50	0.50	0.45	0.45	0.58	0.58	0.58
Solder Land (L) Diameter	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.50	0.50	0.50
Opening in Solder Mask (M) Diameter	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.60	0.60	0.60
Solder (Ball) Land Pitch (e)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Line Width Between Via and Land (w)	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13
Distance Between Via and Land (D)	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70
Via Land (VL) Diameter	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61
Through Hole (VH) Diameter	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300
Pad Array	Full	Full	Full	Full	Full	Full	Full	Full	Full	Full
Matrix or External Row	16 x 16	22 x 22	26 x 26	39 x 39	42 x 42	30 x 30	34 x 34	30 x 30	34 x 34	39 x 39
Periphery Rows	-	7(3)	-	5	6	-	-	-	-	-

Table 2: Recommended PCB Design Rules (continued)

	BG225	BG256	BG352	BG432	BG560	BG575	BG728	BF957	CS144	CP56
Component land Pad Diameter (SMD)	4 0.63	0.63	0.63	0.63	0.63	0.61	0.61	0.61	0.35	0.30
Solder Land (L) Diameter	0.58	0.58	0.58	0.58	0.58	0.56	0.56	0.56	0.33	0.27
Opening in Solder Mask (M) Diameter	0.68	0.68	0.68	0.68	0.68	0.66	0.66	0.66	0.44	0.35
Solder (Ball) Land Pitch (e)	1.50	1.27	1.27	1.27	1.27	1.27	1.27	1.27	0.80	0.50
Line Width Between Via and Land (w)	0.300	0.203	0.203	0.203	0.203	0.203	0.203	0.203	0.13	0.13
Distance Between Via and Land (D)	1.06	0.90	0.90	0.90	0.90	0.90	0.90	0.90	0.56	-
Via Land (VL) Diameter	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.51	0.51
Through Hole (VH) Diameter	0.356	0.356	0.356	0.356	0.356	0.356	0.356	0.356	0.250	0.250

Diameter										
Pad Array	Full	-	-	-	-	Full	Full	Full	-	-
Matrix or External Row	15 x 15	20 x 20	26 x 26	31 x 31	33 x 33	24 x 24	27 x 27	31 x 31	13 x 13	10 x 10
Periphery Rows	-	4	4	4	5	-	-	-	4	1

Notes:
1. 3x3 matrix for illustration only, one land pad shown with via connection.
2. Component land pad diameter refers to the pad opening on the component side (solder mask defined).
3. FG456 package has solder balls in the center in addition to periphery rows of balls.

Cavity Up or Cavity Down

Most Xilinx devices attach the die against the inside bottom of the package (the side that does not carry the Xilinx logo). This is called cavity-up, and has been the standard IC assembly method for over 25 years. This method does not provide the best thermal characteristics. Pin Grid Arrays (greater than 130 pins) and Ceramic Quad Flat Packs are assembled "Cavity Down", with the die attached to the inside top of the package, for optimal heat transfer to the ambient air.

For most packages this information does not affect how the package is used because the user has no choice in how the package is mounted on a board. For Ceramic Quad Flat Pack (CQFP) packages however, the leads can be formed to either side. Therefore, for best heat transfer to the surrounding air, CQFP packages should be mounted with the logo up, facing away from the PC board.

Clockwise or Counterclockwise

The orientation of the die in the package and the orientation of the package on the PC board affect the PC board layout. PLCC and PQFP packages specify pins in a counterclockwise direction, when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin 1 in the center of the beveled edge while all other packages have pin 1 in one corner, with one exception: The 100-pin and 165-pin CQFPs (CB100 and CB164) for the XC3000 devices have pin 1 in the center of one edge.

CQFP packages specify pins in a clockwise direction, when viewed from the top of the package. The user can make the pins run counterclockwise by forming the leads such that the logo mounts against the PC board. However, heat flow to the surrounding air is impaired if the logo is mounted down.

Table 3: Summary of Thermal Resistance for Packages

	$Theta_{JA}$ still air (Max)	**$Theta_{JA}$ still air (Typ)**	**$Theta_{JA}$ still air (Min)**	**$Theta_{JA}$ 250 LFM (Typ)**	**$Theta_{JA}$ 500 LFM (Typ)**	**$Theta_{JA}$ 750 LFM (Typ)**	**$Theta_{JC}$ (Typ)**	
Package Code	**°C/Watt**	**°C/Watt**	**°C/Watt**	**°C/Watt**	**°C/Watt**	**°C/Watt**	**°C/Watt**	**Comments**
BF957	11.2	10.9	10.6	6.75	5.35	4.6	1.1	2S, 2P, Simulation
BG225	37	30	24	19	17	16	3.3	Various
BG256	32	29	24	19	17	16	3.2	4L/2P-SMT
BG352	14	12	10	8	7	6	0.8	4L/2P-SMT
BG432	13	11	9	8	6	6	0.8	4L/2P-SMT
BG492	17.22	17.22	17.22	12.25	11.94	11.92	0.8	4L/2P-SMT
BG560	11.24	10.56	10.22	7.41	6.08	5.53	0.82	4L/2P-SMT
BG575	16.9	16.9	16.9	13.7	12.6	11.8	4.7	2S, 2P, Simulation
BG728	13.7	13.5	13.2	10.24	9.3	8.74	2.22	2S, 2P, Simulation
CB100	44	41	38	25	19	17	5.1	Socketed
CB164	29	26	25	17	12	11	3.6	Socketed
CB196	25	24	24	15	11	10	1.8	Socketed
CB228	19	18	17	11	8	7	1.3	Socketed
CG1156	10.7	-	1.0	8.0	7.6	6.8	-	2S, 2P, Simulation
CP56	65	65	65	-	-	-	15	Estimated
CS48	-	45	-	-	-	-	-	Estimated
CS144	-	65	-	-	-	-	-	Estimated

CS280	30.5	-	0.8	25	23.1	23.2	-	Estimated
DD8	114	109	97	90	73	60	8.2	Socketed
FF896	11.8	11.8	11.8	8.2	6.7	5.9	1.1	2S, 2P, Simulation
FF1152	11.9	11.65	11.4	7.55	6.05	5.2	1.1	2S, 2P, Simulation
FF1517	10.5	10.5	10.5	6.5	5.1	4.4	1.1	2S, 2P, Simulation
FG256	27	25	23	21	20	19	3.9	4L/2P-SMT
FG324	22.3	22.3	22.3	17.6	16.0	15.4	1.8	4L/2P Sub, 4L PCB
FG456	19	18	17	14	13	13	4.8	4L/2P-SMT
FG556	14	14	14	10	9	9	0.8	4L/2P-SMT
FG676	17	17	17	13	12	12	3.2	4L/2P-SMT
FG680	11	11	10	8	6	6	0.9	4L/2P-SMT
FG860	10	10	10	7	6	5	0.8	4L/2P-SMT
FG900	14	14	14	10	9	9	2.4	Estimated
FG1156	14	13	13	10	9	9	1.85	Estimated
FT256	27.5	29.7	31.9	25.23	23.55	22.8	3.83	2L Substrate, 4L PCB
HQ160	14	14	14	10	8	7	1.0	4L/2P-SMT
HQ208	15	14	14	10	8	7	1.7	4L/2P-SMT
HQ240	13	12	12	9	7	6	1.5	4L/2P-SMT
HQ304	11	11	10	7	5	5	0.9	4L/2P-SMT
MQ208	18.36	17.86	17.38	13.98	12.6	35.35	11.85	2L/0P-SMT
MQ240	16.78	16.65	16.45	11.98	10.79	10.49	1.21	2L/0P-SMT
PC20	86	84	76	63	56	53	25.8	2L/0P-SMT
PC28	67.58	66.06	63.02	49.8	44.56	41.59	17.78	Socketed
PC44	51	46	42	35	31	29	13.7	Socketed
PC68	46	42	38	31	28	26	9.3	Socketed
PC84	41	33	28	25	21	17	5.3	Socketed
PD8	82	79	73	60	54	50	22.2	Socketed
PD48	43.2	43.2	43.2	32.57	29.14	27.20	11.6	Socketed
PG84	37	34	31	24	18	16	5.8	Socketed
PG120	32	27	25	19	15	13	3.6	Socketed
PG132	32	28	24	20	17	15	2.8	Socketed
PG156	25	23	21	15	11	10	2.6	Socketed
PG175	25	23	20	14	11	10	2.6	Socketed
PG191	24	21	18	15	12	11	1.5	Socketed
PG223	24	20	18	15	12	11	1.5	Socketed
PG299	18	17	16	10	9	8	1.9	Socketed
PG411	16	15	14	9	8	7	1.2	Socketed
PG475	14	13	12	9	8	7	1.2	Socketed
PG559	-	12	-	-	-	-	-	Estimated
PP132	35	34	33	23	18	17	6.0	Socketed
PP175	29	29	28	19	15	13	2.5	Socketed
PQ44	52.17	51.34	50.05	39.82	36.38	35.35	12.40	4L/2P-SMT
PQ100	35	33	32	29	28	27	5.5	4L/2P-SMT
PQ160	37	32	22	24	21	20	4.6	2L/0P-SMT
PQ208	25	32	26	23	21	19	4.3	2L/0P-SMT
PQ240	28	23	19	17	15	14	2.8	2L/0P-SMT
PQ304	11	11	10	7	5	5	0.9	4L/2P-SMT
SO8	147	147	147	112	1.0	98	48.3	IEEE-(Ref)
SO20	86	86	86	65.36	61.06	57.62	3.6	Vendor data

SO24	80	80	80	60.8	56.8	53.6	28	Vendor data
TQ100	37	31	31	26	24	23	7.5	4L/2P-SMT
TQ128	31.45	30.52	29.98	26.94	25.18	24.33	5.34	4L/2P-SMT
TQ144	35	32	30	25	21	20	5.3	4L/2P-SMT
TQ176	29	28	27	21	18	17	5.3	4L/2P-SMT
VO8	162	162	162	123	116	108	48.3	Estimated
VQ44	44	44	44	36	34	33	8.2	4L/2P-SMT
VQ64	44	41	39	34	32	31	8.2	4L/2P-SMT
VQ100	47	38	32	32	30	29	9.0	4L/2P-SMT
WC44	46.5	46.5	46.5	3	31	25	7.4	Socketed on 2L/0P
WC84	40	40	40	28.5	23	21	4	Socketed on 2L/0P