Reducing CPLD Power Consumption

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Power usage in CMOS circuits appears to be straightforward, yet it is often deceptive. This article will help you understand CPLD power dissipation and will give you some guidelines for minimizing power consumption.

Most vendors provide a table or an equation that specifies the various components of power dissipation for a CMOS part, as shown in **Figure 1**. Typically, these include:

- A component for the input receivers, which must be de-rated if driven from TTL rather than CMOS external drivers.
- A component for the internal core of the chip, which usually has a negligible DC component
- An AC component that requires detailed knowledge of the various switching frequencies encountered. It also requires knowledge of exactly how much circuitry is used or unused at any time.
- A component attributed to the output stages which are functions of both the switching frequencies as well as the external load capacitance.

The power is found as the sum of all components:

Power = $P_{IN} + P_{CORE} + P_{OUT}$ (AC and DC)

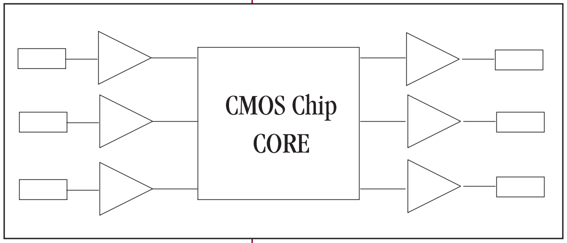

Figure 1: Power Components of a Typical CMOS Chip

This approach is intellectually satisfying, but usually you find that you have little knowledge of the load capacitance or various switching frequencies that your circuits create and encounter. You must resort to estimating the speed and loading parameters to obtain a power estimate. One estimate is often used as the basis for another, giving fuzzy, inaccurate results.

Because of the complexity of arriving at a simple number, many CPLD vendors have resorted to simplifying the power estimation process by providing a single equation. Frequently, when misused, this results in optimistic values. Often, calculation constants are introduced to simplify the process, but no limitation guidelines or explanation of their meaning is given.

Power Dissipation Factors

The basic structure of a CPLD differs from other CMOS devices primarily in its programmable internal core. If **Figure 1** was modified to insert a programmable AND array structure into the core, most of the power differences between a CPLD and other CMOS chips would be explained. Input power must be accounted for, as well as output power, but the core power is different, due to the CPLD sense amplifier approach.

Figure 2 shows a simplified structure for a programmable "AND" gate (actually, it is a NOR internally) which performs the programmable logic operations. It shows three transistors with floating gates that form a "Wired NOR" when appropriately programmed. XC9500XL devices normally have 108 transistors attached to the Bitline for each product term. The pullup and pulldown resistors (R1 and R2) attached to the Bitline are actually transistors.

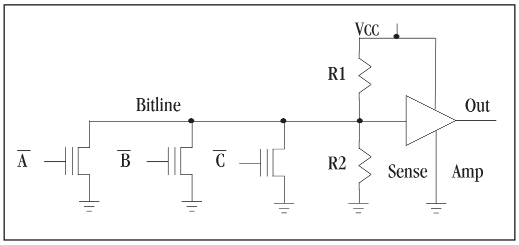

Figure 2: Simplified CPLD Programmable Structure

When the Bitline is High (exceeding the trip voltage of the sense amplifier), the output switches. Otherwise, the output remains Low. From a power dissipation viewpoint, lower consumption occurs when $V_{bitline\_hi}$ is driven onto the bitline. Because CPLDs are comprised of macrocells that include flip-flops, it is important to realize that the flip-flops consume negligible power compared to the pro-

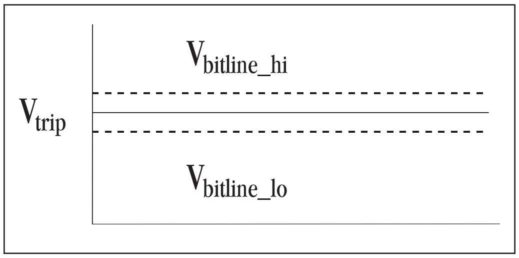

Figure 3: Trip Voltage, Bitline High and Bitline Low Relationships

grammable cells. With that in mind, a CPLD design can be viewed as being a collection of product terms driving pins and flip-flops. The switching speed of the product terms and output pins becomes the dominant factor in most cases.

There is a component of current always present in the standard CPLD programmable structure. The current will be typically one of two values passing either through R2 or through the transistors to ground. This is the primary factor contributing to DC current consumption in the CPLD core. It cannot be ignored.

R1 in **Figure 2** is actually a programmable transistor structure. R1 can be programmed to supply current to the Sense Amp input node to select between a fast ramping input signal, or a low current slower ramping signal. **Table 1** gives relative values of the current drawn by a product term depending on the value of R1 and the condition of the Bitline.

Table 1 indicates several things:

- Each product term can have several different static current values.
- The range is large (10X).
- The value is a strong function of whether the product term is driving High or Low.

For combinatorial designs, where all product term inputs are directly driven from the input pins, this is easily accounted for and an accurate static power estimation can be measured. For sequential circuits, the binary values of flip-flops will be attached to the various product terms, so it is difficult to know what the power consumption is unless careful analysis includes the state of the circuit in the estimation.

In **Figure 4**, consider the case where Input 1 and Input 2 are both logical ones. If the state variable feeds back a logical one, the Bitlines will both be High. However, if the State variable feedsback a logical zero, both Bitlines will be Low and draw significantly more current. This means that system reset may draw the highest current. Frequently, this behavior is seen when you attempt to measure accurate power when the clock is stopped. **Figure 5** gives an example of how this creates an ambiguous measurement.

As shown in **Figure 5**, there exists an ambiguous region for ICC when the switching frequency is very near DC. This is because the exact state of the sequential machine will dictate just how many specific bitlines are High or Low when the clock is turned off (or very slowly switching). Very quickly after the frequency rises, the ICC assumes a much more linear relationship with frequency. Although counter-intuitive, it is possible for a short frequency range to have ICC drop as frequency rises.

Table 1: Relative Product Term Currents

R1 Configuration	Bitline = High	Bitline = Low
High Speed	0.5I	1.0I
Low Power	0.1I	0.5I

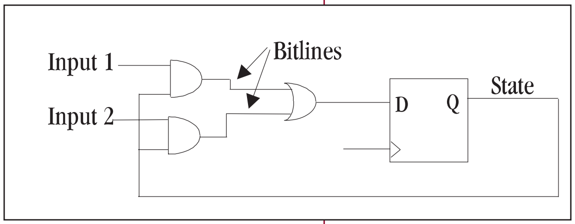

Figure 4: State Influence on CPLD Power

Power Minimization Techniques

The following checklist will help you dramatically lower power consumption:

- **Minimize HP macrocells** - By carefully selecting only those macrocells that need to be in high speed mode, others can be set into low power mode, which will reduce power.
- **Use global resources** - Product term clocks, 3-states, and set/resets may increase s-term current draw.
- **Set VCCIO to 2.5V** - Restricting the voltage swing of the output stage will lower the CV ^{2}f portion of the output power consumed.
- **Attach unused XC9500 input pins to a UPG** - Unused pins should not float. One easy way to do this is to use the User Programmable Ground Option (UPG), which drives the pins Low and gives additional noise immunity. (XC9500 devices have bus-hold circuitry that automatically sets input pins to a known state.)

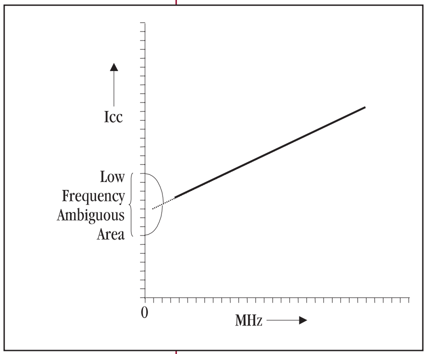

Figure 5: I_{CC} VS Frequency

Conclusion

The general ideas discussed here are applicable to most manufacturers' CPLDs, but in particular to both the Xilinx XC9500 and XC9500XL CPLDs. Xilinx CPLDs offer abundant options to substantially reduce power dissipation and still provide high performance.