New Configuration Options for Virtex-II Pro

Configure Virtex-II Pro FPGAs – and load embedded processor software – using the System ACE pre-engineered configuration solutions.

by Frank L. Toth
Marketing Manager, Configuration Solutions Division
Xilinx Inc.
frank.toth@xilinx.com

Xilinx offers a variety of System ACE™ configuration options to meet a wide range of configuration speeds, densities (bitstream size), and costs, as shown in Table 1. These pre-engineered solutions simplify the configuration of our FPGAs and help you get your design to market as quickly as possible.

The System ACE CF solution, shown in Figure 1, leverages the tremendous density of commercial compact flash memory devices to give you the benefit of industry-wide increases in speed and density. When power is applied, the System ACE CF solution uses the JTAG port to configure the Virtex-II Pro™ fabric and the embedded processor, as shown in Figure 2. Virtex-II Pro FPGAs can also be easily accessed by the Xilinx ChipScope™ debugging tools using this same JTAG port.

The System ACE CF solution uses the industry standard FAT file management system, which enables you to manage both bitstream and software files like disk space. Multiple configuration bitstreams can be selected and managed under software and hardware control. Built In Self Test (BIST) files at the system level can be loaded and used to reconfigure the FPGAs to perform system-level I/O, network communication, functionality, and memory tests. Then the FPGA can be reconfigured for the mission mode.

Built-in Configuration Controller

In a system with a Virtex-II Pro device along with other Virtex™ and Spartan™-II FPGAs, the Virtex-II Pro device may be configured first. Then the embedded processor can be used as a configuration controller eliminating the need for a separate processor. The Virtex-II Pro FPGA

	System ACE CF (Compact Flash)	System ACE MPM (AMD Standard Flash)
Multiple Designs	no limit	up to eight
S/W Storage	Yes	No
Removable	Yes	No
IRL Hooks	Yes	Yes
Density	128Mbit - 8Gbit	16-64Mbit
Performance	~30Mbit/sec	152 Mbit/sec
#Components	2	1
Min. Board Space	~(50mm x 50mm)	~(35mm x 35mm)
Space/bit	32-256 Mbit/sq. in.	8-32 Mbit/sq. in.

Table 1 - System ACE configuration options

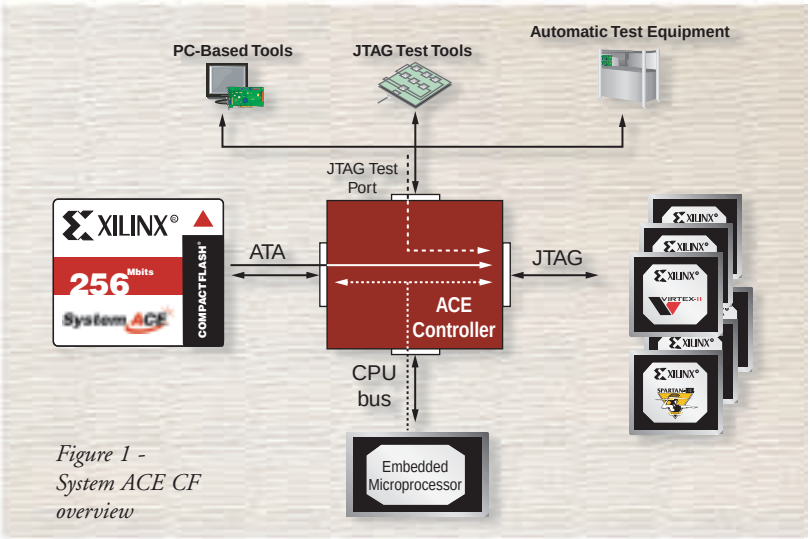

Figure 1 - System ACE CF overview

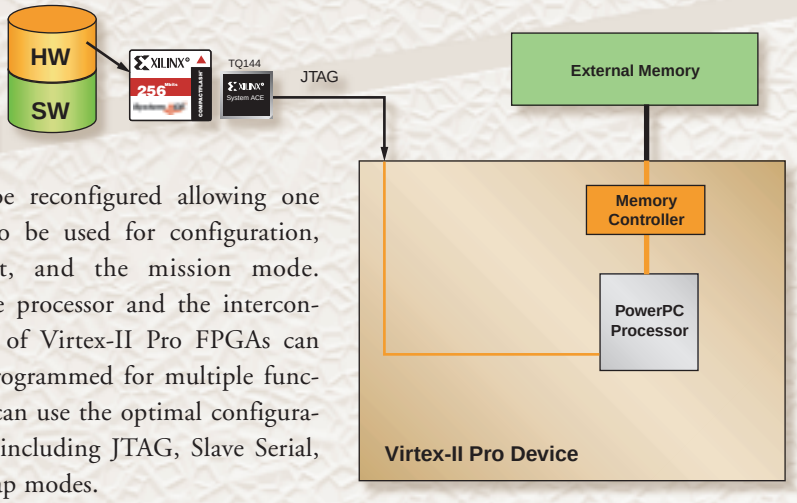

Figure 2 - Configuration via JTAG port

can then be reconfigured allowing one processor to be used for configuration, system test, and the mission mode. Because the processor and the interconnect fabric of Virtex-II Pro FPGAs can easily be programmed for multiple functions, you can use the optimal configuration mode including JTAG, Slave Serial, or SelectMap modes.

As an alternative configuration sequence, the Virtex-II Pro FPGA can be "booted," as shown in Figure 3, using a smaller boot file provided by the System ACE solution on power up. The embedded processor can then take control of the configuration process and in turn configure itself and the rest of the system by sending the appropriate interface and control signals to the System ACE solution.

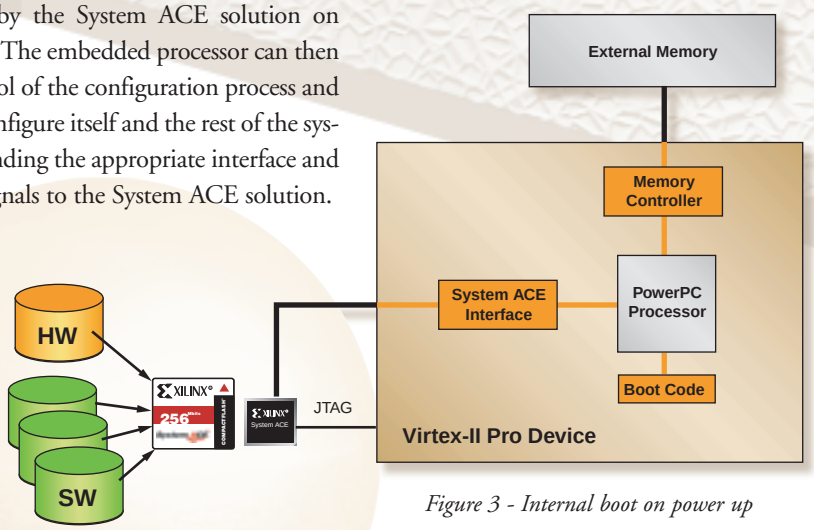

Figure 3 - Internal boot on power up

Other Configuration Options

Xilinx also offers several other pre-engineered configuration solutions including serial PROMs, the System ACE MPM (Multi-Package Module, shown in Figure 4) and the System ACE SC (Soft Controller). The density of the System ACE MPM solution ranges from 16 to 64 megabits (or more by using the System ACE bitstream compression software) and features a Slave Serial or Select Map configuration port output. The native flash/microprocessor interface allows the System ACE MPM solution to be connected to the microprocessor bus.

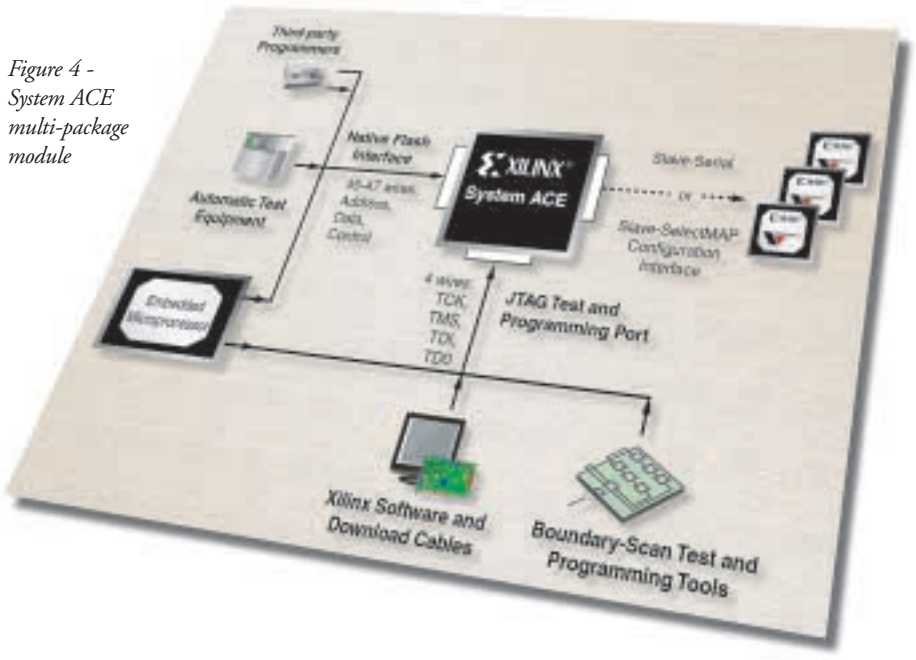

Figure 4 - System ACE multi-package module

If you want to use a different form factor and mount the components directly on the board, the System ACE Soft Controller IP is available. This pre-engineered solution is identical in functionality to the System ACE MPM solution and you can download the IP free of charge.

Taking Full Advantage of System Re-Configurability

With the advent of the embedded processor and the other system-level features of the Virtex-II Pro family, the use of multiple configurations becomes more useful, both to increase system flexibility and extend product life. Multiple configuration files can also be used as a vehicle for loading BIST and for testing system functionality, integrity, and performance.

Conclusion

With the Xilinx System ACE solutions, you can easily control both the configuration of your FPGAs and automatically load your embedded processor software. There is no easier way to configure your Virtex-II Pro designs.

For more information on System ACE products, go to: *www.xilinx.com/xlnx/xil_prodcat_product.jsp?title=system_ace*