Use Virtex FPGAs and Xilinx Software Tools to Reduce Line Echoes in PSTN and Packet Networks

By using Xilinx software and Virtex FPGAs with DSP capabilities, eInfochips Ltd. brought its line-echo canceller to market faster and better than a traditional DSP chip solution.

by Nilesh Ranpura
Project Manager, ASIC Group
eInfochips ltd
nilesh@einfochips.com

Line echoes occur in public switched telephone networks (PSTN) at so-called "hybrid" points, where 2-wire and 4-wire copper lines are interconnected at the central office. Due to electric current leakage in the hybrid, a part of the signal energy is reflected back to the source of the signal, which causes an echo on the phone line. Likewise, in packet networks, the delays associated with processing the voice stream can also produce an echo on the line.

At eInfochips Ltd., we have developed an echo canceller using Virtex™ FPGAs. We chose Virtex devices because they give us high-speed performance and an edge in area-to-cost ratio over traditional ASIC solutions.

Echo cancellers are advanced signal processing algorithms running on DSPs or fixed-function ASICs that remove line echoes in voice networks. An adaptive FIR filter is used to predict the echo from the history of the transmitted signal.

Echo cancellers can be integrated into a phone system or packet network along with other voice-processing functions, such as subtracter, double-talk detector, nonlinear processor, narrow band signal detector, PCM encoder/decoder, offset null filter, and controller/processor interface, as shown in Figure 1.

Virtex FPGAs: The Obvious Choice

We started our project with the goal of creating a single-channel echo canceller capable of handling an echo tail length of 128 ms. We had the option of using a DSP chip for algorithm implementation, but during the course of development, we discovered we could deploy a Virtex FPGA-based solution with DSP capabilities to achieve echo cancellation of up to 128 ms.

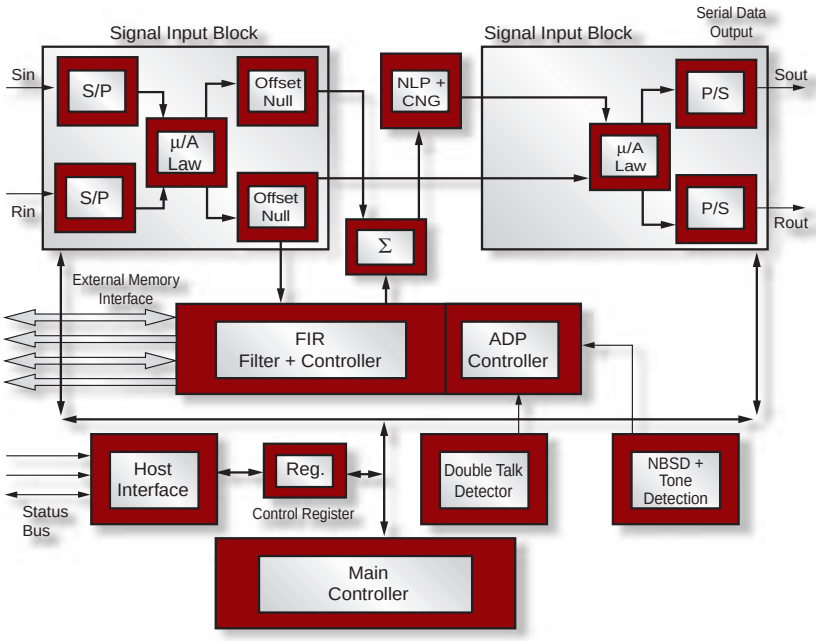

Figure 1 - Echo canceller logic block diagram

The choice was obvious. Not only do Virtex FPGAs have high-speed digital signal processing functions, but they also include extensive flexibility in using block RAM and LUTs as RAM and ROM.

We implemented the following major blocks as a part of the data path design in the FPGA:

- Adaptive FIR filter for estimating the echo signal
- Programmable double-talk detection threshold
- Nonlinear processor with adaptive suppression threshold for removing the residual echo signals
- Offset null filtering of PCM channels
- Narrow band signal detector conforming to ITU-T G.165 requirements for preventing the divergence of the adaptive filter coefficients
- Selectable μ/A law companding, PCM coding, and sign magnitude.

The core was verified using Industry Standard Vectors compliant with the G.165 standard.

Conclusion

Xilinx Virtex FPGAs support high density and speed with extensive EDA tools support on a wide spectrum of features. The combined solution of Virtex hardware (in this case, the Virtex XCV800 FPGA), associated Xilinx Foundation™ Series software, and the Xilinx ChipScope™ integrated logic analysis tool saved us invaluable time to market.

As a result, of implementing a total Xilinx Virtex solution, we were able to be among the first to bring our echo canceller solution into the emerging areas of Internet gateway, ATM gateway, XDSL technology, cable modem, and wireless telephony. For more information visit *www.einfochips.com* or write *info@einfochips.com.*