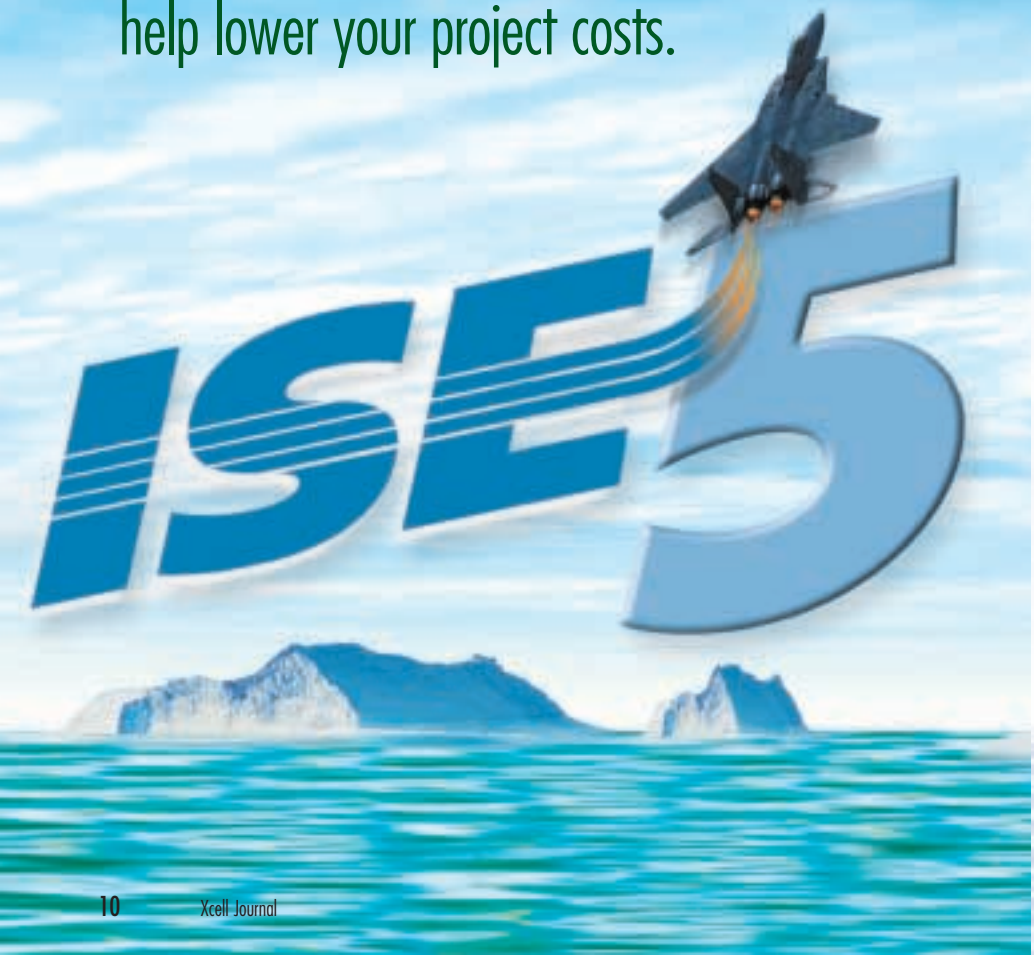
The New ISE 5.1i Software

Efficient design methodologies help lower your project costs.



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As the economic downturn drags on, the pressures are now greater than ever before to lower your project costs. ISE 5.1i, the latest release of our design software, offers a number of productivity technologies that shorten your logic design flow, freeze design results, shorten implementation and verification cycles, and provide interactive design assistance – while at the same time enabling you to realize even faster design performance. The end result to you is cost savings across your entire project.

ISE 5.1i, released this past August, delivers all the potential of the leading-edge Xilinx programmable device families by incorporating methodologies that reduce logic design bottlenecks. Built on the ProActive Timing Closure technology introduced in ISE 4.1i last year, ISE 5.1i gives you:

- Designs with 15% higher-performance (2x faster than ISE 4.1i) – allowing the use of slower devices to achieve a cost savings of at least one device speed grade
- PACE (Pinout and Area Constraints Editor) – a graphical pin assignment and area editing tool
- Incremental Design to lower design recompile times
- Macro Builder to freeze performance for design reuse
- Architecture Wizards for fast and easy programming of advanced device features
- ChipScope Pro™ 5.1i for on-chip, real-time debugging.

Xilinx continues to deliver the fastest design performance available anywhere in the PLD industry. Internal benchmark data shows that ISE, coupled with Virtex-II Pro™ FPGAs, is 30 % faster than any competing PLD design solution. Higher performance from ISE means you hit your design target faster and earlier than with any other PLD software – and spend less time reaching design closure.

PACE – Pinout and Area Constraints Editor

ISE 5.1i includes the new Pinout and Area Constraints Editor tool (PACE), delivering new functionality to pin and area management in an easy-to-use, graphical environment. PACE helps speed you through the design flow by streamlining a difficult and time-consuming process.

Pin Management Made Easy

PACE includes graphical pin management that is both powerful and easy to use. You can drag-and-drop pin assignments onto a graphical map of the device, group pins logically and by color-coding for easy recognition, specify I/O standards and banks, prohibit I/O locations, and verify legal pin assignments using the built-in design rules-checking. You can assign and place differential I/Os, and much more. Even as devices grow larger, PACE brings a new level of ease to the difficult task of assigning and verifying your design pins, and quickly moves you forward in the design flow.

Area Definition Moves Forward in the Design Flow

Because PACE uses the Native Generic Database (NGD) file, it can be used in the design flow from the very beginning of the design process. PACE allows you to edit both location and area constraints, define logic areas graphically, and display I/Os on the periphery for connectivity checking. PACE also allows area mapping by examining the defined HDL hierarchy and checks logic areas against expected gate size, making area definitions quick, accurate, and easy.

Incremental Design – Minimizing the Impact of Design Changes

ISE 5.1i includes Incremental Design, a next-generation technology that shortens design recompile times and helps to minimize the time and cost impact of late-arriving design changes. With Incremental Design, you begin by using either PACE or the ISE Floorplanner to plan your design along hierarchical boundaries. The design process then proceeds as usual. Should a change then be required, Incremental Design ensures that only the area in question need be reimplemented. The rest of the design stays locked and intact. Incremental Design lets you use your project time where it's most needed: concentrating on verification, thoroughly testing a critical area of your project, or simply using your time savings to get to market faster.

Macro Builder

Built into the ISE 5.1i Floorplanner is a new feature that allows you to build and save "macros," or blocks of logic, to be reused in a later design. Once a design has been floorplanned and placed, you can execute the "write RPM to NCF" command within the ISE Floorplanner. This saves both the design EDIF (Electronic Design Interchange Format) file and placement information. The new macro, including relative placement information, can then be reused in a future design. Macro Builder lets you leverage your existing investment in HDL development and delivers excellent performance every time; and during project downtime, your engineers can be developing HDL code for later use.

Architecture Wizards

Each new hardware capability released in a Xilinx device family results in an associated learning curve for you. As a designer, you must learn all the programming attributes necessary to make the best use of those new features.

ISE 5.1i includes new Architecture Wizards that help you quickly and easily program both the Digital Clock Manager (DCM) in Virtex™-II and Virtex-II Pro FPGAs, and the 3.125 Gigabit Multi-Gigabit Transceiver (MGT) RocketIO™ pins in Virtex-II Pro devices.

The Architecture Wizards provide a simple, graphics-based way to specify the device feature. By setting dialog box switches appropriately according to the way the device is to be used, HDL code is output in either VHDL or Verilog format for use in the design source files. The Architecture Wizard is great for the first-time designer, for designers new to Virtex-II and Virtex-II Pro devices, or to speed you through device setup, enabling everyone to make the best use of feature-rich device capabilities.

Unsurpassed On-Chip Real-Time Debugging

Released in October, the new ChipScope Pro 5.1i debugging and verification software takes on-chip verification to new levels. ChipScope Pro includes all the functionality of the ChipScope ILA release, plus new enhancements that support even greater debugging potential. These include a new IBA (Integrated Bus Analysis) core that supports debugging of the IBM CoreConnect™ bus (for the Virtex-II Pro IBM PowerPC™ 405 processors); enhancements for logic analysis; and CORE Generator™ and Core Inserter tools for placing the necessary cores into either the HDL source or directly into the design netlist.

The new Agilent Trace Core (ATC), also included in the ChipScope Pro software, is a result of the pioneering relationship between Xilinx and Agilent, the leader in test and measurement equipment. The ATC core links FPGA debugging to the Agilent FPGA Trace Port Analyzer (available separately from Agilent). This test equipment/FPGA combination yields deeper trace debugging with ample sampling memory, more complex triggering options, and support for remote debugging over the Internet.

The combination of Virtex-II Pro devices, ChipScope Pro software, and ISE delivers the most powerful design and real-time debugging solution available, shortens verification cycles, and lowers associated project costs.

Conclusion

ISE continues to define the standard of logic design, concentrating on performance and productivity. ISE delivers the time efficiency demanded by today's high-pressure design environments, and helps you get the highest performance from your logic devices. Go to *www.xilinx.com/xcell_ise* to find out more about ISE 5.1i. To get your copy of ISE 5.1i today, contact your local sales office.