ISE Delivers a Spectrum of High-Density Solutions for Completing Large Designs

Manage multimillion-gate designs with ISE 5.1i — the latest suite of design tools from Xilinx.

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As logic design sizes now routinely exceed 1 million gates, new pressures unique to high-density designs are being felt by logic engineers worldwide. ISE (Integrated Software Environment) from Xilinx is responding with a spectrum of technology for larger designs, including Incremental Design, available in ISE 5.1i. These technologies augment the larger design flow with "divide and conquer," and performance-locking strategies that help bring large, daunting projects under control.

Area Groups – Quick-and-Easy

Area groups is a quick-and-easy way to bring a measure of control to your project. Engineers can map areas of logic for the target FPGA using either the new PACE tool (Pinout and Area Constraints Editor) in ISE 5.1i, or the ISE Floorplanner. PACE lets you create area maps around hierarchical HDL boundaries automatically, or let PACE give area estimates for target logic that you can either use or modify and draw by hand. Figure 1 demonstrates PACE being used to define a logic area.

Defining area groups delivers many design advantages. First, and most simply put, being able to "see" the different areas of logic can help delineate regions where different design entry methods are being used, partition out areas for design reuse or IP placement, or point out where the "known problem" areas of the design will occur. But defining area groups also offers technical advantages as well. Most important, area planning the design correctly can accelerate timing closure by keeping critical logic cells and paths together, and by minimizing the number of interface ports between modules.

Using area groups is a good and fast methodology to help gain some advantage over a large design, but area groups do not provide control over design changes.

Incremental Design – Change Without Risk

In the middle of the high-density technology spectrum is a new capability called Incremental Design, available at no cost in ISE 5.1i. Incremental Design combines the quick-and-easy aspects of area groups with performance-locking, to offer a measure of immunity to late-cycle design changes.

With Incremental Design, engineers can use PACE to assign area groups along hierarchical HDL boundaries, as previously discussed. The overall design is then completed as usual. Should a design change occur after or close to completion – Incremental Design guarantees that only the area that needs to change has to be re-implemented. The remainder of the design stays locked and intact.

Incremental Design reduces the overall design re-compilation time by focusing the implementation cycle on the module that needs to change. During debug and verification this speedup offers a number of advantages; including more debug iterations possible, faster overall verification cycles, and allowing engineers to focus on the real design problems rather than recompiling the entire design over and over.

Incremental Design also delivers faster design completion when late design changes must occur. A recent informal survey of Xilinx customers indicated that every one of their logic design projects underway in 2001 had at least one late-cycle design change that occurred after design freeze, negatively affecting the overall completion date. Incremental Design delivers an overall completion advantage for this common problem, and can help with large and midrange design sizes as well.

Modular Design – Divide and Conquer Management

At the high end of the high-density spectrum is Modular Design, an optional team design technology that can be purchased and then added to your ISE software environment. Modular Design implements a "divide and conquer" approach for corporate environments that deploy teams of engineers on large designs.

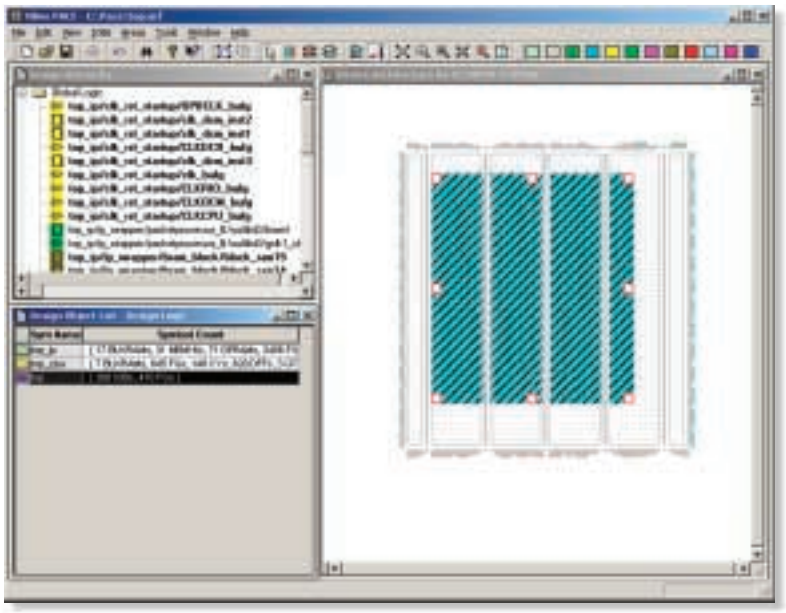

Figure 1 - PACE Area Management

Modular Design requires the design manager to plan the larger design ahead of time, based on knowledge of which engineers will be assigned to each portion of the design. The design manager can then use the ISE Floorplanner to partition the overall larger design into smaller "modules," which are then implemented independently. All of the ISE design tools and flows can be brought to bear on the smaller modules individually and in parallel. Engineers are focused solely on the smaller and more direct task of completing just their respective modules. Once a module is finished, its place and route results are locked while the manager waits for all modules to be completed.

Modular Design delivers full planning control and faster project completion over the larger design, implementing a true bottoms-up design approach that completes the larger design via smaller modules implemented in parallel.

Macro Builder – Locked Performance

Also included in ISE 5.1i, the new Macro Builder function lets you generate design macros for saving your design away. Using ISE Floorplanner on a design that has been placed, the "write RPM to NCF" command saves away the placed floorplan along with the design file. This new macro, including relative placement information, can now be registered with your IP cataloging tool and then reused in later designs. Macro Builder helps corporate environments leverage their HDL development, reduces overall costs for future designs, and lets you save away "known-good" designs.

In this tight economy, Macro Builder helps managers make more efficient use of their HDL investments. When a new project is started, design time is saved by reusing proven functions, and not having to re-create design sections that previously worked before. And engineering resources can be utilized during project downtimes, to create modules for future use, starting the next project with an even greater completion time advantage.

High-density Design Made Easier

ISE 5.1i includes a spectrum of strategies that bring larger design sizes under control. From quick-and-easy area management to team-based "divide-and-conquer" methodologies, ISE offers technology that streamlines your high-density design process and works the way you expect it to. For more information on ISE 5.1i visit *www.xilinx.com/xcell_ise* and contact your local sales representative to order ISE 5.1i