

Agenda

◆ Introduction

- Market trend and application
 - 1394 Market Analysis Data
 - 1394 and industry
 - Applications

- 1394 Operation
- Bus Management
- Cable and Connection
- Architecture
- Topology

◆ Technology

- What is 1394?
- Why 1394?
- Applications
- 1394 Protocol
- PHY
- Link Layer
- Transaction Layer

◆ Other Technologies

- USB
- DVI

◆ 1394 In Home Networking

◆ Xilinx Value

◆ Alliances

◆ Summary



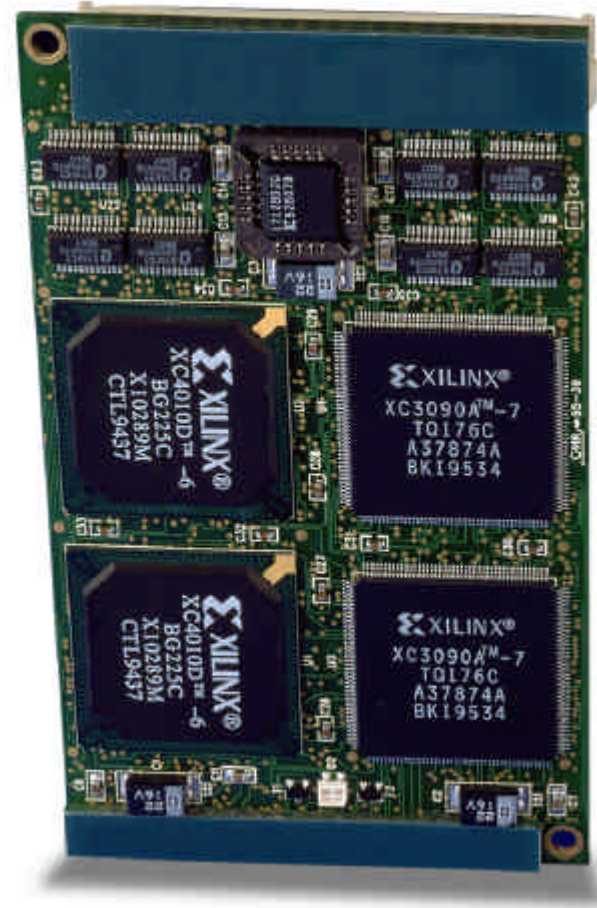
Introduction to Xilinx

Where Does Xilinx Fit In the Electronics Industry

Key components of an electronics system:

- ◆ Processor
- ◆ Memory
- ◆ *Logic*

Xilinx is the Leading Innovator of Complete Programmable Logic Solutions



Strategic Business Model Ensures Focus

- ◆ “Fabless” strategy
 - Leading edge IC process technology
 - Wafer capacity at competitive prices
 - Fastest, lowest cost, densest parts
- ◆ Independent sales organization (Reps & Distributors)
 - Sales is a variable cost
 - Permits greater reach—over 20,000 Customers
 - Over 10,000 “Feet On The Street”
- ◆ Focus on key strengths
 - Product design
 - Marketing
 - Applications & Technical Support

Xilinx Product Portfolio

Advanced Products Group



High Performance
High Density

General Products Division



High Volume
Low Cost

CPLD Division



Low Power
Low Cost

Software Solutions



IP Center



Alliance
CORE



XILINX
ONLINE
UPGRADABLE SYSTEMS



www.xilinx.com



Xilinx - Leader in Core Solutions

Base Level Functions	- 82xx, UARTs, DMA - 66MHz DRAM, SDRAM I/F - Memory blocks - 29xx - Proprietary RISC Processors	- 8051 - IEEE 1284 - 200MHz SDRAM I/F - SGRAM, ZBTRAM I/F - Multi-channel DMA	- JAVA - Adv 32-bit RISC Processors - 64-bit RISC - DDR/QDR RAM - 622 Mbps LVDS	- 128-bit processors - Reconfigurable processors
Communication & Networking	- Cell assem/delin - CRC - T1 Framer - HDLC - Reed-Solomon - Viterbi - UTOPIA	- 10/100 Ethernet - ATM/IP Over SONET - Cell scram/descram - SONET OC3/12 - ADPCM - IMA	- Network processors - 1Gb Ethernet - SONET OC48/192 - CELP - VoIP - ADSL, HDSL, xDSL - UMTS, wCDMA	- Software Radio - Modems - Neural networking - Emerging Telecom and Networking Standards
DSP Functions	- Basic Math - Correlators - Filters: FIR, Comb - Multipliers - FFT, DFT - Sin/Cos	- DCT - Adaptive filters - Cordic - DES - DES - Divider - NCO - Satellite decoders	- MP3 - QAM - JPEG - Speech Recognition - DSP Processor I/Fs - Wavelet	- MPEG - DSP Functions > 200 MSPS - Programmable DSP Engines
Standard Bus Interfaces	- CAN - ISA PnP - I2C - PCI 32-bit - PCMCIA	- CardBus - FireWire - PCI 64-bit/66MHz - Compact PCI Hot-Swap - PC104 - VME	- AGP - PCI-X 133MHz	- InfiniBand - Emerging High-Speed Standard Interfaces

1998

1999

2000

2002

2004



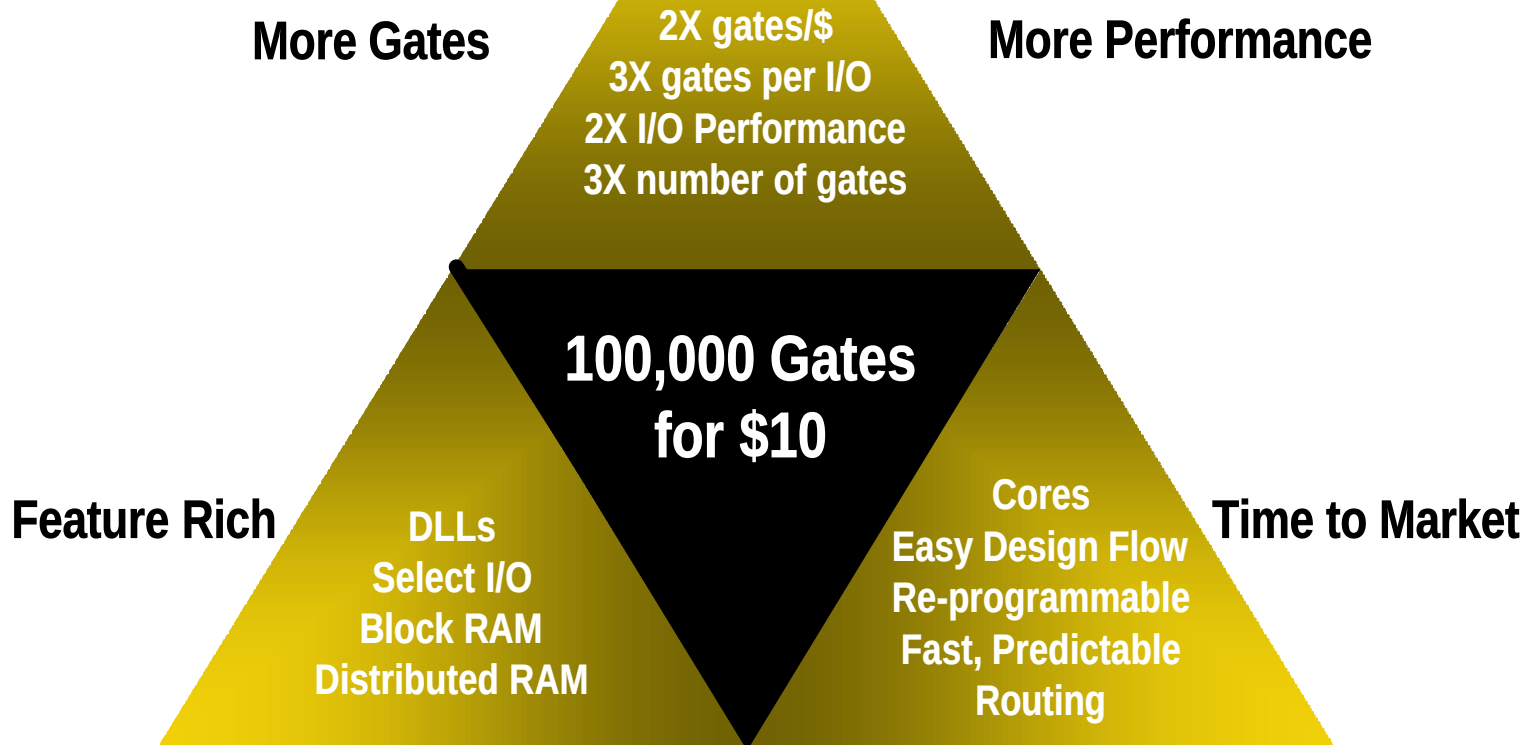
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Introducing the Spartan-II FPGA



Spartan-II: Extending the Spartan Series



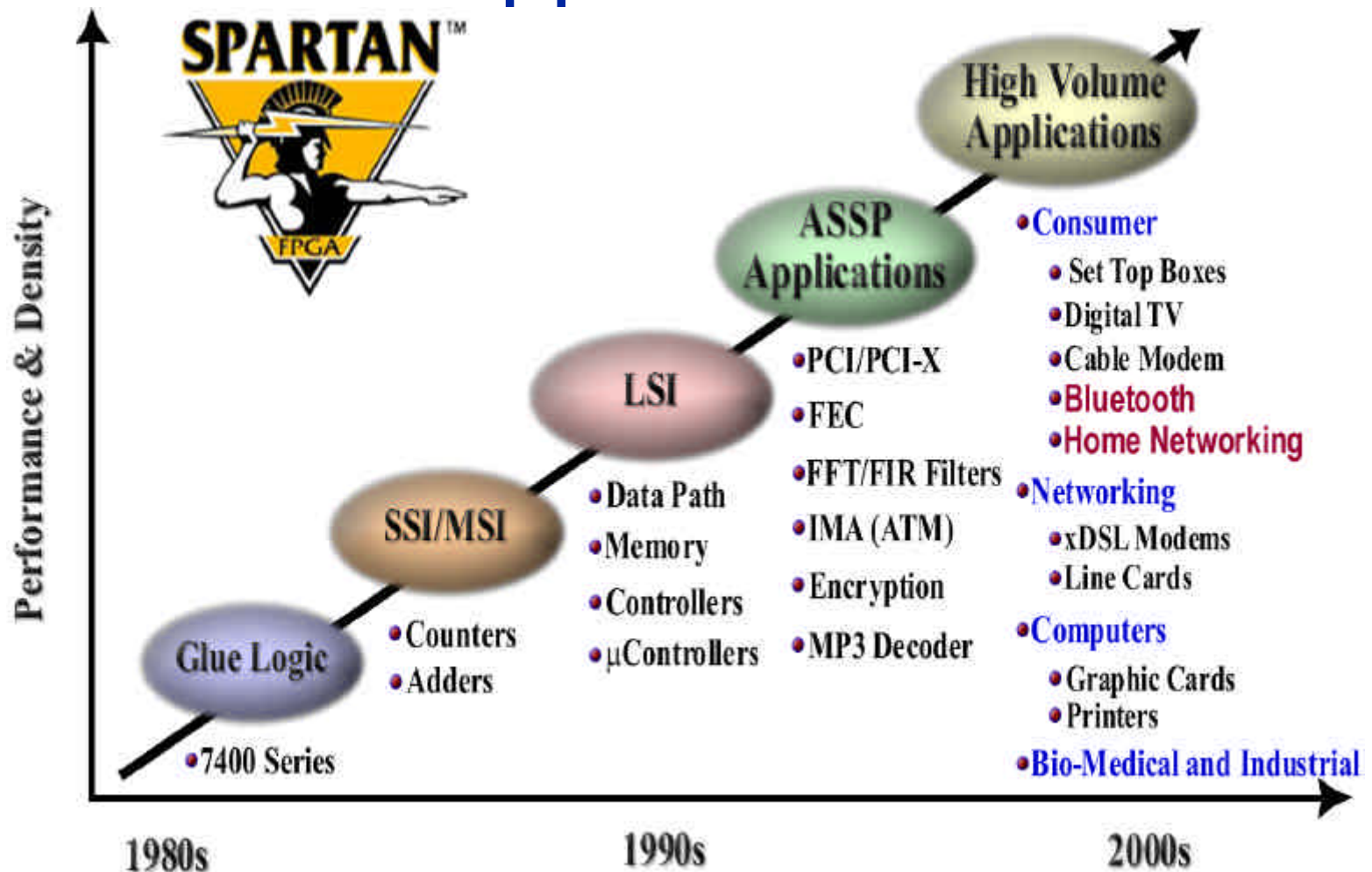
Programmable ASIC/ASSP Replacement!



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FPGA Application Trends



Programmable ASIC/ASSP Replacement!

Spartan-II - Architecture Overview

Delay Locked Loop (DLL)

Clock Management:
Multiply clock
Divide clock
De-skew clock

Configurable Logic Blocks (CLB)

Configurable Logic Block Array and Distributed RAM

Block Memory

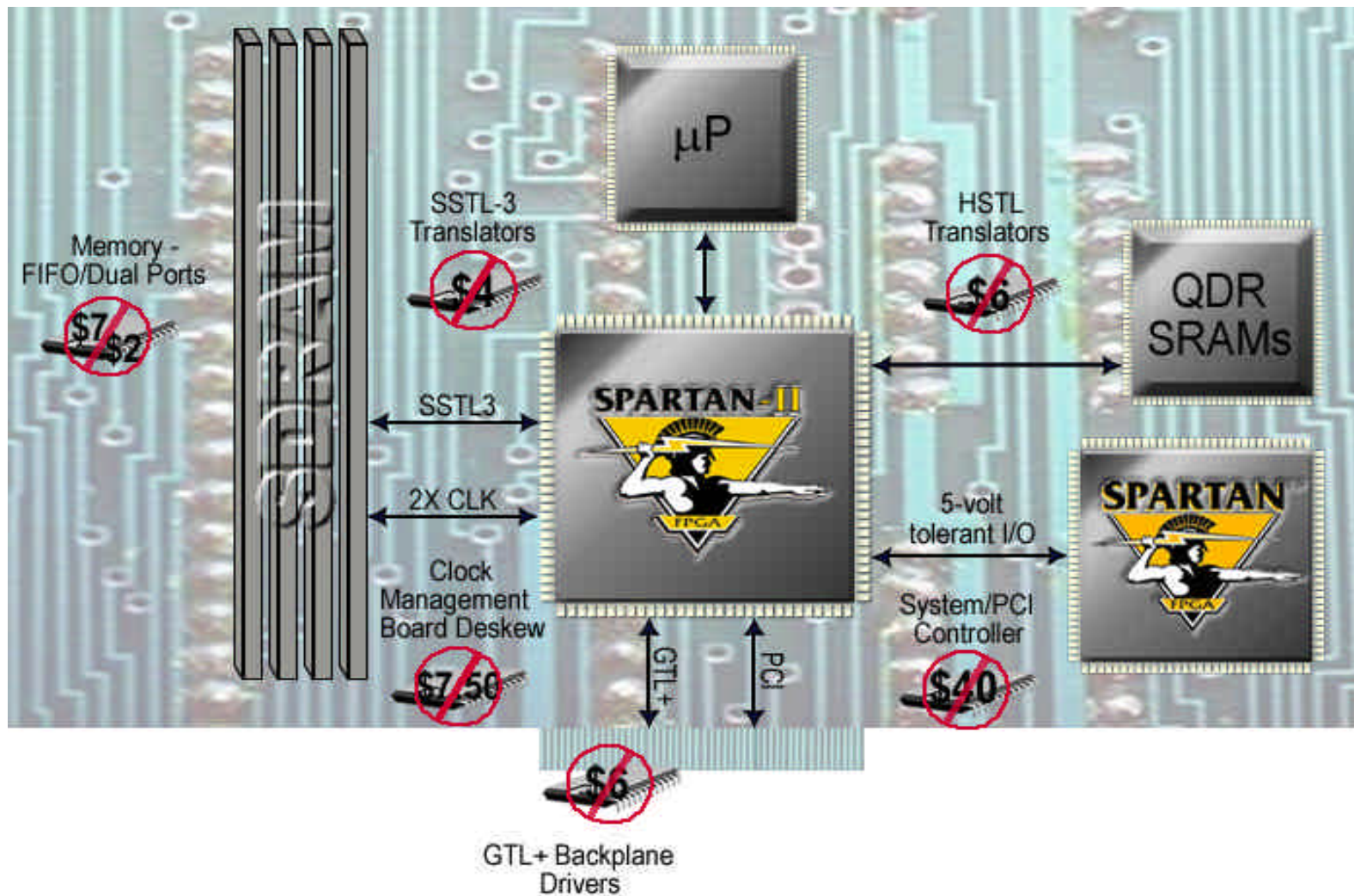
True Dual-Port™
4K bit RAM
4Kx1
2Kx2
1Kx4
512x8
256x16

Select I/O™ Technology

Chip to Backplane
PCI 33MHz 3.3V
PCI 33MHz 5.0V
PCI 66MHz 3.3V
GTL, GTL+, AGP
Chip to Memory
HSTL-I, HSTL-III
HSTL-IV
SSTL3-I, SSTL3-II
SSTL2-I, SSTL2-II
CTT
Chip to Chip
LVTTL, LVCMOS

"The Spartan-II family, in our opinion, may be the closest that any FPGA has come to being at a low-enough price to compete against an ASIC"
--Dan Niles, Industry Analyst

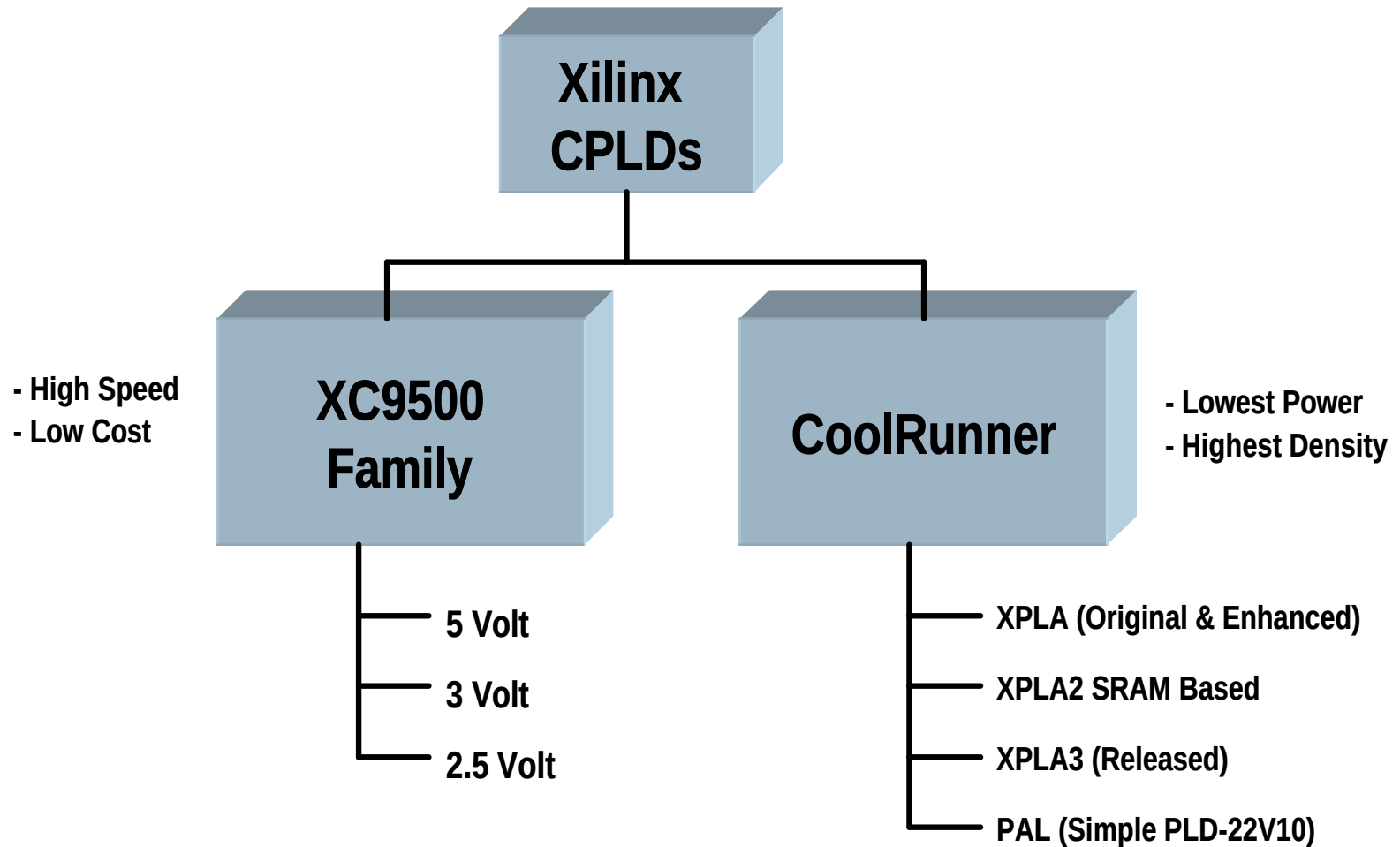
Spartan-II - System Integration



Spartan-II Core Support

- ◆ On-chip memory & storage
 - Distributed, BlockRAM, FIFOs
- ◆ Bus products
 - PCI (64- & 32-bit, 33/66MHz), Arbiter, CAN bus interface
- ◆ DSP Functions (FIR filter)
- ◆ Error correction
 - Reed-Solomon, Viterbi
- ◆ Encryption (DES & triple DES)
- ◆ Microprocessor
 - ARC 32-bit configurable RISC, 8-bit 8051 microcontroller
- ◆ Memory controllers (10+)
 - SDRAM, QDR SRAM
- ◆ Communications
 - ATM (IMA, UTOPIA), Fast Ethernet (MAC)
- ◆ Telecom
 - CDMA matched filter, HDLC, DVB satellite, ADPCM speech codec
- ◆ Video & image processing
 - JPEG codec, DCT/IDCT, color space converter
- ◆ UARTs

Xilinx CPLD Families



Spartan-II End Applications

◆ Consumer

- Set Top Boxes/Digital VCRs
- DTV/HDTV
- Digital Modems
 - xDSL, Cable, Satellite
- Home Networking products
- Bluetooth appliances
- LCD/Flat-Panel Displays

◆ Networking

- Telecom linecards
- DSLAMs
- LAN Hubs/Switches
- SOHO Routers
- Cellular base stations

◆ Computer/Storage

- Printer/Scanner
- Multi-function office equipment
- Storage devices
- Home servers
- Audio/Video add-in cards

◆ Industrial/Medical

- Medical Imaging
- Industrial automation/control
- Data acquisition
- Video capture/editing
- Automated test equipment
- Automotive Info-tainment systems

CoolRunner Technology

- ◆ Full density range 32 to 960 macrocells
- ◆ World's only TotalCMOS CPLD
 - Bipolar style sense amps eliminated
 - Virtually no static power dissipation
- ◆ Advanced PLA Architecture
 - Product term sharing (no redundant logic)
 - No wasted product terms
- ◆ 3.3v and 5.0v devices
- ◆ ISP/JTAG compatible & full software support

The CoolRunner Advantage



- ◆ Industry's lowest power CPLDs
 - Standby current $< 100\mu\text{A}$
 - High speed TPD = 6 ns
 - Revolutionary XPLA architecture
 - Exceptional routability & pin-locking
 - Fast, predictable timing
 - Small form factor packaging
 - New 0.5mm 56-pin MicroBGA

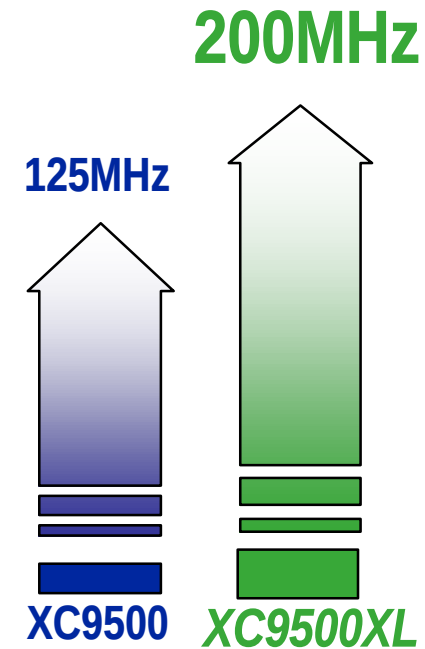


- ◆ No Speed / Power tradeoffs in scaling
 - Can build very large / very fast devices
 - 960 macrocell device @ 7.5 nsec t_{PD}



XC9500XL Key Features

- ◆ High performance
 - $t_{PD} = 5ns$, $f_{SYS} = 178MHz$
- ◆ 36 to 288 macrocell densities
- ◆ Lowest price, best value CPLD
- ◆ Highest programming reliability
- ◆ Most complete IEEE 1149.1 JTAG
- ◆ Space-efficient packaging, including chip scale pkg.



Lowest Price
Per Macrocell

XC9500XL/XV System Features

- ◆ I/O Flexibility
 - XL:5V tolerant; direct interface to 3.3V & 2.5V
 - XV:5V tolerant; direct interface to 3.3V, 2.5V & 1.8V
- ◆ Input hysteresis on all pins
- ◆ User programmable grounds
- ◆ Bus hold circuitry for simple bus interface
- ◆ Easy ATE integration for ISP & JTAG
 - Fast, concurrent programming times



System Block Diagrams for 1394 Solutions

Block Diagram Template / Index



Xilinx Solution



Or



Peripheral Components



Memory



Mixed Signal / RF / Analog Component

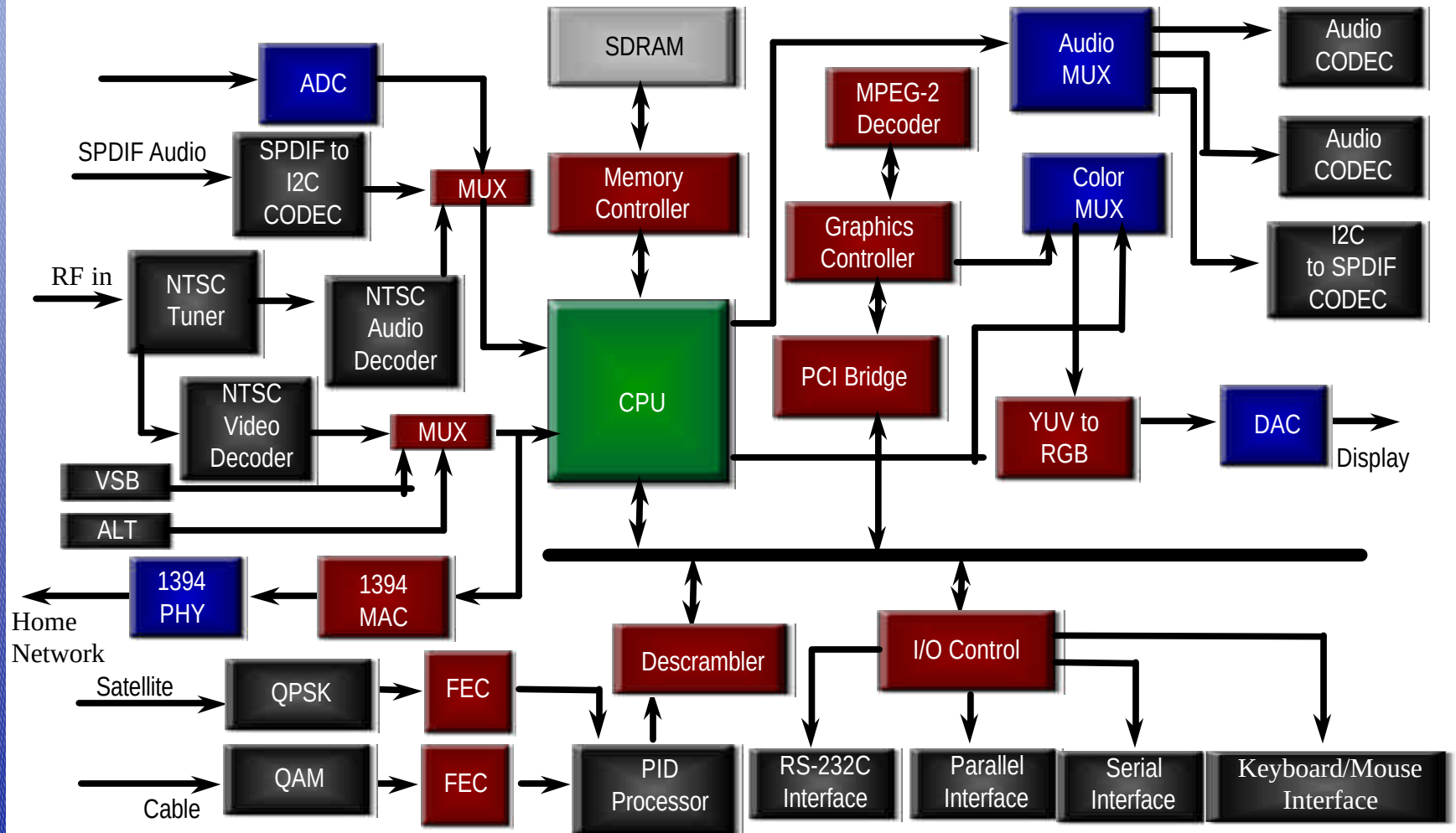


mP/ mC

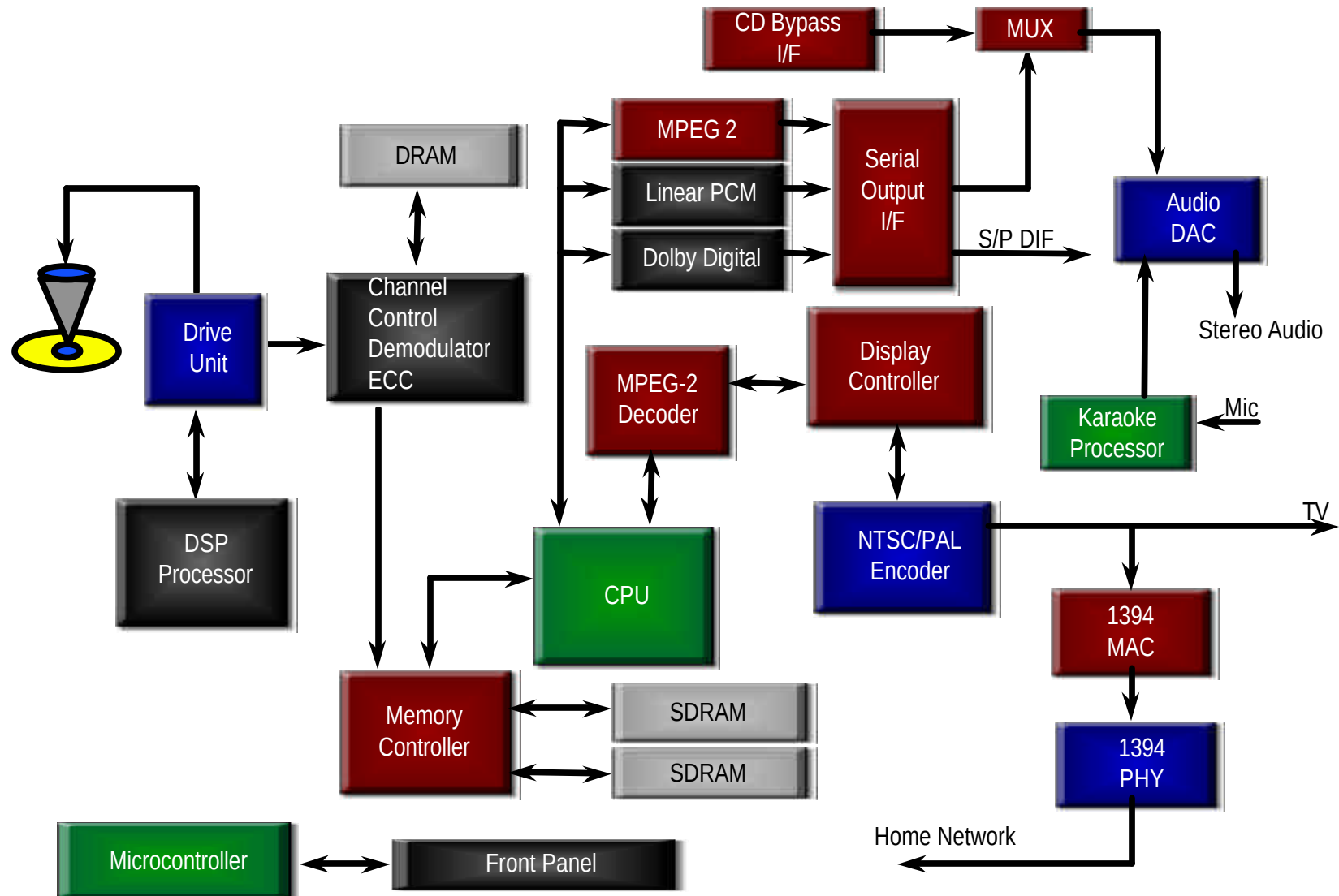


Embedded Chip/ ASSP

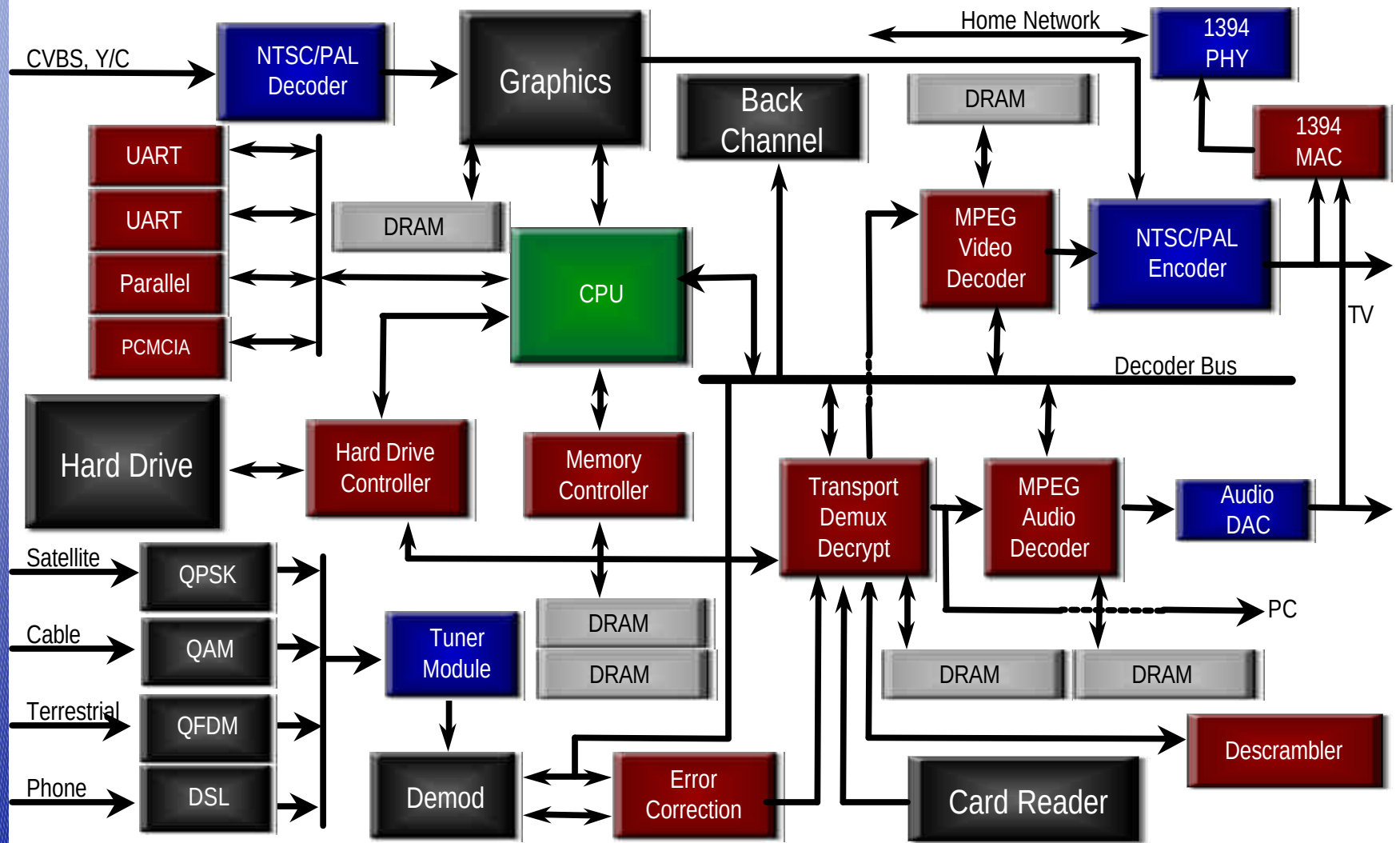
Digital TV



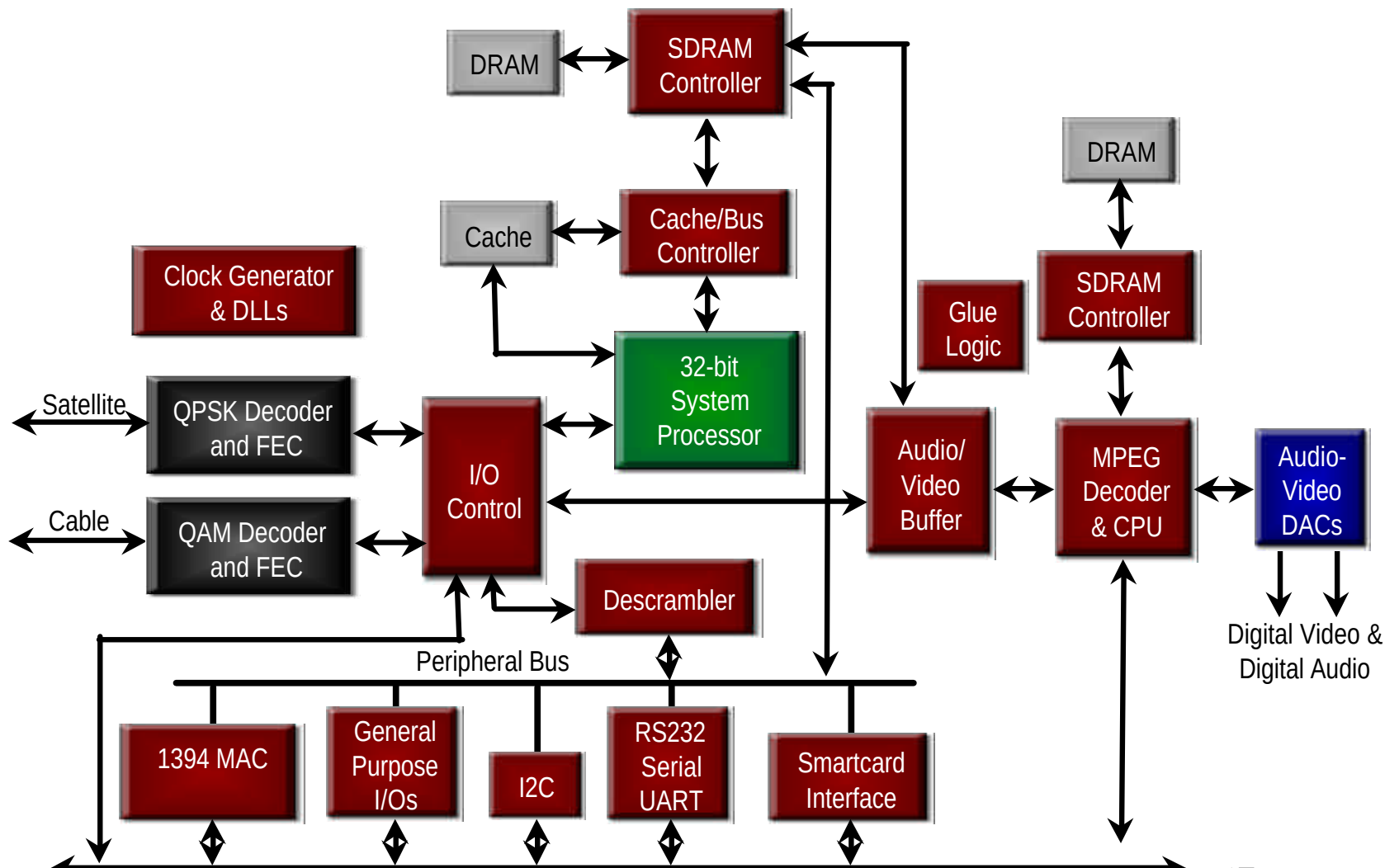
Interactive DVD Player



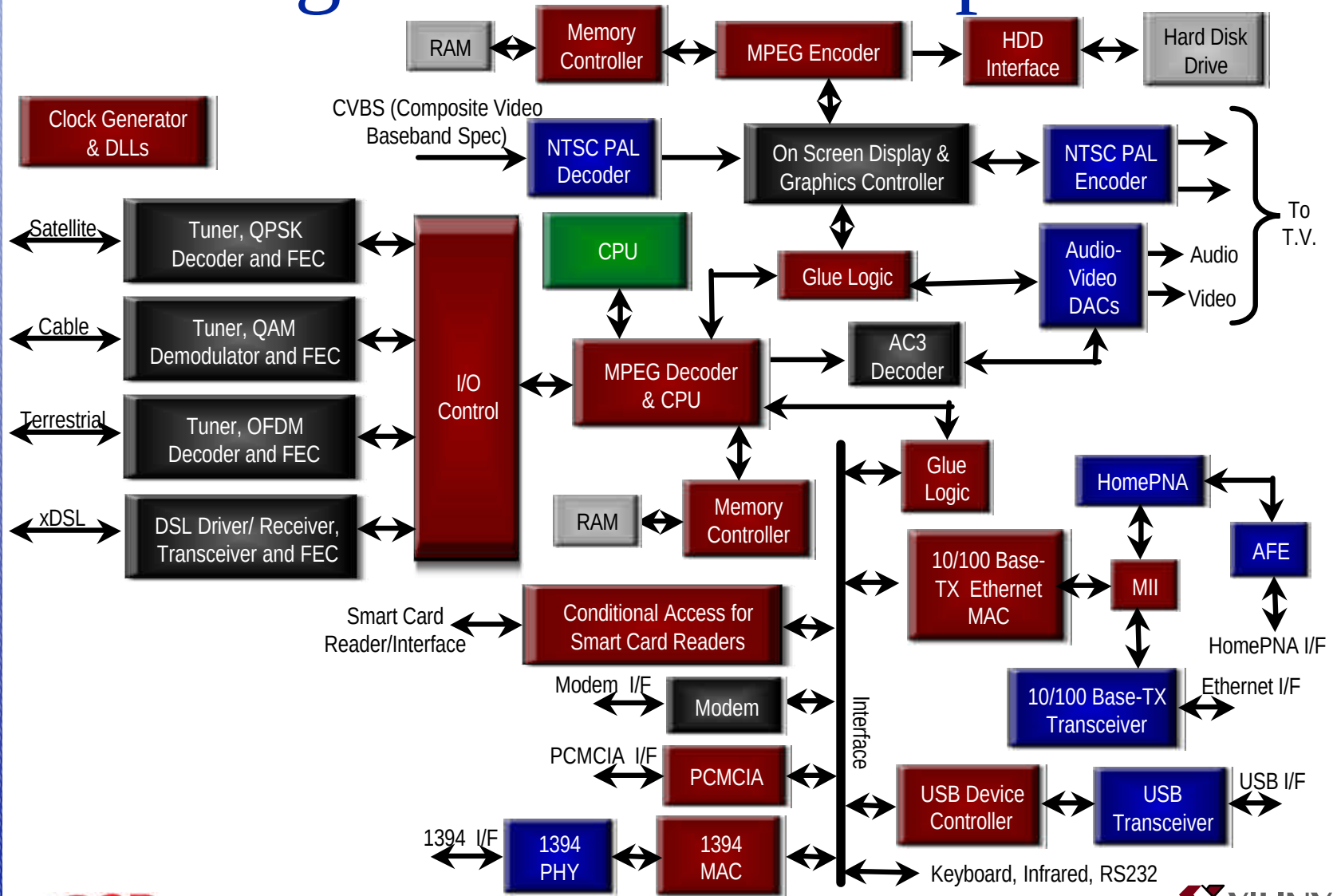
Set Top Box



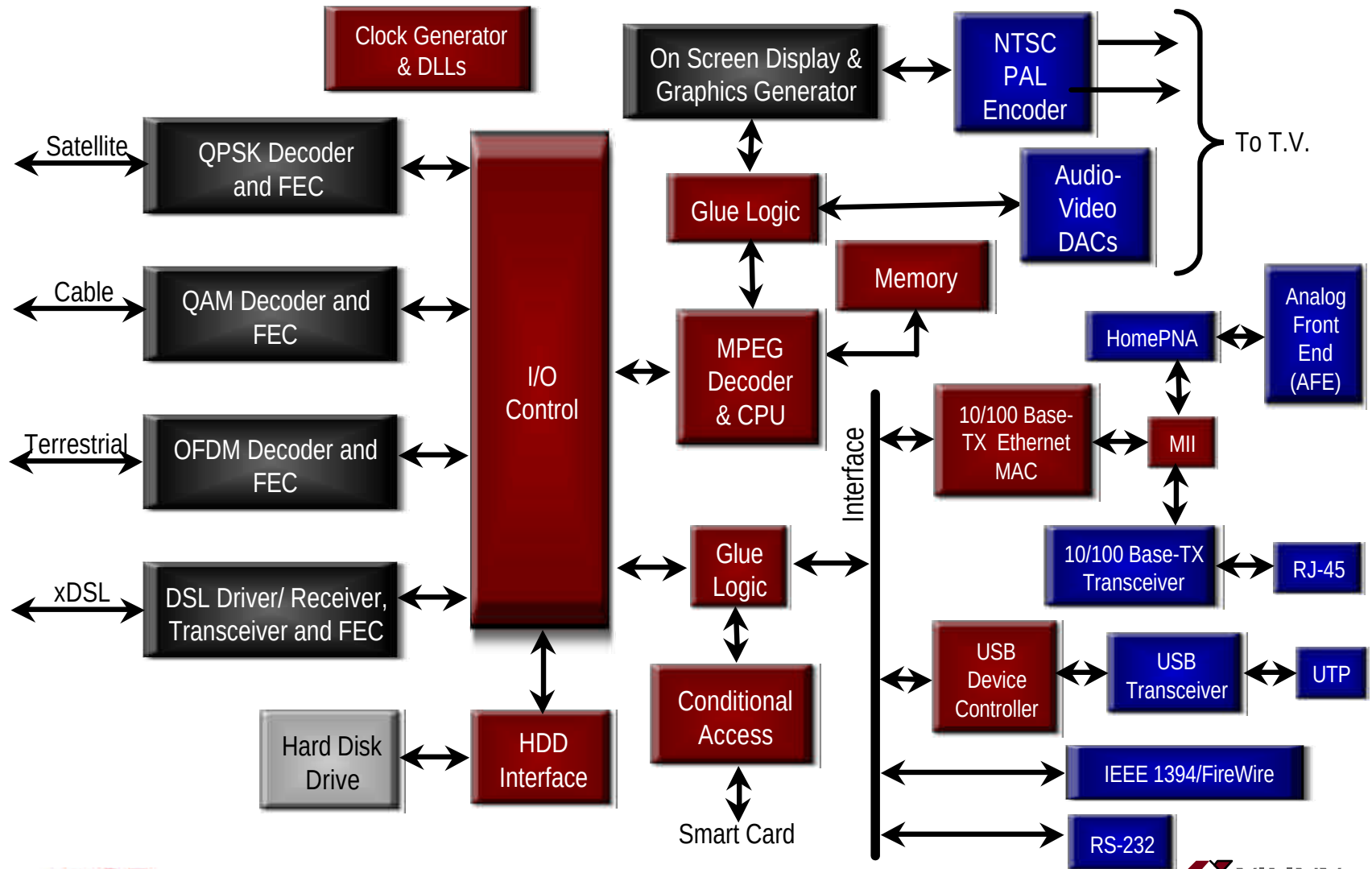
Set-Top Decoder Box



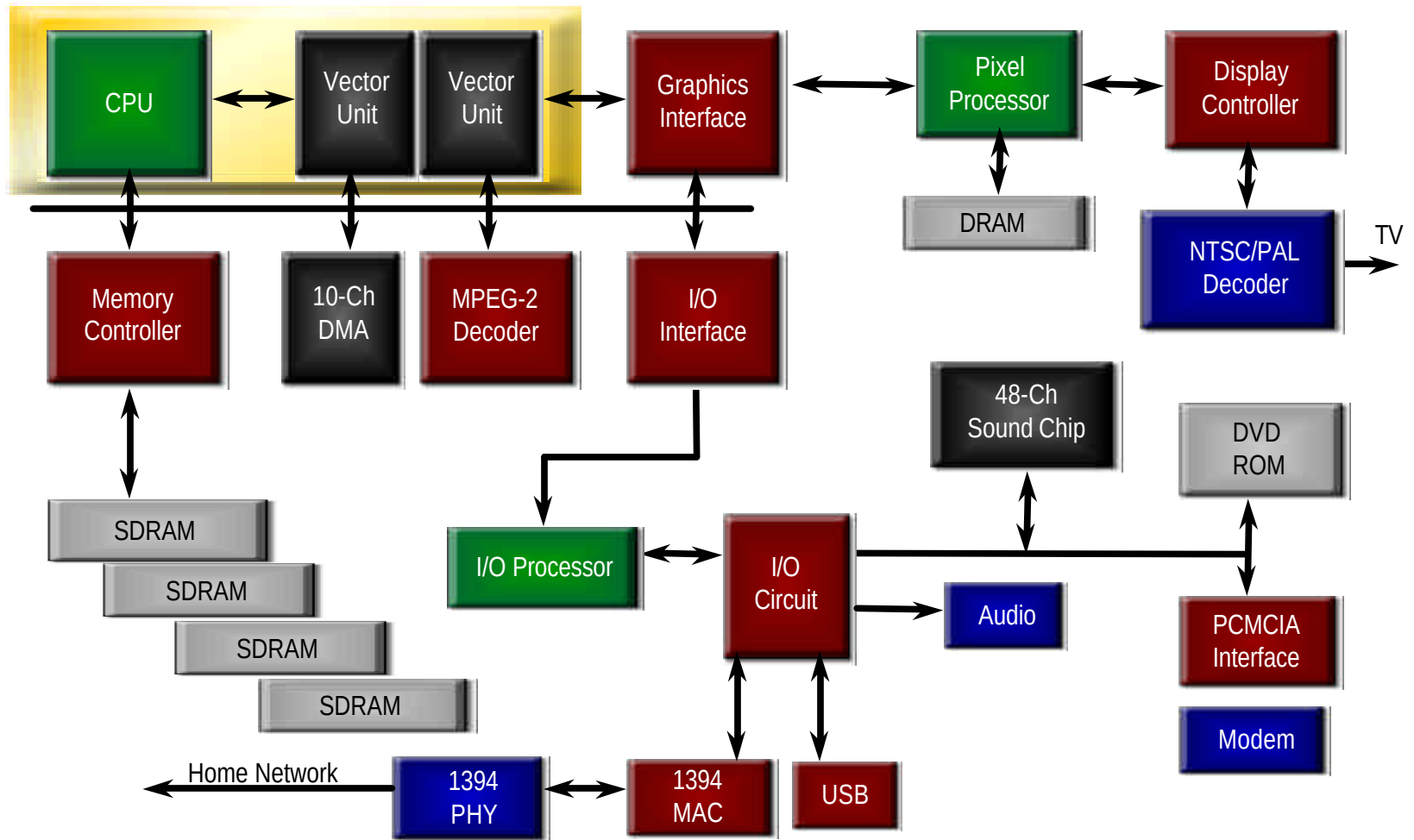
Digital VCR Set-Top Box



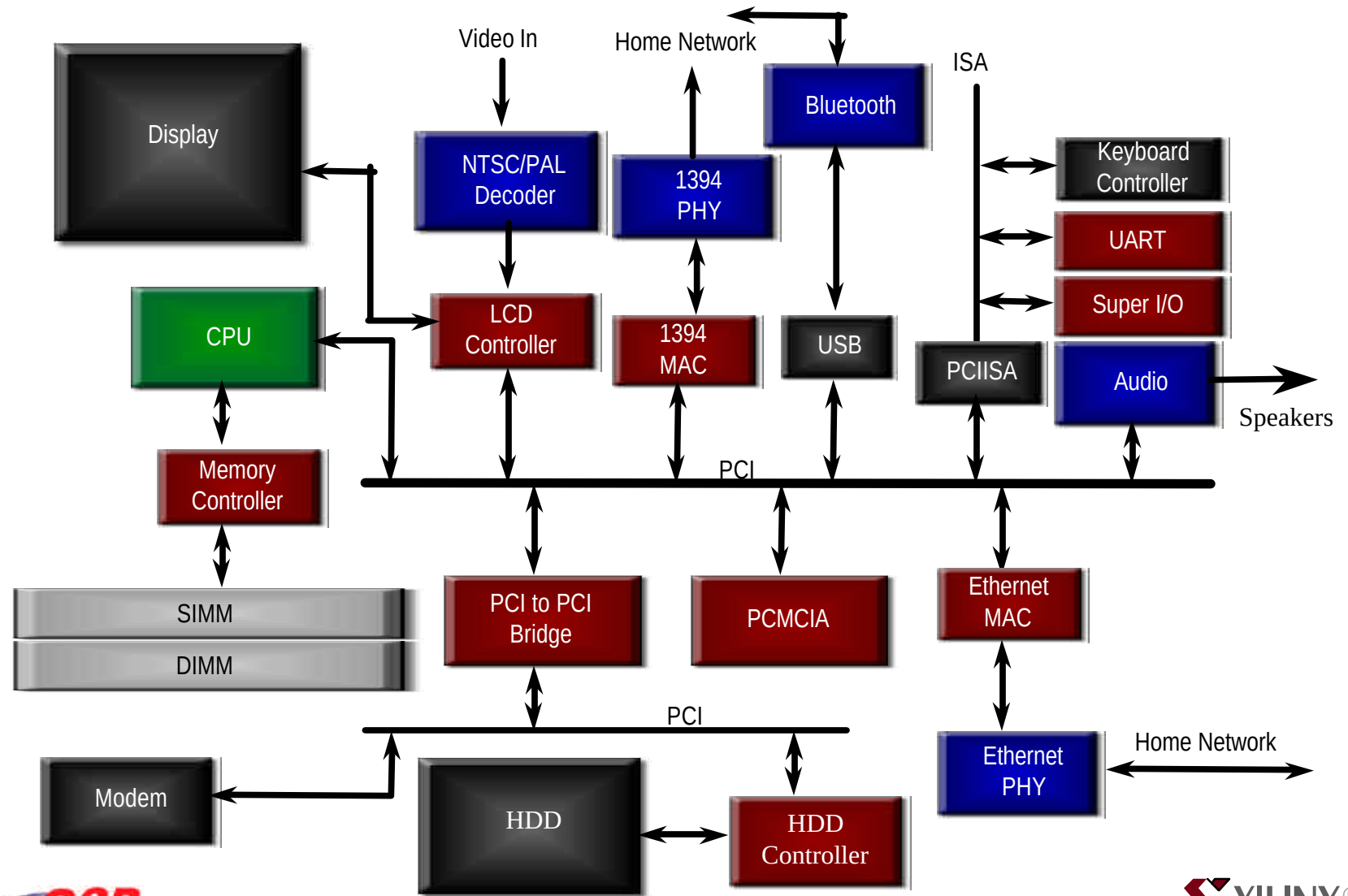
Residential Gateway (STB)



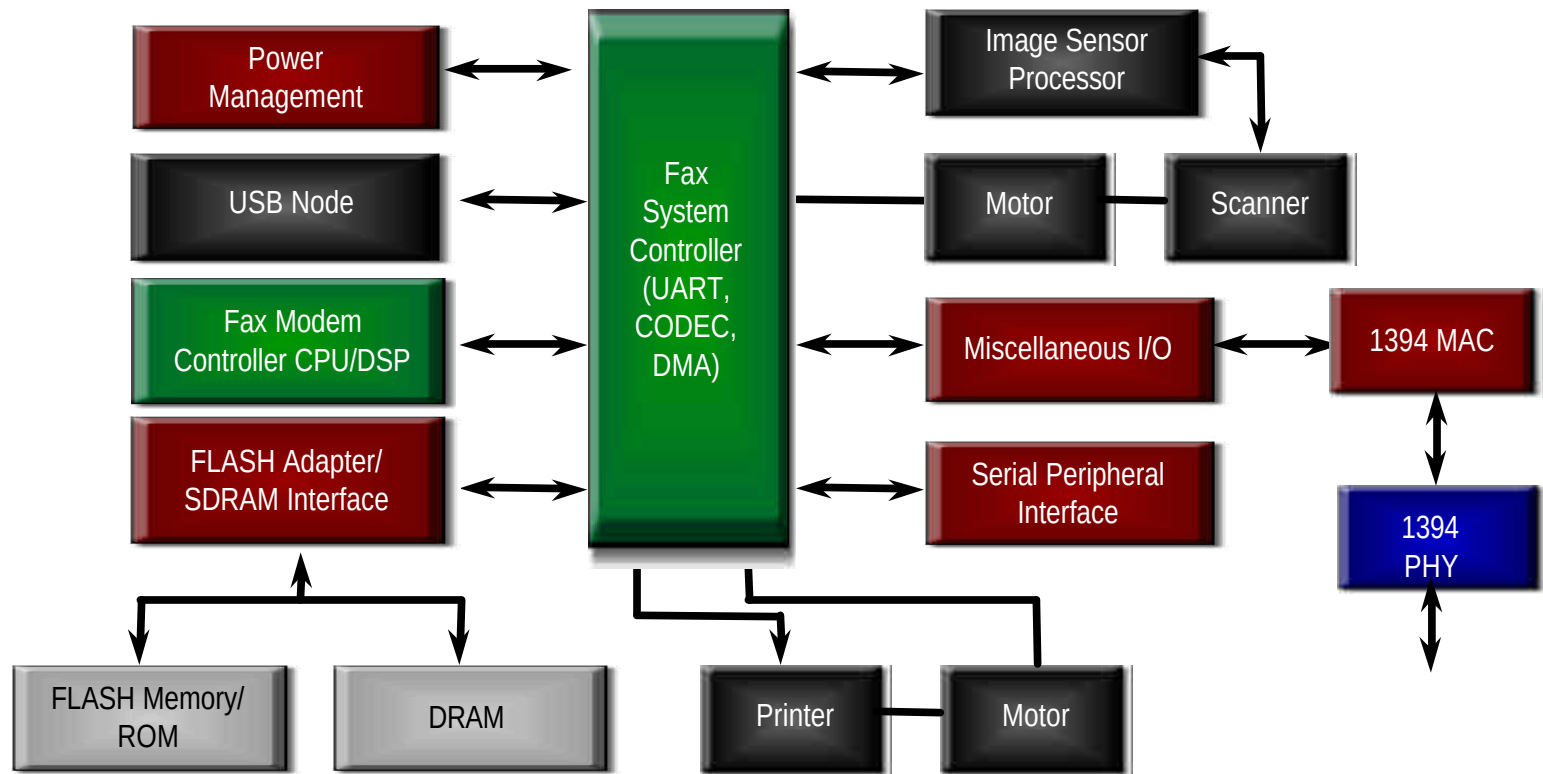
Gaming Station



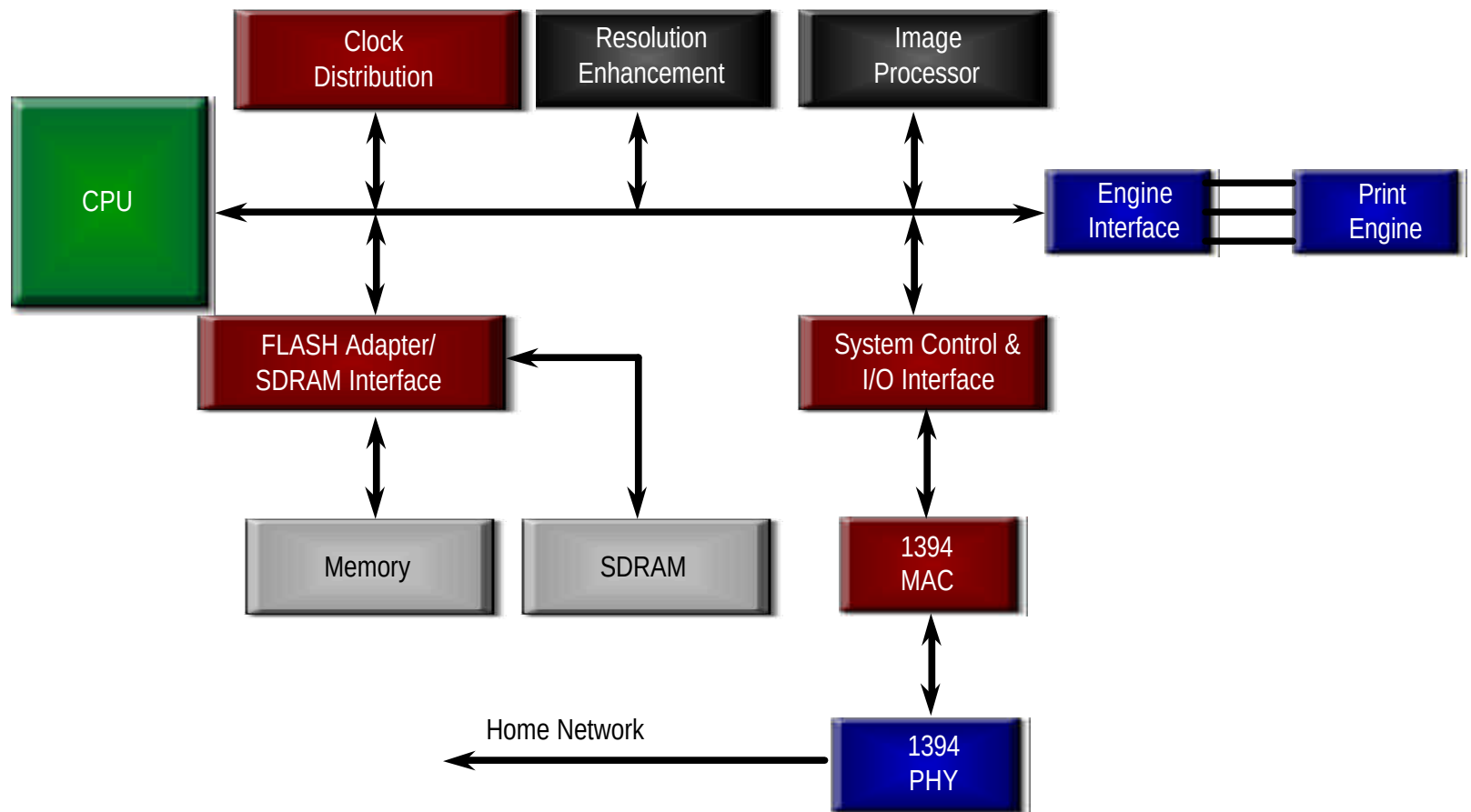
Desktop PC



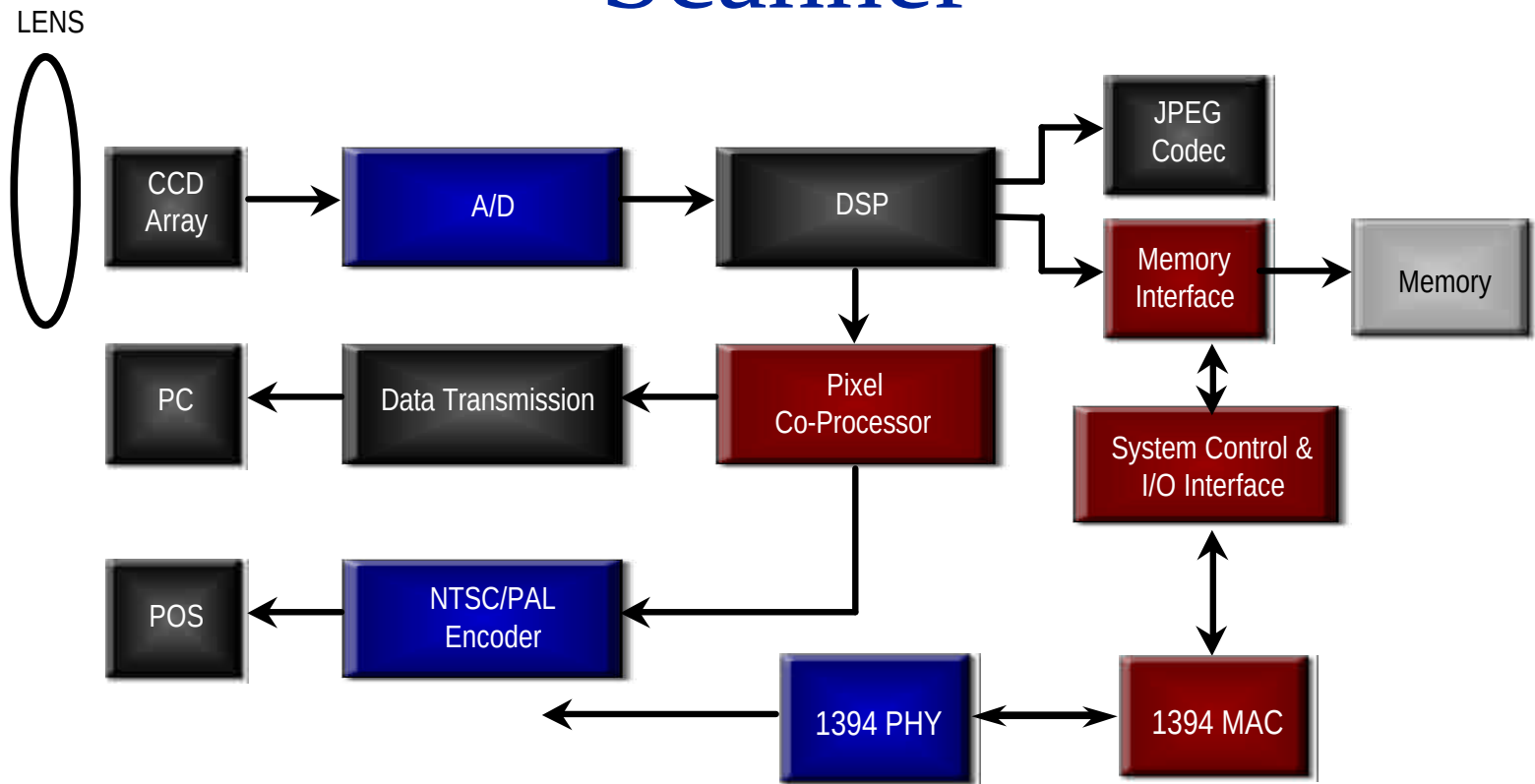
Multi-Function Peripheral



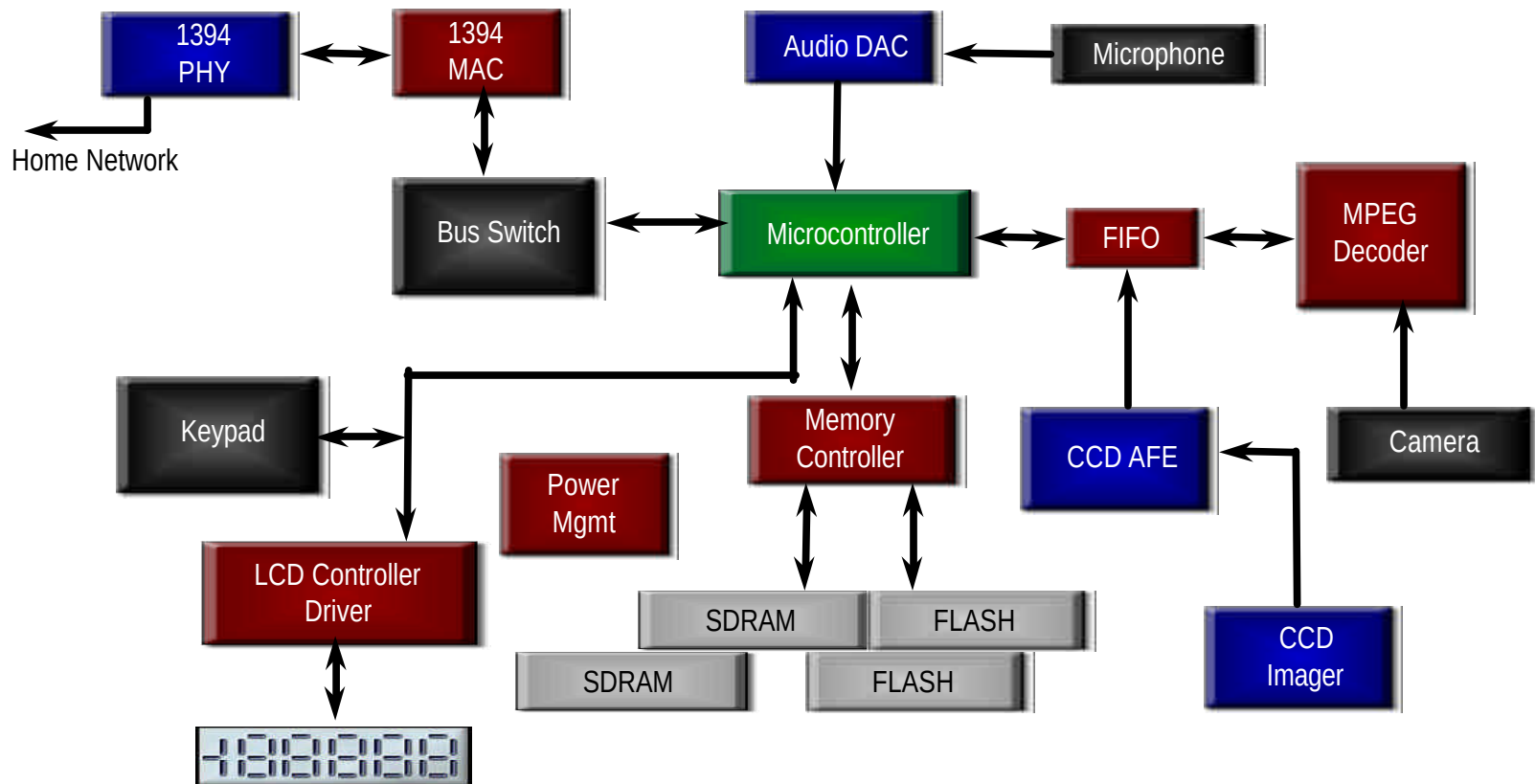
Printer



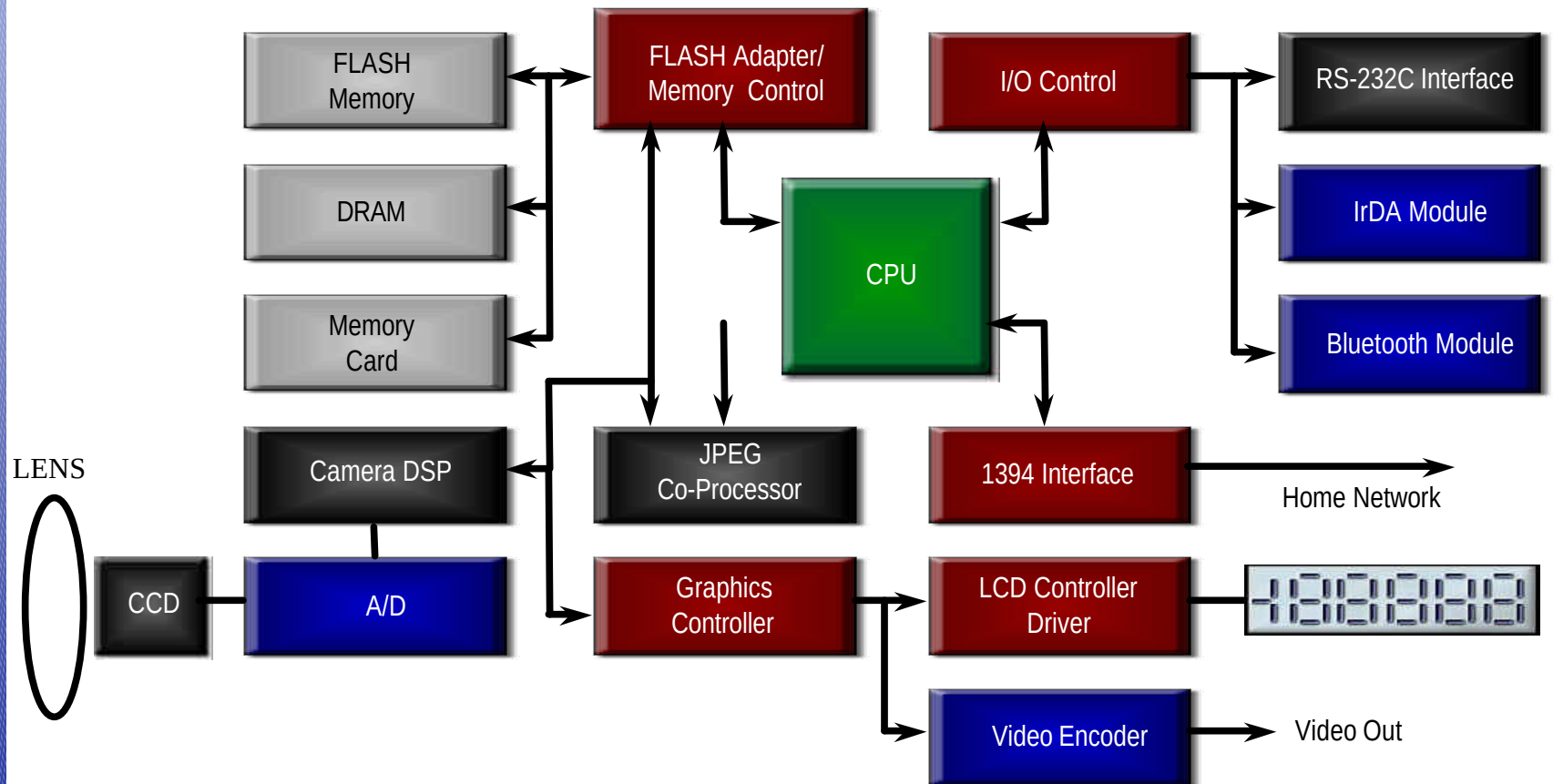
Scanner



Home Security

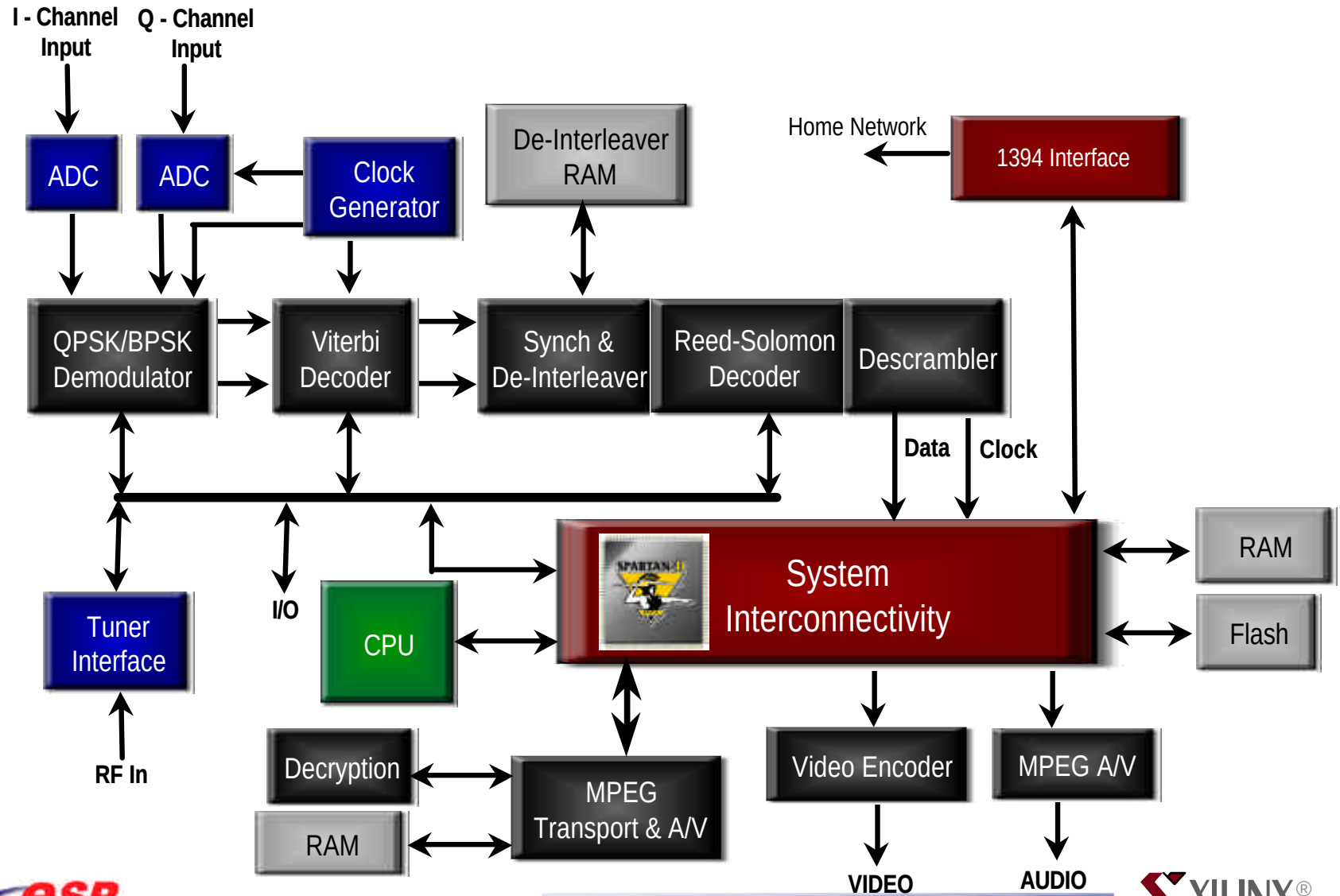


Digital Camera

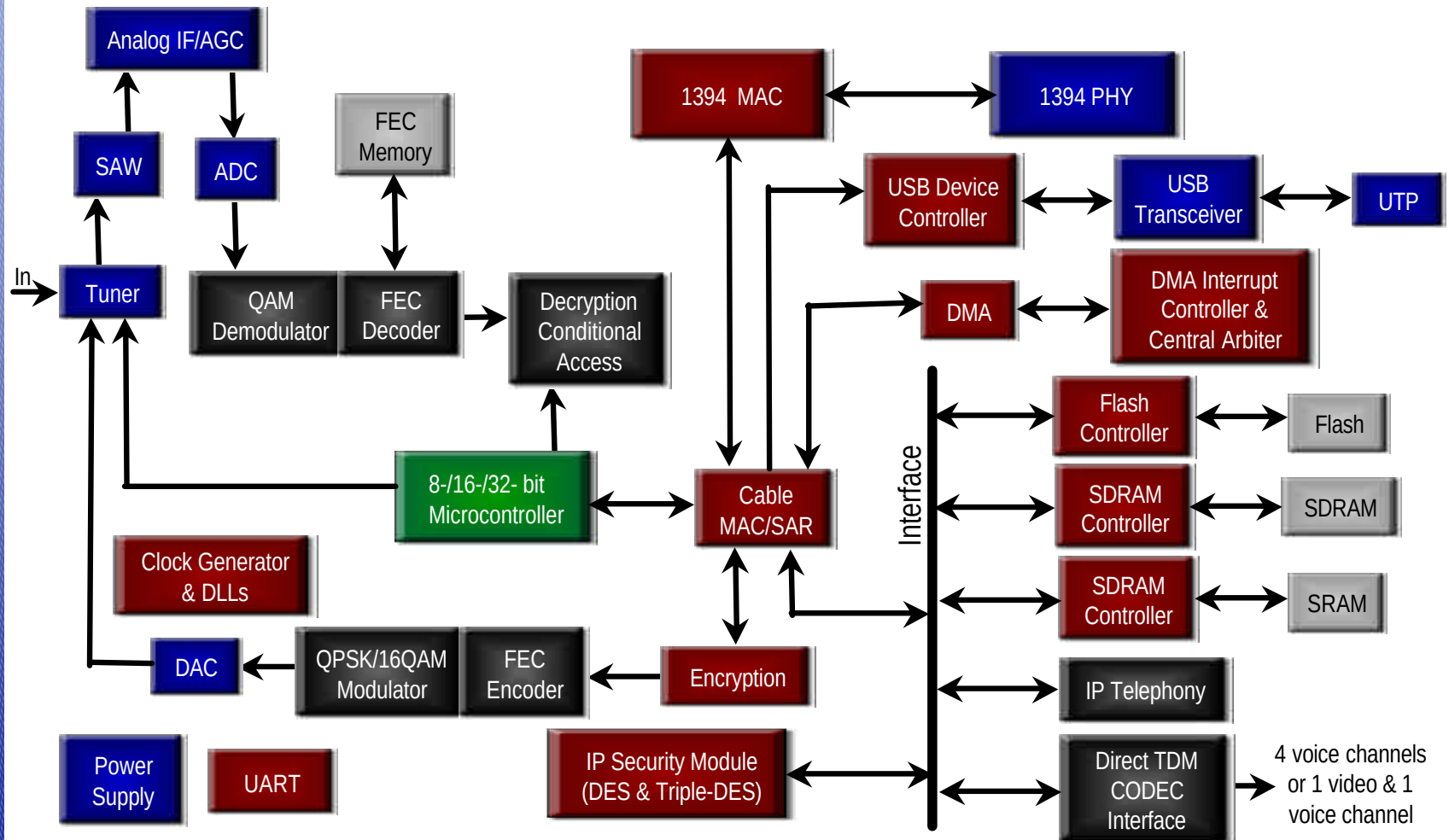


Satellite Modems

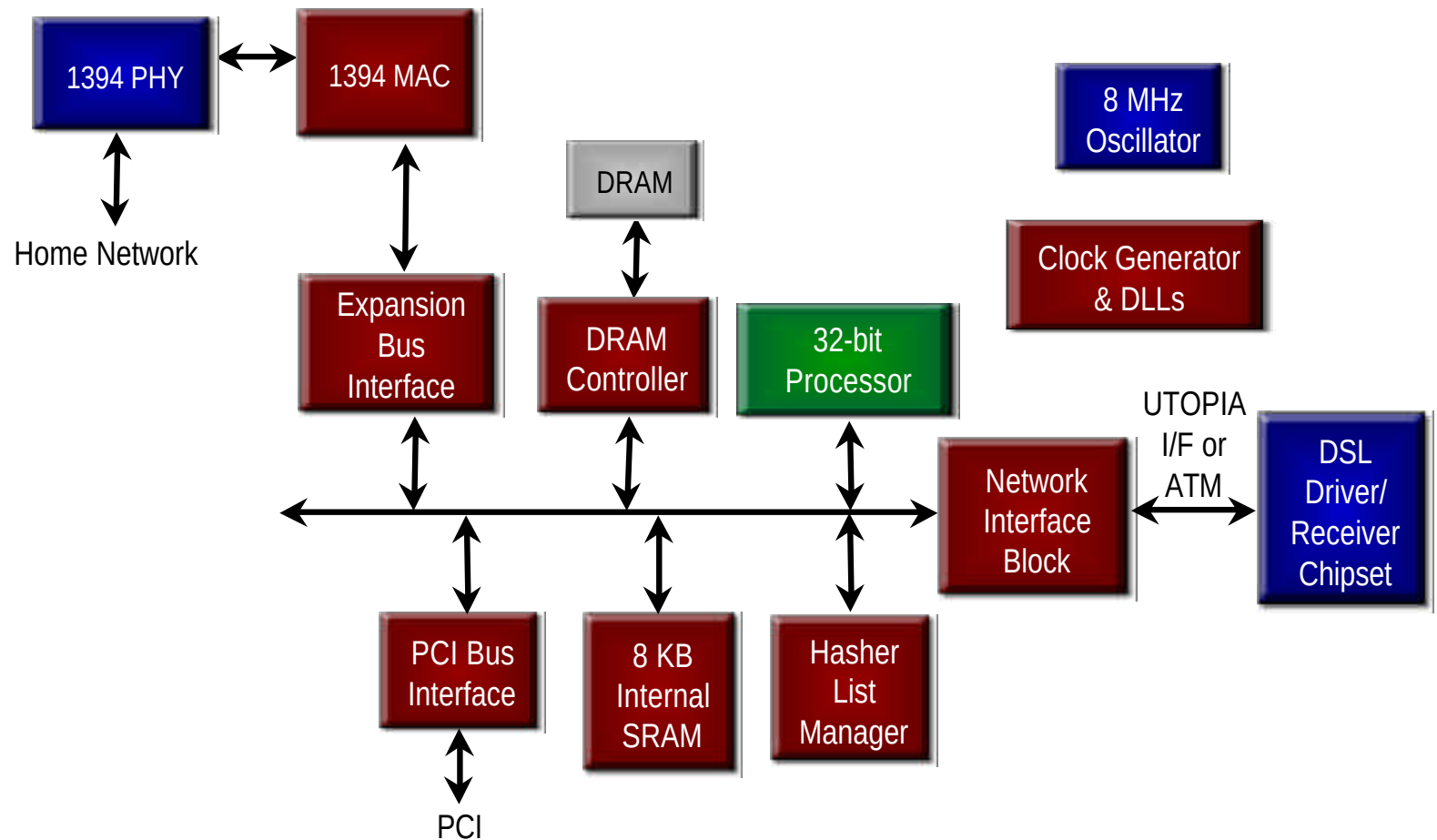
Quadrature Data from Tuner



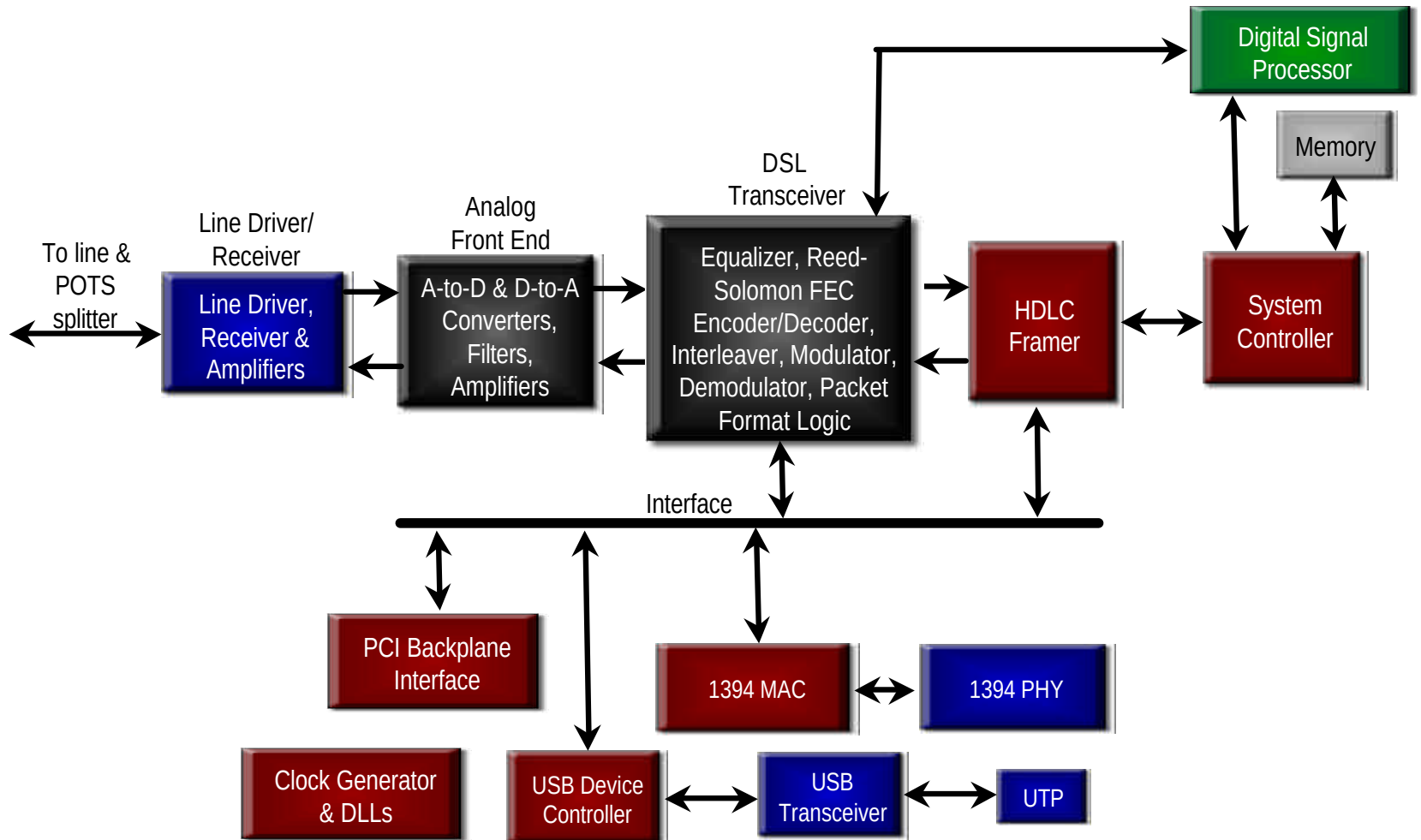
Cable Modem Residential Gateway



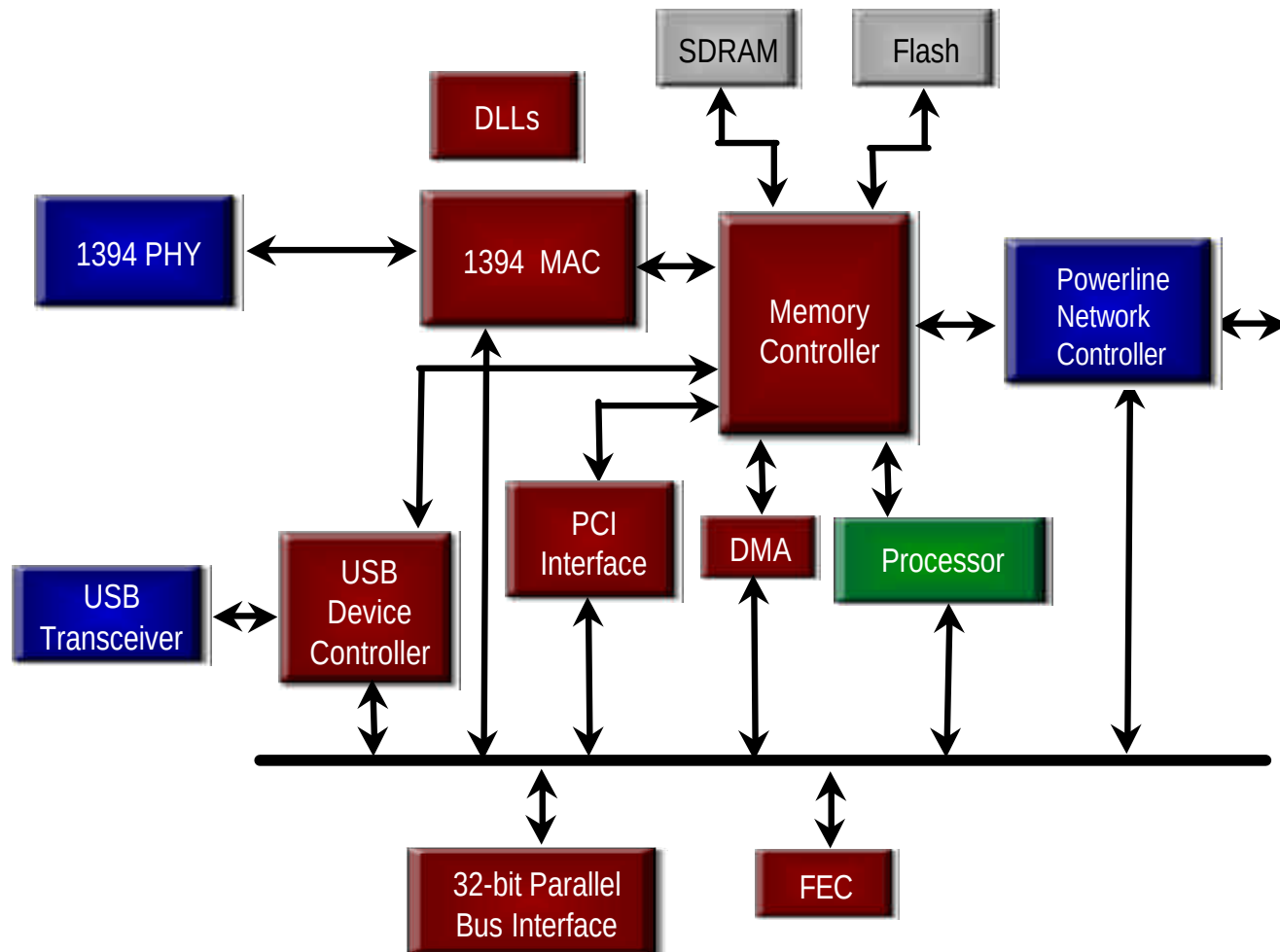
DSL Modem Home Gateway



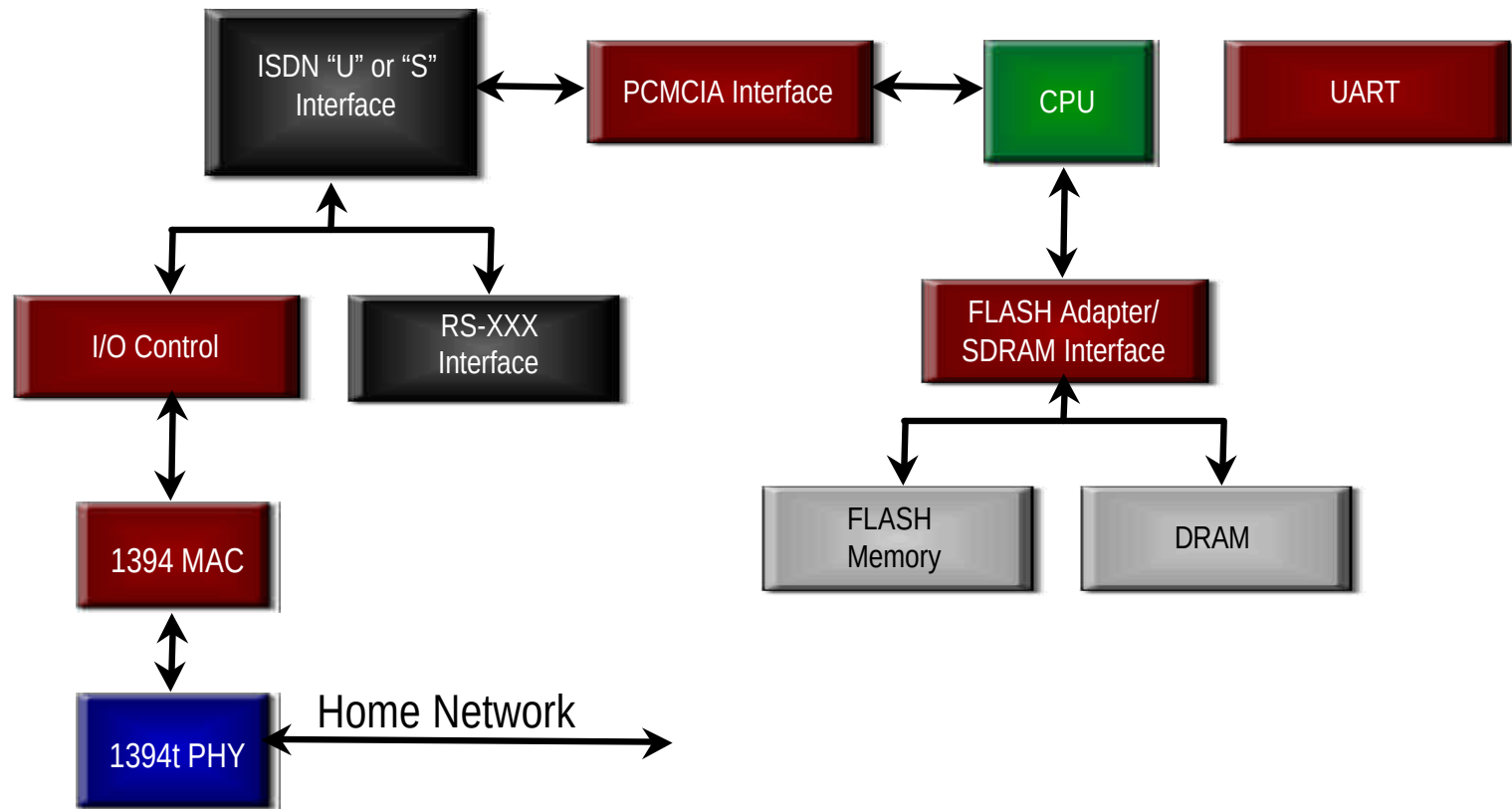
DSL CPE (Customer Premise Equipment)



HomePlug to 1394 Bridge



ISDN Modems



Spartan-II IP Solutions for 1394 Enabled Devices

- ◆ I/O Control
 - Multiple front end interfaces
 - Multiple back end interfaces
- ◆ Hard disk drive interface
- ◆ Clock distribution
 - DLLs
- ◆ MPEG decoder
- ◆ Ethernet MAC
- ◆ Error Correction
 - Reed-Solomon, Viterbi
- ◆ Memory solutions
 - Distributed memory, BlockRAM
 - Memory controllers
- ◆ CPU
- ◆ HDLC controller
- ◆ PCI
- ◆ Glue Logic
 - LCD controllers
 - UARTs
 - DMA controllers



Programmable Solutions Advantages

Xilinx Programmable Solutions Provide Several Benefits

- ◆ Time to market
 - Consumer devices require fast time-to-market
 - ASICs & ASSPs take 12-18 months to spin out
- ◆ Flexibility
 - Product customization to meet customer needs
 - Accommodate multiple standards & spec updates/changes
 - Feature upgrades
- ◆ Testing and verification
 - Re-programmable allows risk aversion
 - Your solutions are built on a proven FPGA technology with pre-verified silicon and IP that guarantees performance

Xilinx Programmable Solutions Provide Several Advantages

- ◆ Xilinx On-line - field upgradability
 - Remote update of software and hardware
 - Results in increased lifetime for a product (time-in-market) and allows new, interesting applications
 - Enable product features per end-user needs
- ◆ Issues in creating a stand-alone ASIC/ASSP
 - Choosing the right solution
 - Product customization
 - Development cost and amortization
- ◆ Low Cost

Lifecycle Component Logistics

- ◆ Xilinx is an assured source of supply
 - Spartan FPGAs are high volume standard parts
 - Xilinx is a Strategic customer to our fab partners
 - If a device is retired, designs are quickly portable
- ◆ Xilinx's solutions reduce exposure to component supply issues
 - Designs can be quickly adapted to efficiently address component supply problems
 - NAND to NOR type Flash support for example
 - Gives latitude in maintaining a cost effective BOM in dealing with the allocation, end of life & generational migration realities of today's component market

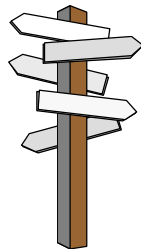
Specification Changes

- ◆ Emerging markets are exposed to multiple standards and specification changes
 - DSL Modem market
 - 6 different variations
 - DTV market
 - 18 different formats

OEM/ Vendor



Market



U.S. Networks Select Digital Broadcasting Format

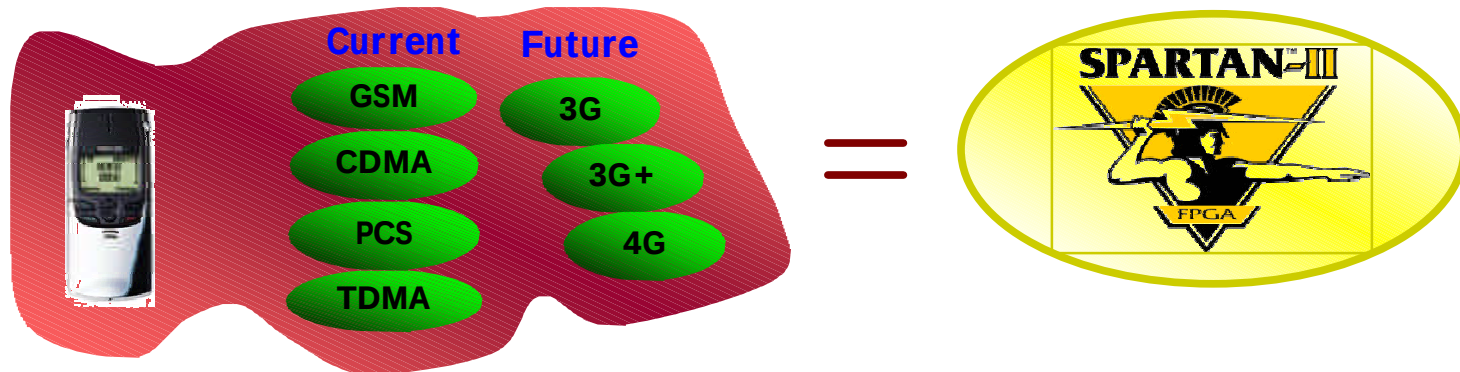
ABC	720-Progressive. For non-HDTV broadcasts, ABC will use 480-line progressive format.
CBS	1,080-Interlaced. Wants to be compatible with HDTV sets as well as normal quality formats on regular analog television sets. Digital broadcasting will begin at select CBS-owned stations in the fall of 1998. By November 1999, CBS plans to be broadcasting digitally into 43% of U.S. households. For other broadcasts, CBS will use the 480-line Interlaced format.
NBC	1,080-Interlaced. NBC is leaning toward 480-line progressive for non-HDTV broadcasts.
FOX	720-Progressive. For non-HDTV broadcasts, Fox will use the 480-line progressive format.
PBS	For HDTV, PBS is undecided. For non-HDTV broadcasts, PBS will use the 480-line interlaced format.
Local Stations	Will have to conform to their network's format for national programming but can select any format for local programming.

Source: IC Insights

A Programmable Solution Future Proof's Success

New Flexibility from FPGAs

Driving down the cost of consumer products with low cost reprogrammable products



Enabling a whole new breed of consumer products



Xilinx & Replay TV

- Revolutionizing consumer TV

Reprogrammable nature allows

- Field upgrades
- Field fixes
- Mars probe repair from earth
- Support for numerous standards



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FPGAs, the Unsung Hero

Driving the Consumer Digital Logic Revolution

- ◆ The digital consumer world is here
 - Imperatives driving market success
 - Time to market and time-in-market
 - Flexibility
 - Custom digital logic
- ◆ Xilinx - The answer for consumer digital applications
 - Introducing the low cost Spartan-II programmable family
 - Cost reduced for the consumer market
 - Fully programmable at the desktop, in the field or in the application
 - Future proofed for changing standards



Xilinx Digital Consumer Logic

A Natural Fit for Home Networking

- ◆ Xilinx solutions enable you to thrive in chaos
 - Fastest time-to-market
 - First to market, gains market share and revenue advantage
 - Xilinx Online provides reconfigurability in the field
 - Allows shipped product to support revisions to the spec
 - Enables unique opportunities to add Value
 - Increases life-cycle revenue yield & hence time-in-market
 - Enables rapid product proliferation
 - New designs can be quickly turned into derivatives
 - Feature superior lifecycle component logistics
 - Testing and Verification
 - Proven FPGA technology, software, test benches
- ◆ Cost Effective!!!