Xilinx Solutions for Home Networking Products

Spartan-II FPGAs + IP Cores

Strategic Applications

Agenda

- Introduction
  - Spartan-II solutions for home networking products
- IP cores information
- Summary

Spartan-II Solutions for Home Networking Products

- I/O control
  - Multiple front end interfaces
  - Multiple back end interfaces
- Hard disk drive interface
- Clock distribution
  - DLLs
- MPEG decoder
- Ethernet MAC
- Error correction
  - Reed-Solomon, Viterbi
- PCI
- Memory solutions
  - On-chip Distributed memory, BlockRAM
  - Memory controllers
- CPU / microcontroller
- HDLC controller
- ADPCM
- Color Space Converters
- Glue logic & system integration
  - LCD controllers, UARTs, DMA controllers

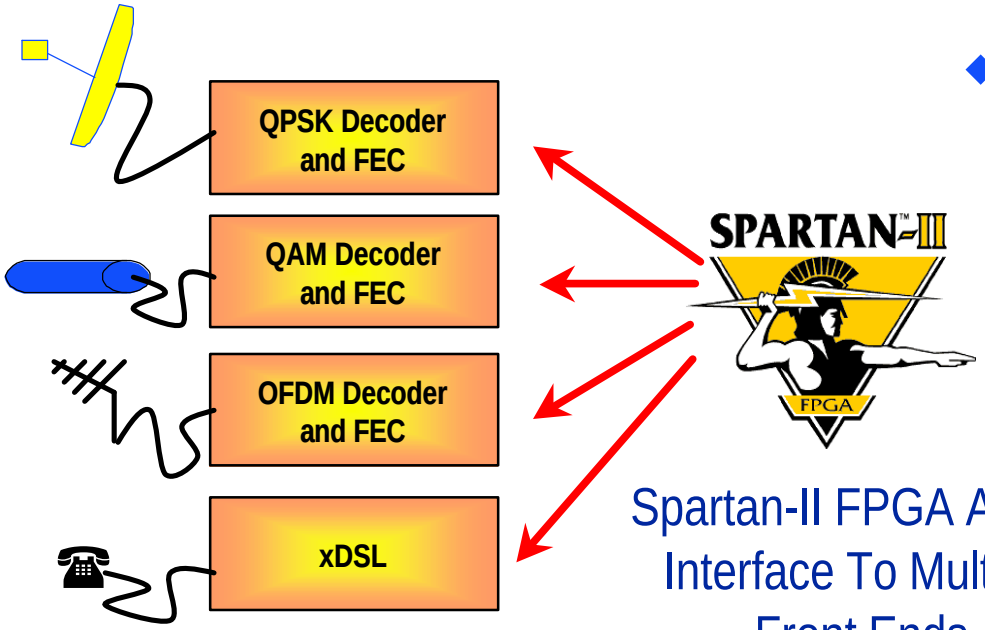
I/O Control

Front End Interface (to Broadband Access)

Back End Interface (for Home Networking)

I/O Control - Front End Interface

- Cost prohibitive to support multiple receivers
  - Multiple receivers are required to have one product fit maximum markets
  - Cable, terrestrial, satellite and xDSL



Spartan-II FPGA Allows Interface To Multiple Front Ends

- Interface required to support multiple ASSPs
  - Choice of ASSP influenced by broadcaster features

Back End Interface For Multiple Home Networking Technologies

- RGs network multiple technologies within the home
  - USB/USB 2.0, Ethernet, 1394/FireWire,
  - HomePNA (phonelines), powerlines
  - HomeRF, Wireless LANs (IEEE 802.11a, IEEE 802.11b, HiperLAN2), Bluetooth
- Interfaces to multiple receivers & multiple home networking chipsets are imperative
  - Several products for different markets is cost prohibitive
    - OEMs are always second guessing if another technology will prevail and if their products will remain in the market
  - FPGAs provide the needed time-to-market and time-in-market

Hard Disk Drive Interface

HDD Interface

- Spartan-II FPGAs provide value as hard disk drive interfaces to a residential gateway
  - Provide capability to store video on hard disk drives
  - Provide capability to record and view video simultaneously like in digital VCRs (TiVo, Replay)
- Provides data buffer and disk control logic
  - On-chip memory for FIFOs
- Provides ability to support evolving disk drive technologies
  - Optimized for simultaneous disk read and write
- Enables dual sourcing of multiple types of hard disk drives

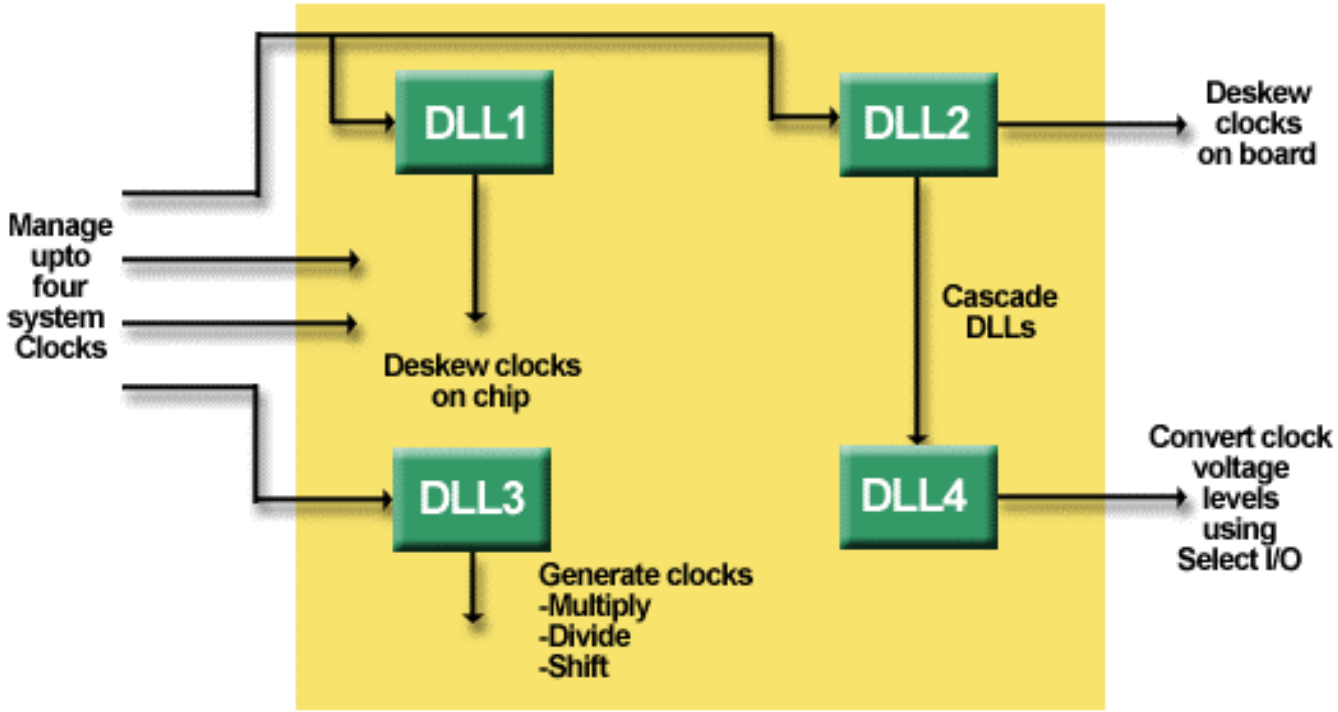
Spartan-II FPGA Enables New Set-Top Box Technology

- Spartan-II FPGAs are used to revolutionize the TV experience
  - Pause live TV
  - Instant replay
  - Automatically records favorite programs
  - Advanced TV program search

Clock Management

DLLs

Spartan-II - Clock Management



Delay Locked Loops Lower Memory and Board Costs

Clock Generation and Distribution

- Spartan-II DLL circuits provide full clock management solution
- Clock generation
  - Synthesizing many clocks from a single reference crystal or clock
- Clock buffering and distribution
  - Providing multiple copies of a single clock
  - SDRAM clocks
- Spread spectrum clocks for EMI reduction
  - DLL circuits allow tolerance for ±2.5% variance

MPEG Decoder

DCT/IDCT

MPEG Decoder

- DCT/IDCT compression allows increased throughput through transmission medium
  - Discrete Cosine Transform (DCT) and Inverse DCT (IDCT)
  - Video & audio compression makes multimedia systems very efficient
    - Increases CPU bandwidth
    - Higher video frame rates
    - Better audio quality
    - Enables multimedia interactivity
- DCT / IDCT are widely used in video & audio compression

DCT/IDCT Applications

- List of some end applications
  - DVD/Video CD players
  - Cable TV
  - DBS systems
  - HDTV
  - Graphics/image processing cards
  - Ultrasound/MRI systems
  - Digital VCRs
  - **Set-top boxes**
  - Digital camera

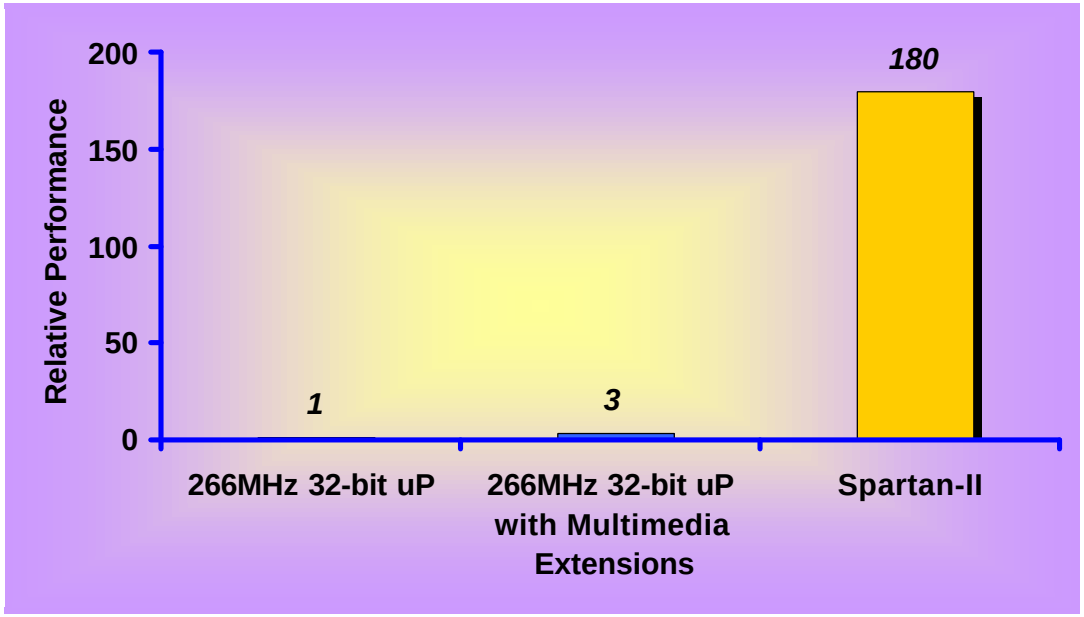
Spartan-II DCT/IDCT Solution Features

Features	Spartan-II
Device	XC2S100-6
CLBs	1026
Clock IOBs	1
IOBs	28
Performance (MHz)	33.3

AllianceCORE Xentec DCT/IDCT Core

Top End Set-Top Box Solution

- Spartan-II FPGAs provide low cost, high performance MPEG encoding/decoding
  - DCT/IDCT AllianceCORE IP from Xentec
  - Offload processor for high performance system



Fast Ethernet MAC

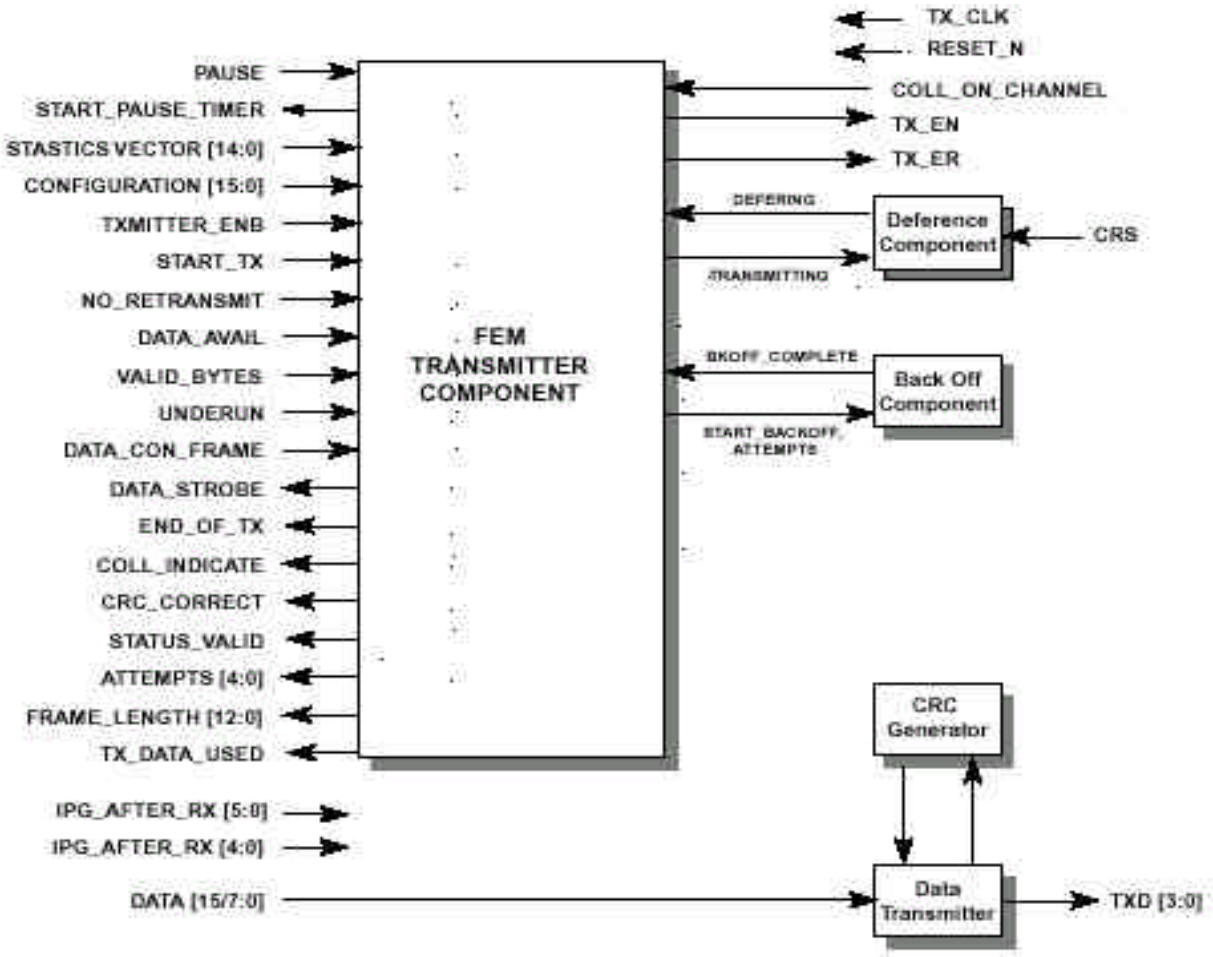
Fast Ethernet Media Access Controller

- Spartan-II Fast Ethernet MAC transmitter and receiver cores are provided by CoreEl MicroSystems
  - Cores may be purchased and used separately for systems that only require a transmit or receive function
- Applications of the Fast Ethernet MAC cores
  - Applications requiring CSMA-CD protocol for media access
    - Used to implement a multi-channel MAC chip with other common functions like a linked list buffer manager and a DMA control function
  - Used for Ethernet switches, hubs and network interface cards (NICs)

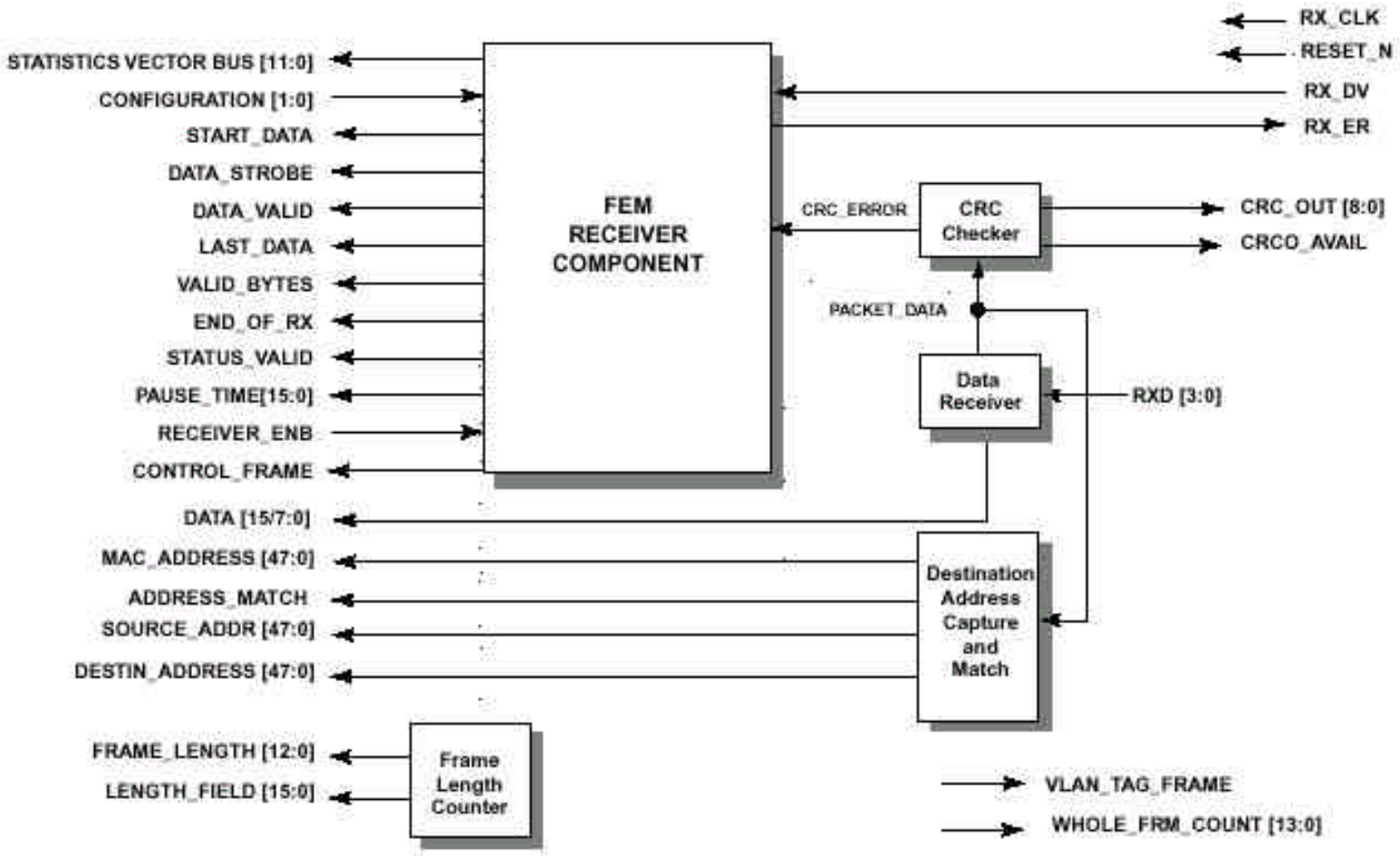
Features of the Fast Ethernet MAC Core by CoreEl MicroSystems

- Individual transmitter & receiver cores
  - Available separate or together
- Fully synchronous logic design
- Fully meets IEEE 802.3 spec
- Supports half & full duplex operation
- Supports full duplex flow control feature (802.3x)
- Flexible frame retransmission or abort feature
- Media Independent Interface (MII)
- Meets Virtual Socket Interface (VSI) spec for a Soft Virtual Component
- Short frame transmission by padding
- Programmable inter-packet gap
- MAC address match feature
- Pause control frame detection
- Multicast & broadcast frame detection
- Extensive statistics information on transmit frames for RMON and MIBs
- Simple host data transfer interface
- Two host interface data path width options: 8- or 16-bits
- Optional long frame transmission & reception

Fast Ethernet MAC Transmitter



Fast Ethernet MAC Receiver



Spartan-II Based Fast Ethernet MAC

Spartan-II FPGAs Based Fast Ethernet MAC Specifics	
Product Families Supported	Virtex, Virtex-E, Spartan-II
Device Tested	XC2S150
CLBs - Transmitter: CLBs - Receiver:	440 332
Clk IOBs - Transmitter: Clk IOBs - Receiver:	1 1
IOBs - Transmitter: IOBs - Receiver:	99 261
Performance (MHz)	50

Spartan-II Solutions In Error Correction

Reed-Solomon

Viterbi

Error Correction

- Data transmission & storage are fundamental functions in most electronic systems
- In an Ideal Communication Medium
  - Errors do not come into play during transmission
- In the Real World
  - Noise causes data corruption
- Error-correcting coding systems are required
  - Reed Solomon
    - Block codes
  - Viterbi
    - Convolution codes

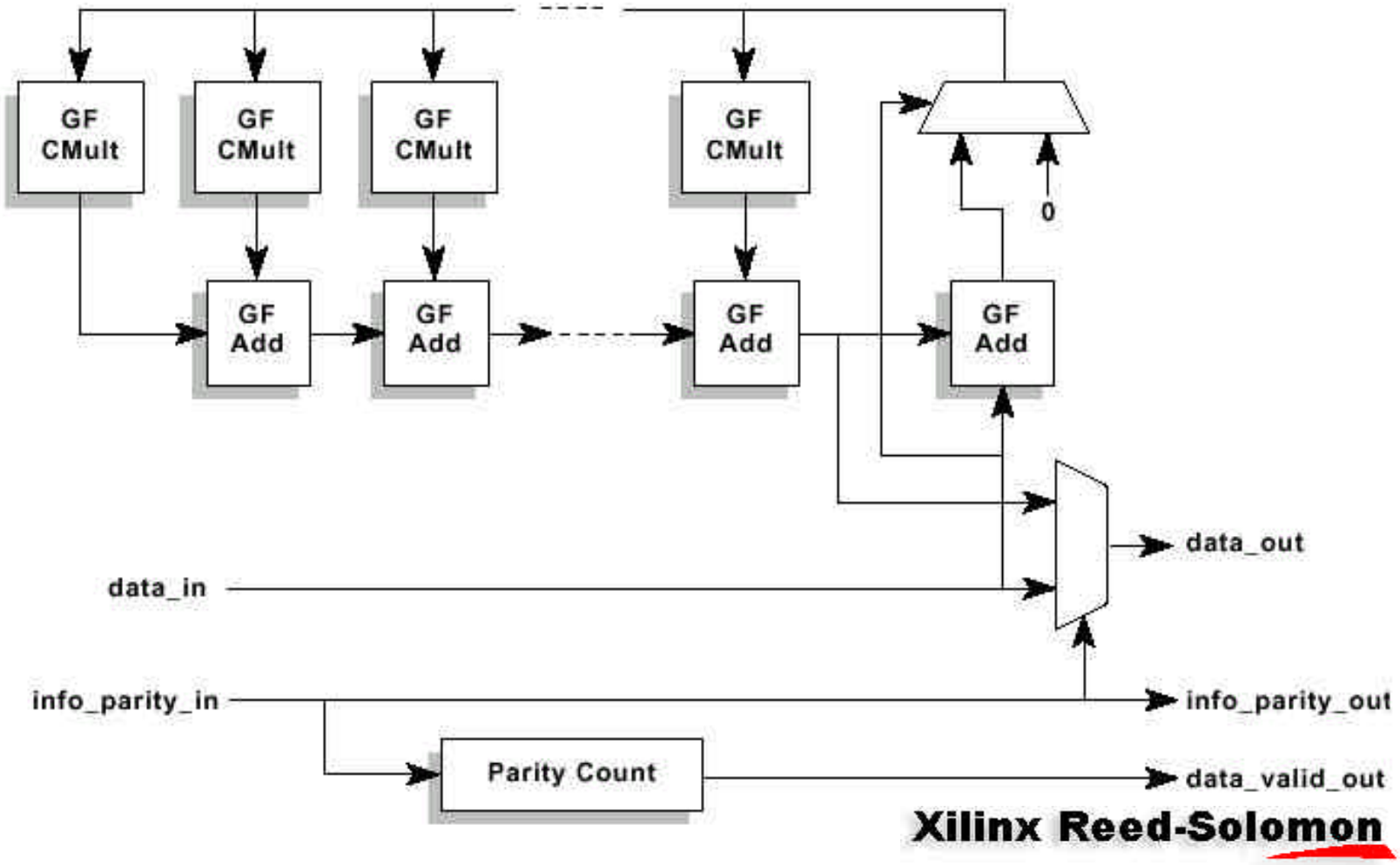
Reed-Solomon Encoder / Decoder

- Reed-Solomon
  - An error-correcting coding system that corrects multiple errors, especially burst-type errors in communication systems
  - Transmitter (encoder)
    - Data is encoded to be corrected in an event it acquires errors
  - Receiver (decoder)
    - Uses the appended encoded bits to determine errors
    - Corrects the errors upon reception of the transmitted signal

Spartan-II Reed-Solomon IP Solutions

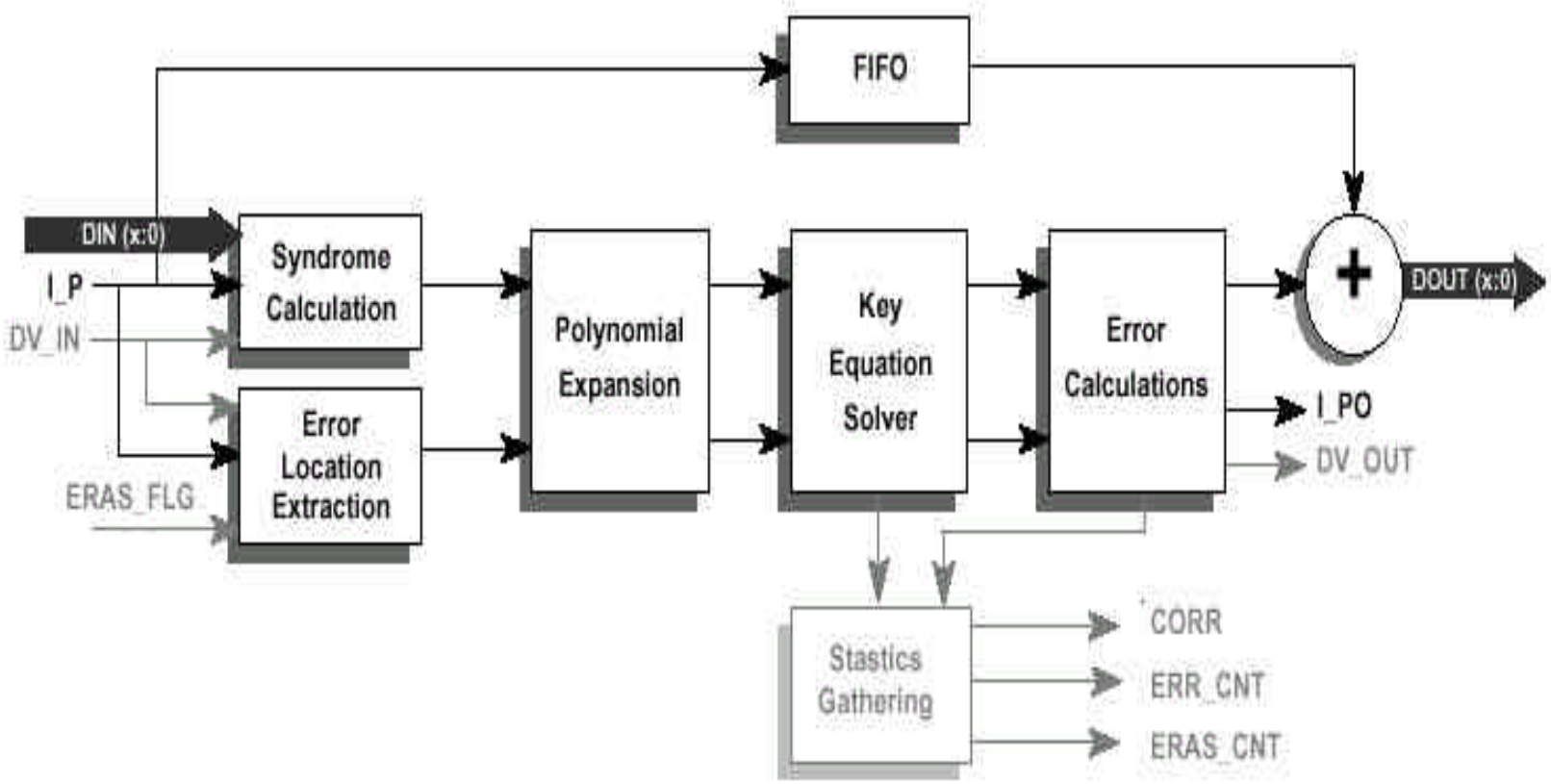
- Spartan-II + Reed-Solomon IP = Programmable Reed-Solomon Solution
- Xilinx Reed-Solomon is provided through LogiCORE program by
  - Integrated Silicon Systems
    - Reed-Solomon Encoder & Decoder core
- Reed-Solomon solutions are also provided by the following AllianceCORE partner
  - Memec Design Services
    - XF-RSENC Reed-Solomon core - Encoder
    - XF-RSDEC Reed-Solomon core - Decoder

Integrated Silicon Systems



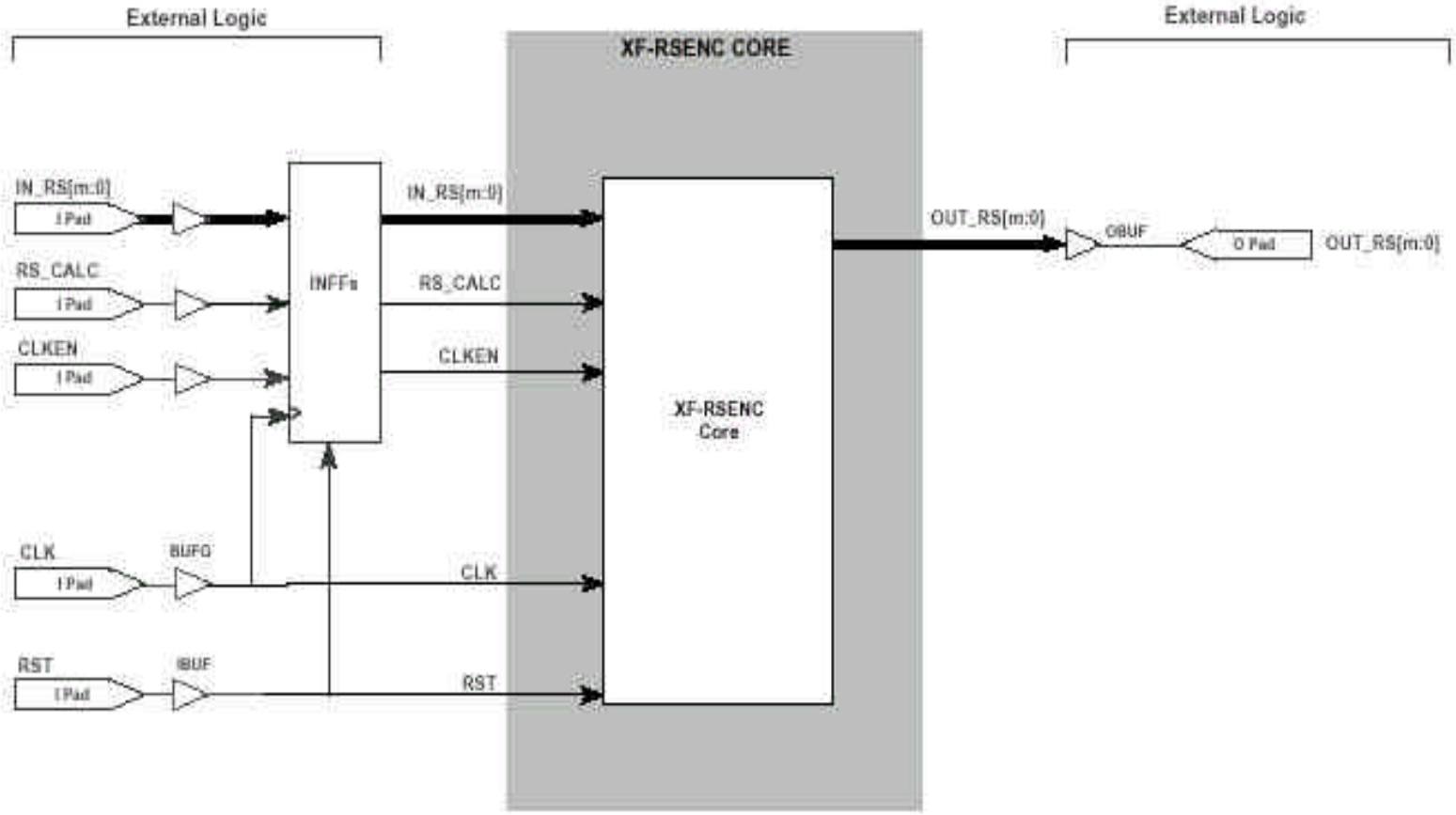
Reed-Solomon Encoder Block Diagram

Integrated Silicon Systems



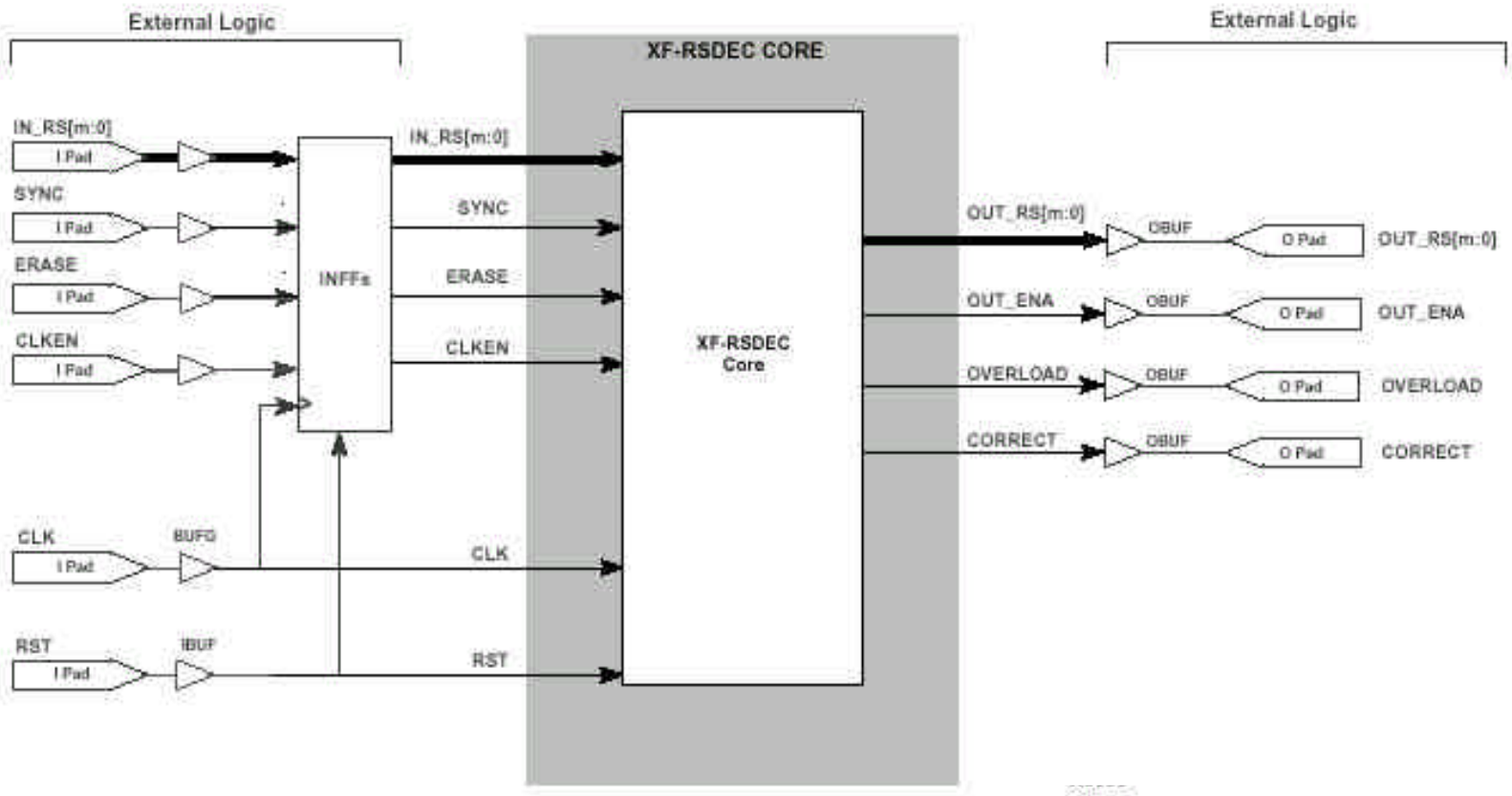
Reed-Solomon Decoder Block Diagram

Memec Design Services



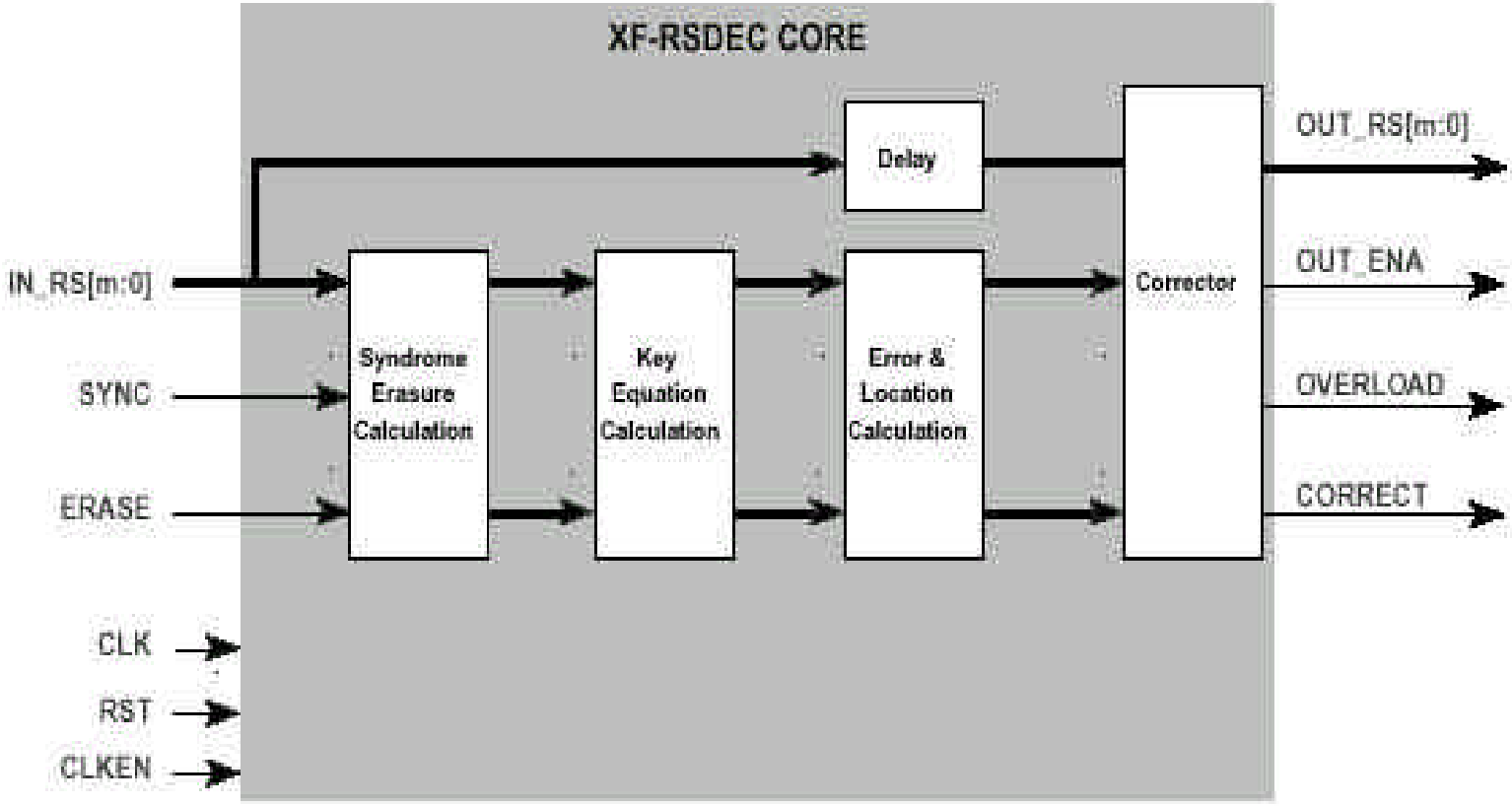
XF-RSENC Core with External Logic - Reed-Solomon Encoder

Memec Design Services



XF-RSDEC Core with External Logic - Reed-Solomon Decoder

Memec Design Services



XF-RSDEC Core - Reed-Solomon Decoder Block Diagram

Spartan-II Reed-Solomon IP Solutions - Features

- Encoder and decoder cores
  - Available Separately
- Web-based configuration and download
  - Supports many Reed-Solomon coding standards and “roll-your-own”
  - Receive customized core in minutes (via email)
  - Generate unlimited number of cores (site licensing)
- Both cores can be considered as black boxes
- RPM Technology
  - Used for predictable performance & fast implementation times

Spartan-II Reed-Solomon IP Solutions - Advantages

- The Xilinx decoder core is half the size than any competitor's offering
- Automatically configured from user parameters
  - Supports all major coding standards and custom implementations
- Can be optimized for area or speed
- Incorporates Xilinx Smart-IP technology for design predictability

Xilinx Smart-IP Technology

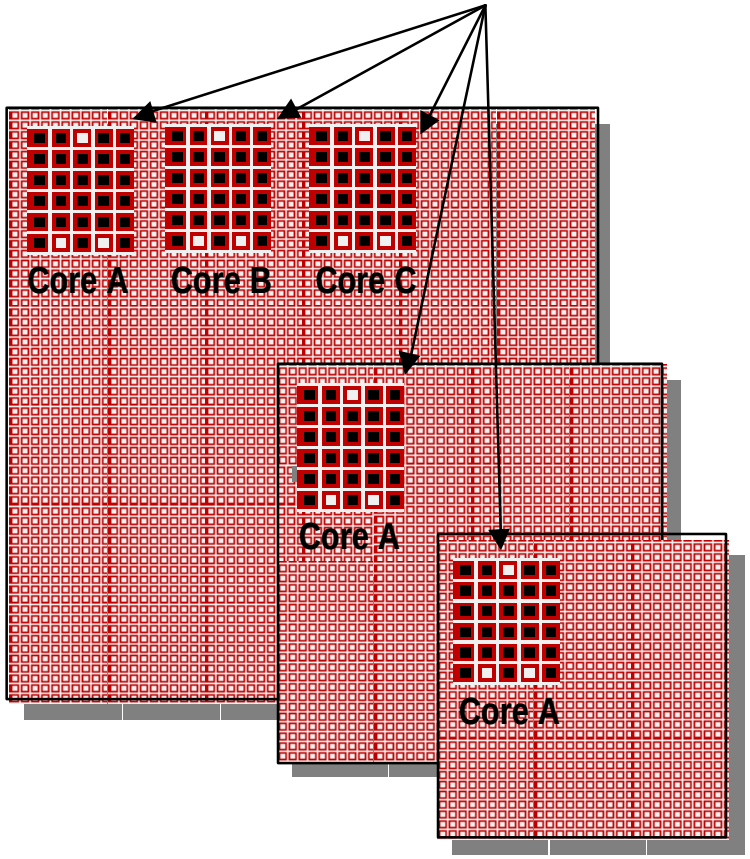
Features

- FPGA Architecture tailored to cores
  - Segmented routing
  - Distributed & block memory
- Pre-defined core placement & routing

Customer Benefits

- Performance independent of:
  - Core placement
  - Number of cores used
  - Surrounding user logic
  - Device size
  - EDA tools

Consistent performance



Spartan-II Competitive Advantage

Features	Typical Reed-Solomon ASSPs	Reed-Solomon in Spartan-II
Polynomial	Fixed	Parameterizable
Symbol Width	Fixed	Parameterizable
Block Length	Programmable (3 - 255)	Parameterizable (3 - 4095)
Correctable Errors	Programmable (1 - 10)	Parameterizable (1 - 64)
Erasure Handling	Fixed	Parameterizable
Maximum Throughput	12.5 Mbytes/sec	Decoder: 62 Mbytes/sec Encoder: 108 Mbytes/sec
Latency	1181 cycles	418 cycles
Cost (in 250k units)	$20	9.95*

* With Reed-Solomon configuration comparable to listed Typical ASSP example. The price is based on 250KU resale price for XC2S100

The Spartan-II Solution has a clear competitive advantage over stand-alone ASSPs

The Reed-Solomon Spartan-II solution is priced below ASSP prices:

Encoder and Decoder Solution = $9.95

Encoder Solution = $3.95

Viterbi

- Viterbi algorithm
  - It is a convolutional code to correct random errors
  - It minimizes the number of sequences in the trellis search as new data is received by the demodulator
  - Developed by Dr. Andrew J. Viterbi
    - Co-founder, Retired Vice chairman, Board of Directors of QUALCOMM
- Xilinx Viterbi Decoder IP is provided by CSELT
  - VITERBI_DEC Viterbi Decoder
  - Used to decode convolutional codes

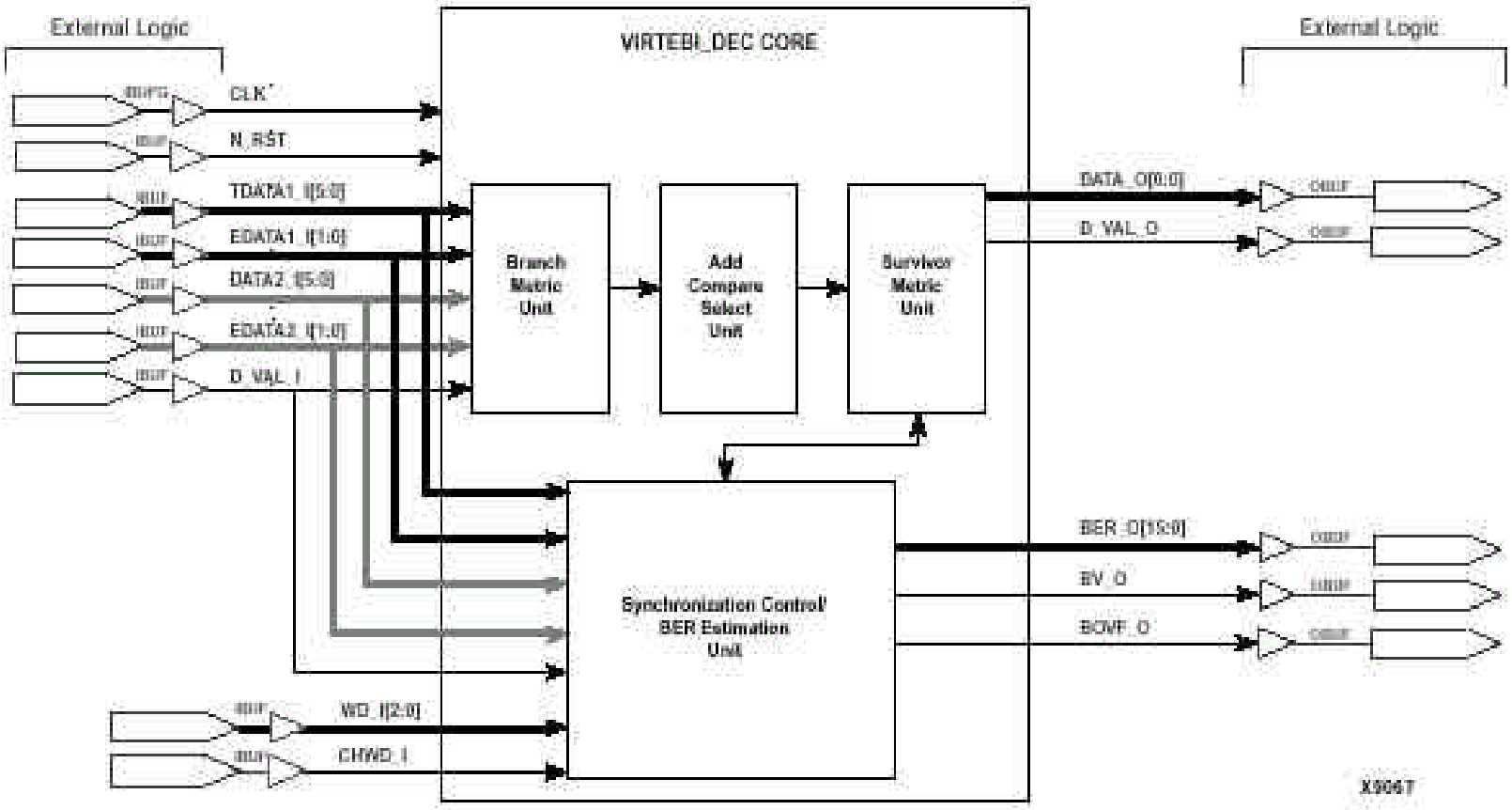
Features of the Spartan-II Based Viterbi Decoder IP

- Decoder of convolutional codes
- Customizes VHDL source code available, allowing generation of different netlist versions
- Customized testbench for pre- and post-synthesis verification supplied with the module

Features of the Spartan-II Based Viterbi Decoder IP (contd.)

- Core customization
  - Convolutional code definition parameters: Code rate; Code generation vectors; Code constraint length
  - Number of input bits per symbol bit (specifies number of quantization levels for soft decoding)
  - Traceback decision depth
  - Radix-2 / radix-4 architecture selection
  - ACS processors sharing factor
  - Optional inclusion of depuncturing unit interface
  - Optional inclusion of stream alignment/BER estimation unit
  - Estimated BER precision

Viterbi Decoder Block Diagram



Spartan-II Based Viterbi Decoder

Spartan-II FPGAs Based Viterbi Decoder Specifics	
Product Families Supported	Spartan, Spartan-II, Virtex, Virtex-E
Device Tested	XC2S50-6
CLBs	495
Clock IOBs	1
IOBs	34
Performance (MHz)	56
Special Features	4 BlockRAMs

Memory Solutions

Distributed RAM and Block RAM

Memory Controllers

Spartan-II Memory Solutions

Distributed RAM

16x1

DSP Coefficients
Small FIFOs

Block RAM

4Kx1
2Kx2
1Kx4
512x8
256x16

Large FIFOs
Video Line Buffers
Cache Tag Memory

External Memory Interface

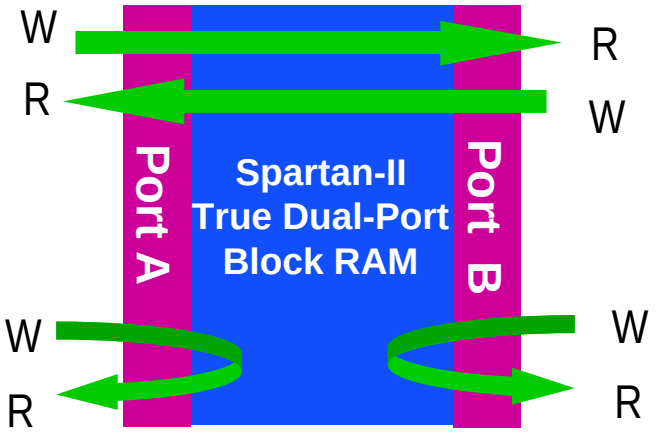
SDRAM
SGRAM
PB SRAM
DDR SRAM
ZBT SRAM
QDR SRAM

200 MHz Memory Continuum - Transparent Bandwidth

1998 1999 2000

Spartan-II Block RAM

- True Dual-port Static RAM - 4K bits
  - Independently configurable port data width
    - 4K x 1; 2K x 2; 1K x 4; 512 x 8; 256 x 16
  - Fast synchronous read and write
    - 2.5-ns clock-to-output with 1-ns input address/data setup



Data Flow	Spartan-II
A to B	Yes
B to A	Yes
A to A	Yes
B to B	Yes

Spartan-II Memory Controllers

- Spartan-II FPGAs
  - Unique and extensive features, flexible architecture, low cost
- Memory controller for interface to different types of SRAM, DRAM & Flash memory
  - Xilinx provides FREE VHDL source code for implementing the memory controllers in Spartan-II

Spartan-II Memory Controllers Reference Designs

- DRAM reference designs
  - 64-bit DDR DRAM controller
  - 16-bit DDR DRAM controller
  - SDRAM controller
- SRAM reference designs
  - ZBT SRAM controller
  - QDR SRAM controller
- Flash controller
  - NOR / NAND flash controller
- Embedded memory reference designs
  - CAM for ATM applications
  - CAM using shift registers
  - CAM using Block SelectRAM
  - Data-width conversion FIFO
  - 170MHz FIFO for Virtex
  - High speed FIFO for Spartan-II

These Reference Designs are Available for Immediate Download at the Memory Corner

Memory Corner

- Collaboration between Xilinx and major memory vendors to provide comprehensive web-based memory solutions
  - Free reference designs (VHDL/Verilog)
  - SRAM, DRAM & embedded FPGA memory solutions
  - Data sheets, app notes, tutorials, FAQs, design guidelines

Microprocessors and Microcontrollers

- 8-bit 8051 Microcontroller
- 32-Bit Reconfigurable RISC Processor

Processors & Microcontrollers

- Xilinx offers 8-bit 8051 microcontrollers
  - IP Cores by Dolphin Integration & CAST
    - CPU (with Boolean processor)
      - Includes program counter, ALU, working registers, clock circuits
    - Internal RAM, I/O ports with programmable ports, 5 or 6 interrupts, 2 or 3 16-bit counters/timers, programmable full-duplex serial port, 32 I/O lines (four 8-bit ports)

- Xilinx offers configurable 32-bit RISC processor
  - By ARC Cores

8051 µC Applications - Home

- Home networking appliances
- Bluetooth appliances
- xDSL modems
- Cable modems
- Set-top boxes
- Voice recognition
- Video-processing
- Secure surveillance systems
- TVs, HDTV, digital TV
- Home PCs & notebooks
  - CD-ROM & tape drives
  - Keyboards & mouse
  - Printers & scanners
  - Modems
  - PC & Digital Cameras
- VCRs, DVD/VCD players
- Camcorders & camera
- Remote control
- Cable TV tuner
- Microwave

8051 µC in Home & Office Applications

- Printers (Laser & Inkjet)
- Scanners
- Digital telephones
- Copiers
- Vending machines
- POS terminals
- Security systems
- Answering machines
- Fax machines
- Garage door openers
- Lighting control
- Intercom
- LCD displays

8051 µC in Automotive Applications

- Trip computer
- Engine control
- Air bag
- ABS
- Instrumentation
- Security system
- Transmission control
- Entertainment
  - Radio/Cassette/CD controls
  - CD Changers
  - GPS Navigation Systems
- Climate control
- Cellular phone
- Keyless entry

8051 µC in Other Applications

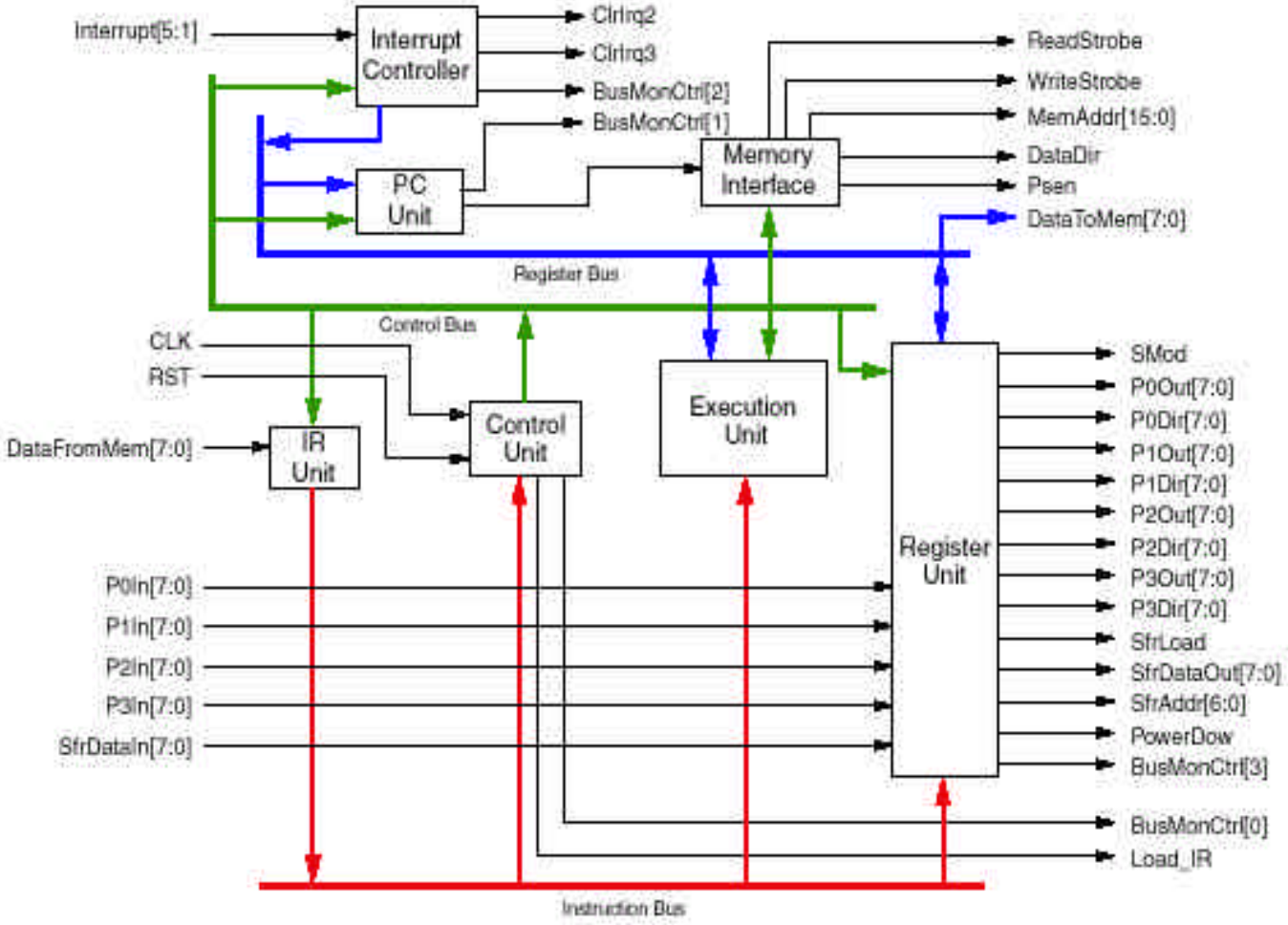
- Industrial controls
- System supervision
- Motor control
- Aerospace
- Biomedical instruments
- Telecom, datacom & networking
  - Line cards
  - Wireless: Cellular phones, pagers
  - Repeaters & Switches
- Communication through power lines
- Video games, toys, exercise equipment
- Hand-held/portable devices
- Data logging equipment
- Light-rail equipment
- Satellite base stations
- Wireless monitoring systems

Spartan-II 8051 µC Solutions

	Xilinx Spartan-II Solutions	
	Dolphin Integration	**CAST**
Speed	29.8MHz	51MHz
Performance	20 MIPS	
Memory	Dual Data Pointer, De-Multiplexed Address/Data bus	Addressable up to 256 bytes of Read/Write (internal), Addressable 64K bytes (external), Dual Data Pointer, Variable MOVX to access fast/slow RAM/Peripheral
Serial Interface	Provides 4 I/O ports	Provides 4 I/O ports
Counter/Timer	2 or 3 timers	Two 16-bit timers/counters, 15-bit programmable watchdog timer
Interrupts	6 external interrupt plus software interrupt	14 interrupt sources
Functional Description	IR Unit, Control Unit, ALU, Boolean Operation Unit, Multiply/Division Unit, Register Unit, PC Unit	8-bit Control Unit, 8-bit ALU, Memory Control Unit, RAM & SFR CU, 32-bit fast multiple/division unit

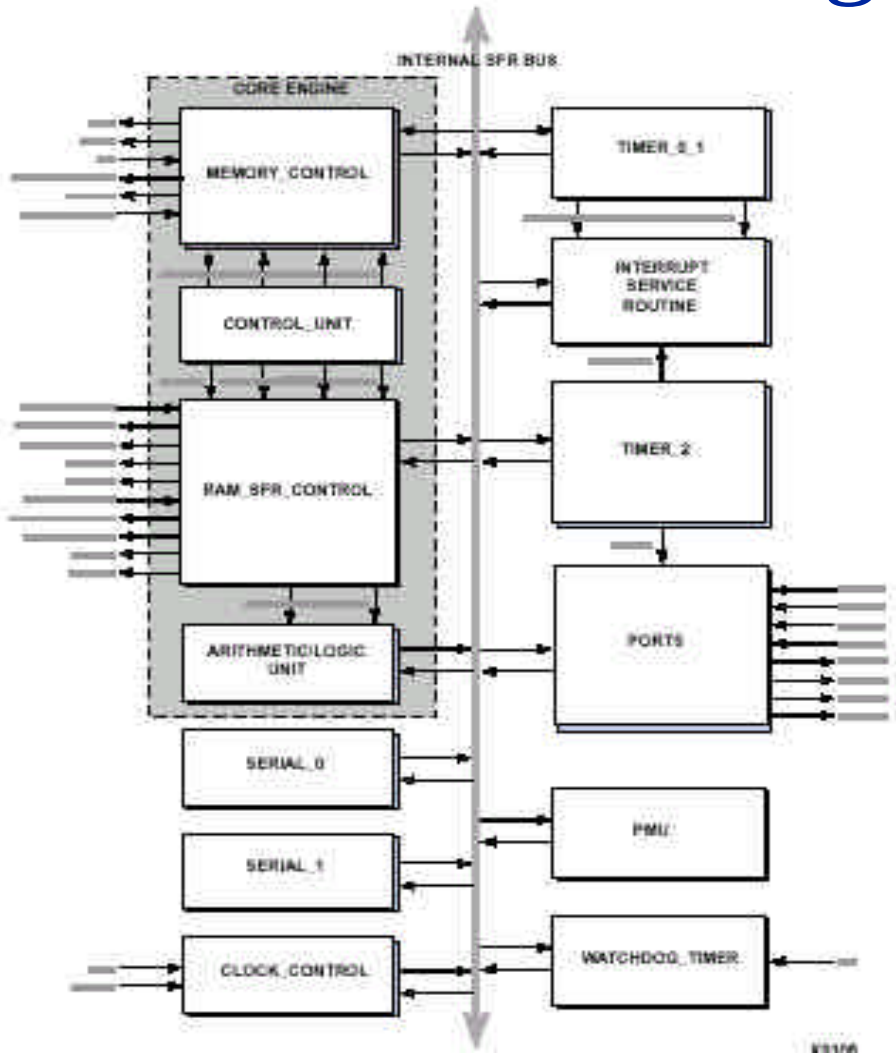
Spartan-II 8051 Solutions by AllianceCore Partners
- Dolphin Integration & CAST

Dolphin Integration

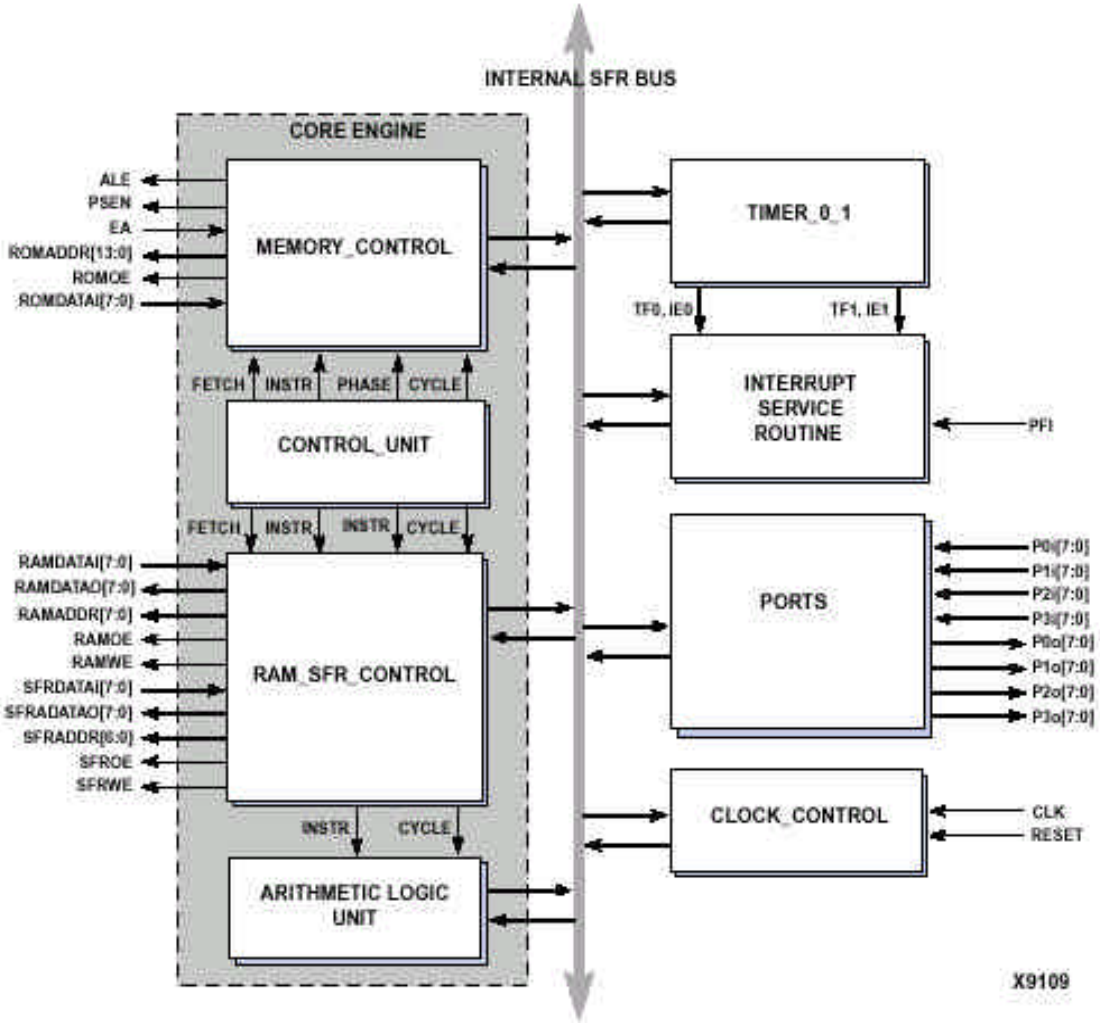


Flip805x-PR Microcontroller Core - Block Diagram

CAST - DS80530 Microcontroller Core - Block Diagram



CAST - DS80530C (Compact) Microcontroller Core - Block Diagram



Spartan-II 8-bit µC Solutions

- Spartan-II 8051 microcontroller solutions from CAST & Dolphin Integration

Features	Spartan-II Solution	
	CAST	Dolphin Integration
Spartan-II Device	XC2S150-6	XC2S150-6
CLB Slices	1515	1174
Clock IOBs	1	1
IOBs	143	
Performance (MHz)	51	29.8
Percentage Device (CLBs) Used	87.67%	67.94%

Spartan-II Value Proposition In 8-Bit µC

- High performance
  - DS80530C Core by CAST in a Spartan-II
    - Operates at 51MHz
    - Instruction execution performance equal to 2.5 times legacy 8051s
  - Flip8051 by Dolphin in a Spartan-II
    - Operates on an average 8 times faster than legacy 8051s
  - Higher performance than other 8051 ASSPs
    - Expensive (16- or 32-bit) microcontrollers are not required for higher processing power
  - Advanced power management capabilities
- High flexibility in programmable logic

Spartan-II Value Proposition In 8-Bit µC

- Advantages of programmable ASSP over ASSPs
- Embedded solutions
  - Choosing right feature set & optimization
  - Value proposition within same piece of silicon
    - FPGA logic not used from the 8051 IP can be integrate other IP
    - Product Customization
    - Reduced cost
  - High-performance “8051 + other IP” Integrated solutions
    - PCs, cable modems, set-top boxes, home networking, Bluetooth, image processing, wireless, voice recognition

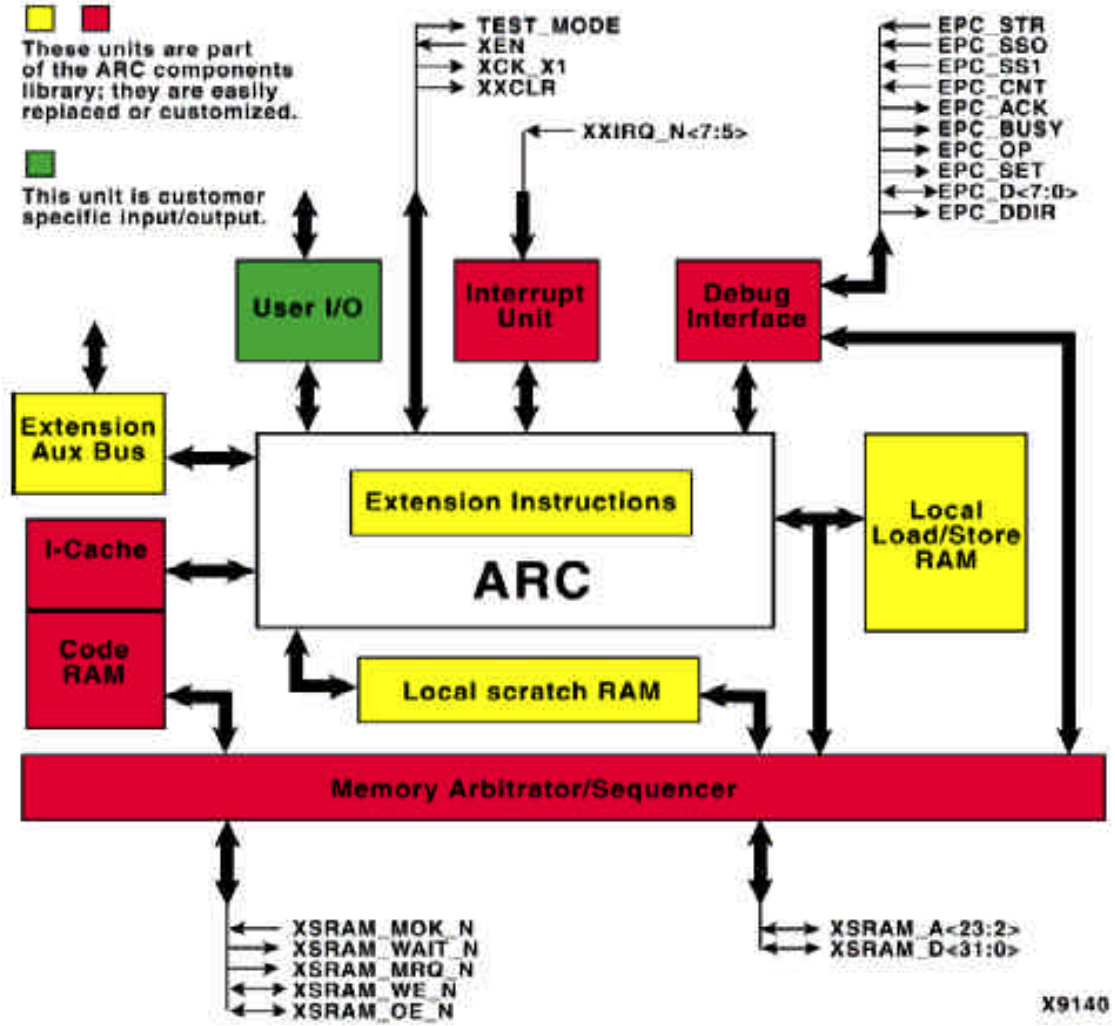
32-bit Reconfigurable RISC Processors - ARC Cores

- ARC is a configurable 32-bit RISC processor technology supplied as two generic pre-configured processor systems
  - First system is a basic (or basecase) configuration that is simply a minimal 32-bit RISC processor
  - Second configuration is a larger, but more powerful, DSP configuration
- Has been designed to make the addition of custom instructions, condition flags, special registers & custom interfaces very easy

32-Bit RISC Processor Applications

- 32-bit processing applications
  - Systems that require a 32-bit processor with custom interfaces or instructions
- DSP applications
- Network processors and routers
- Digital cameras
- Set-top boxes
- Bluetooth & wireless LAN devices
- Cellular base stations

ARC 32-bit RISC Processor System Block Diagram



32-Bit RISC Processor Implementation Data

Example Implementation	Basecase ARC	Basecase ARC
Device Tested	2S150-6	V400E-8
CLB Slices	1538	1517
Clock IOBs[1]	2	2
IOBs[1]	82	82
Performance (MHz)	37	41
Xilinx Tools	M2.1i SP6	M2.1i SP6
Special Features	9 Block RAMs	9 Block RAMs
ARC Extensions Used	2Kb I-Cache	2Kb I-Cache

32-Bit RISC Processor Features

- RISC architecture for low gate count & high performance
- Full RISC orthogonal instruction set
- 4-stage pipeline
- 16 single-cycle instructions (basecase)
- 32-bit ALU; all ALU instructions are conditional
- 32-bit data bus
- 32-bit Load/Store address bus
- 32-bit instruction bus
- 24-bit instruction address bus
- 32 general purpose core registers
- 24-bit program counter and stack pointer
- Maskable external interrupts

32-Bit RISC Processor Features

- Jumps/branches with single instruction delay slot
- Delay slot execution modes
- Zero overhead loops
- Integrated PC parallel port debug interface
  - Allows the debugger to access the processor registers and memory
- C Compiler, debugger, and simulator available from MetaWare Inc.
  - GNU version also available.
- ARCangel™ development system
  - Available for evaluation and rapid product development
- Custom versions of processor available through ARC Certified Design Centers (ACDC)

HDLC Controllers

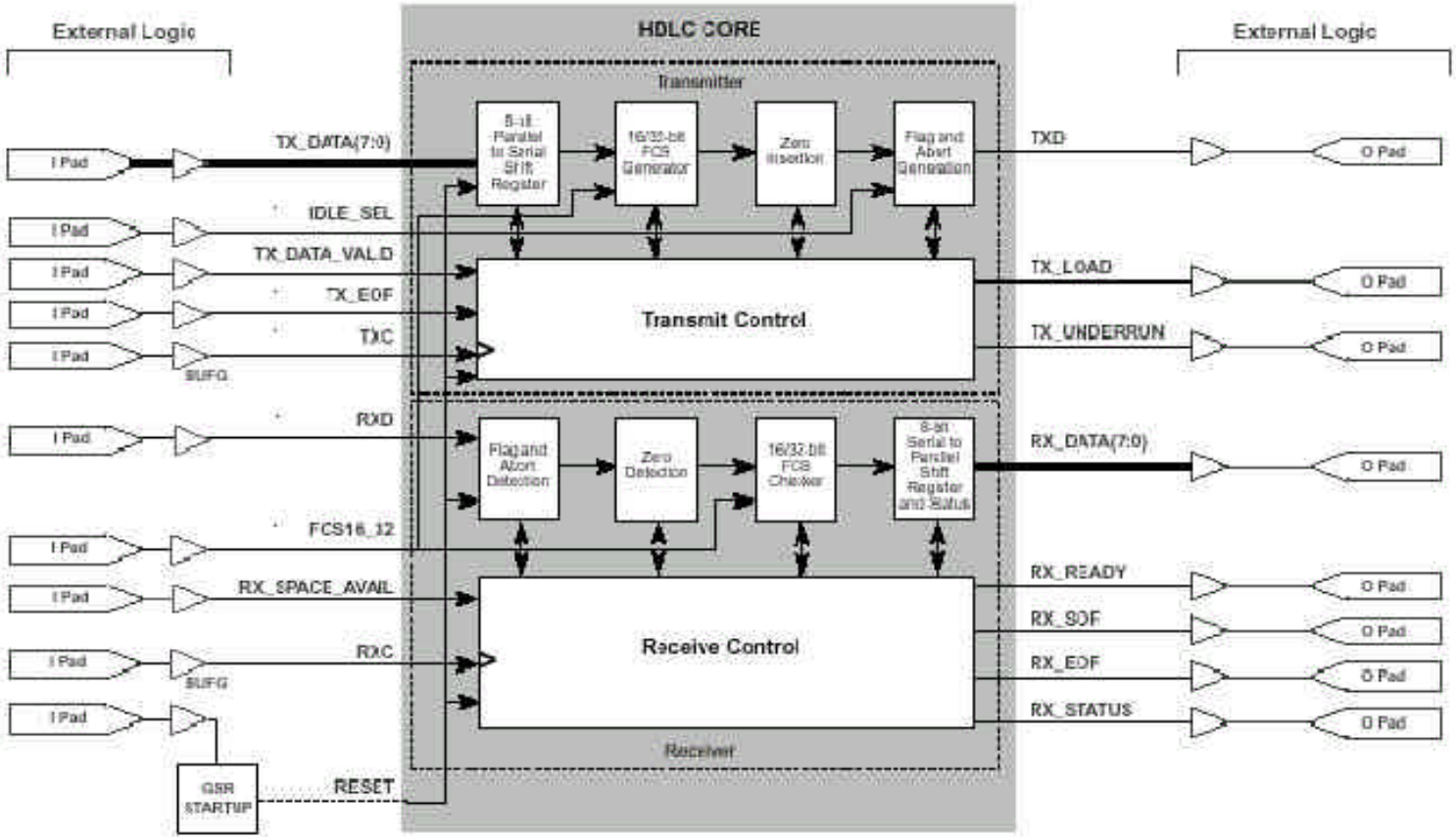
Spartan-II IP Solutions for HDLC Controllers

- Spartan-II + HDLC Controller IP = Programmable HDLC Controller Solution
- AllianceCORE partners
  - Memec Design Services
    - Single channel XF-HDLC controller core
  - CoreEl Microsystems
    - PPP8 HDLC (CC318f) controller core
- The two IP solutions are crafted to cater to different applications

Spartan-II IP Solutions for HDLC Controllers

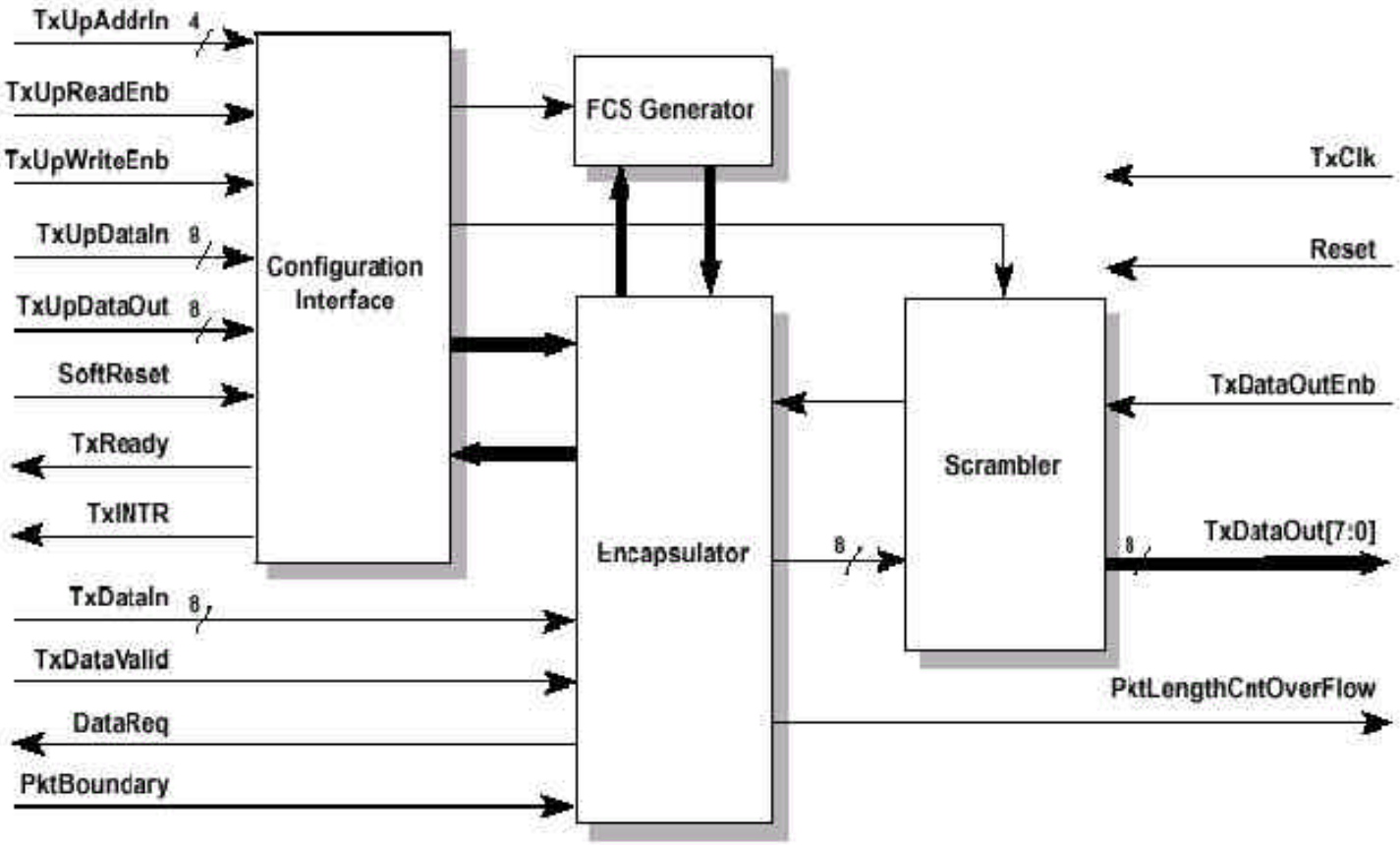
AllianceCORE Partners	Memec Design Services	CoreEl Microsystems
Products/Cores	Single Channel XF-HDLC Controller	CC318f - PPP8 HDLC
Specification Standard	International ISO/IEC3309	RFC1619 PPP over SONET
Address Recognition	N.A.	N.A.
Data Rate	DC to 53Mbps (STS-1)	N.A.
CRC/FCS	16- & 32- Bit	16- & 32- Bit
FIFO customization	Yes	N.A.
DMA customization	Yes	N.A.
Multiple HDLC Scaling	Yes	Yes
Synchronous	Full	N.A.
Features	full duplex operation allowed	supports programmable address, control, protocol fields; supports 8-bit pkt & framer interface; error detection statistics

Memec Design Services



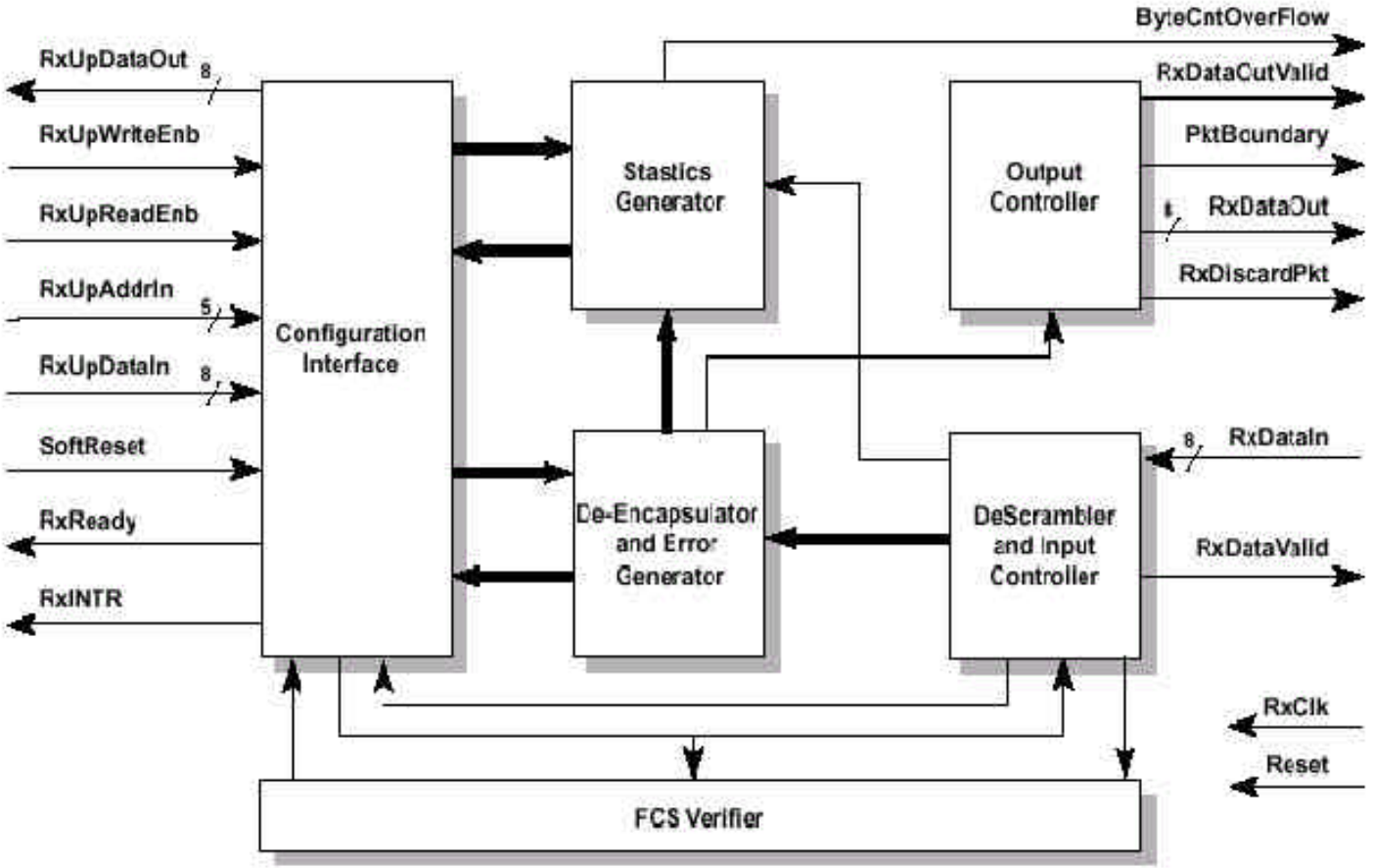
Single-Channel XF-HDLC Controller Block Diagram

CoreEL MicroSystems



CC318f HDLC Controller (Transmitter) Block Diagram

CoreEL MicroSystems



CC318f HDLC Controller (Receiver) Block Diagram

The Spartan-II Competitive Advantage: Data Rate/Throughput

- HDLC controller solution data throughput
  - Spartan-II
    - 53Mbps
  - Typical HDLC controller ASSP data throughput
    - ~ 2.5 - 8.192Mbps
- HDLC controller solution CRC
  - Spartan-II
    - 16-bit and 32-bit provided
  - Typical HDLC controller ASSP
    - No flexibility

The Spartan-II Competitive Advantage: 100k Unit Cost

- Typical HDLC controller ASSP
  - ~$4.56 (1 channel)
  - ~$60 - $120 (multi channel)
- Spartan-II HDLC controller solution
  - ~$3.95 (1 channel)
  - ~$10 (multi channel)

The Spartan-II Solution has a Clear Competitive Advantage over Stand-alone ASSPs

Conditional Access

DES/Triple DES

Others

Broadcaster Proprietary

Data Encryption for Conditional Access

- Motivation for data encryption & cryptography
  - Data privacy
    - Integrity
    - Secrecy
  - Authenticating the source of the information
- Several methods of data encryption exist
  - RSA (Rivest-Shamir-Adleman), Diffie-Hellman, RC4/RC5
  - Secure Hashing Algorithm (SHA), Blowfish
  - Elliptic Curves, ElGamal, LUC (Lucas Sequence)
  - DES (Data Encryption Standard) & Triple-DES (TDES)

DES Concept

- The Data Encryption Standard (DES) algorithm
  - Developed by IBM Corporation
  - Most prevalent encryption algorithm
  - Adopted by the US government in 1977, as the federal standard for encryption of commercial and sensitive-yet-unclassified data
  - Is a Block cipher
    - Encryption algorithm that encrypts block of data all at once, and then goes on to the next block
  - Divides 64-bit plaintext into blocks of fixed length (ciphertext)
  - Enciphers using a 56-bit secret internal key

Triple-DES Concept

- Triple-DES concept
  - More powerful & more secure
  - Equivalent to performing DES 3 times on plaintext with 3 different keys
  - TDES use 2 or 3 56-bit keys
  - With one key, TDES performs the same as DES
  - TDES implementation: serial and parallel
    - Parallel improves performance and reduces gate count

Spartan-II “Secure” Applications

- eCommerce security enabled PCs
- Cable TV
- DVD/Video CD players
- Ultrasound/MRI systems
- Bluetooth wireless systems
- Home networking
- Financial transactions
  - prepaid smart cards
  - personal banking systems
- Graphics/image processing cards
- DBS systems
- HDTV
- Cable modems
- **Set-top boxes**
- Wireless LAN
- Digital VCRs
- Digital camera

Spartan-II DES/TDES Solution

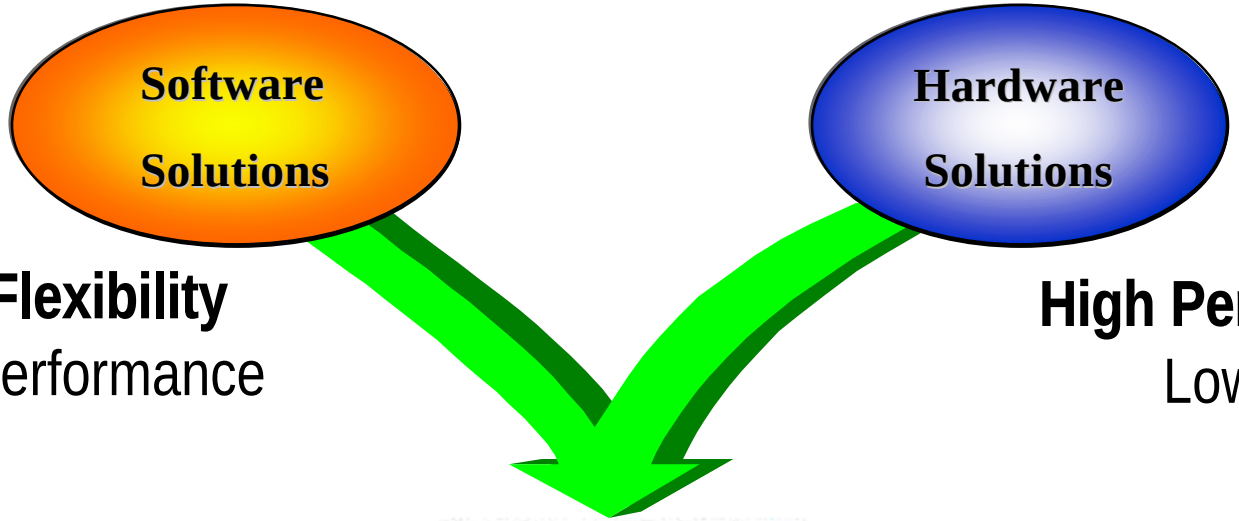
- Spartan-II DES & Triple-DES solutions
- Spartan-II DES solution is NIST approved

Features	Spartan-II Solution	
	DES	Triple - DES
Spartan-II Device	XC2S100-6	XC2S150-6
CLB Slices	235	1611
Clock IOBs	1	1
IOBs	188	244
Performance (MHz)	94	48
Percentage Device (CLBs) Used	19.58%	93.23%

Spartan-II Value Proposition in DES and Triple DES

- High performance, many features and cost effective
- High scalability and flexibility
  - Reconfigurable fabric and Internet Reconfigurable Logic
- Embedded solutions
  - FPGA logic not used from DES/Triple-DES soft IP can be used for other IP solutions
    - DCT/IDCT and DES/TDES soft IP in a Spartan-II FPGA can be used in multimedia and imaging applications
  - Increase the value proposition and reduces solution cost
- Spartan-II can be programmed with broadcaster proprietary conditional access algorithms

Spartan-II Advantages Over Hardware & Software Solutions



High Flexibility
Low Performance

High Performance
Low Flexibility

SPARTAN-II
FPGA

High Performance
High Flexibility

Enhanced Security & Performance

PCI Bus Interface

Peripheral Component Interconnect Bus (PCI)

XILINX®

PCI - Concept

- Peripheral Component Interconnect
- Originated in the PC industry
- High performance bus that provides a processor independent data path between the CPU and high-speed peripherals
- Robust interconnect mechanism developed to relieve the I/O bottlenecks
- Used in the multiple high performance peripherals for graphics, full motion video, SCSI, LAN & embedded systems

PCI End Applications

- Xilinx PCI Solutions are used in a Wide-Array of Applications:
  - Processor Bus to PCI Bus Conversions
  - Data Encryption/Decryption
  - High Speed Networking
  - Digital Video Applications
  - I/O Communications Ports
  - Memory Interfaces
  - High Speed Data Input/Output (Acquisition)
  - Multimedia Communications

Spartan-II PCI Solution Overview

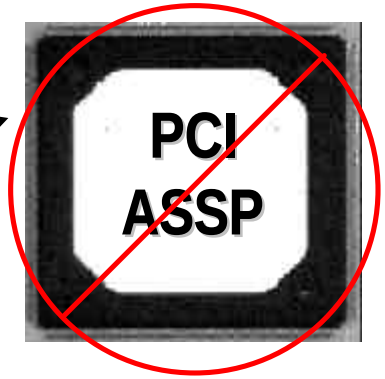
- First 64-bit PCI solution under $13
  - Supports 33 MHz PCI (50 MHz embedded designs)
- First 32-bit PCI solution under $6
  - Supports up to 66 MHz PCI Designs
- Customizable asynchronous FIFO reference designs
  - Integrate seemlessly with PCI cores

Spartan-II PCI Customer Benefits

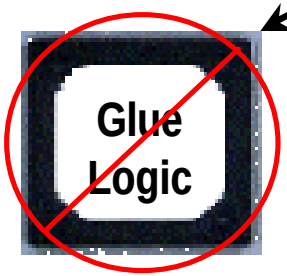
- Reduces cost over PCI ASSPs
  - Cost savings of more than 50%
- Integrate and replace system functions
  - PLL/DLL clock management devices
  - SSTL-3/HSTL translators
  - Back plane logic and Drivers
  - External Memory devices
  - System & caches controllers
- Significant time to market advantage

ASSP Replacement & Integration

System & Memory Controllers,
DLLs, Level Translators ($20)



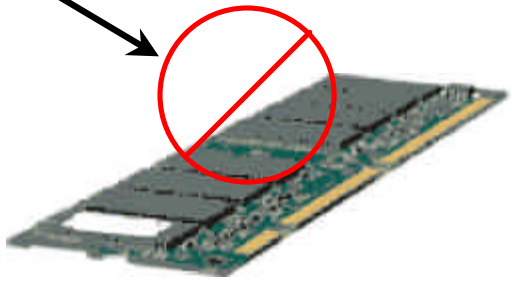
Standard Chip
PCI Master I/F ($15)



External PLD
PCI Master I/F ($5)

The **Real-PCI™**

*Supported Devices
XC2S30
XC2S50
XC2S100
XC2S150

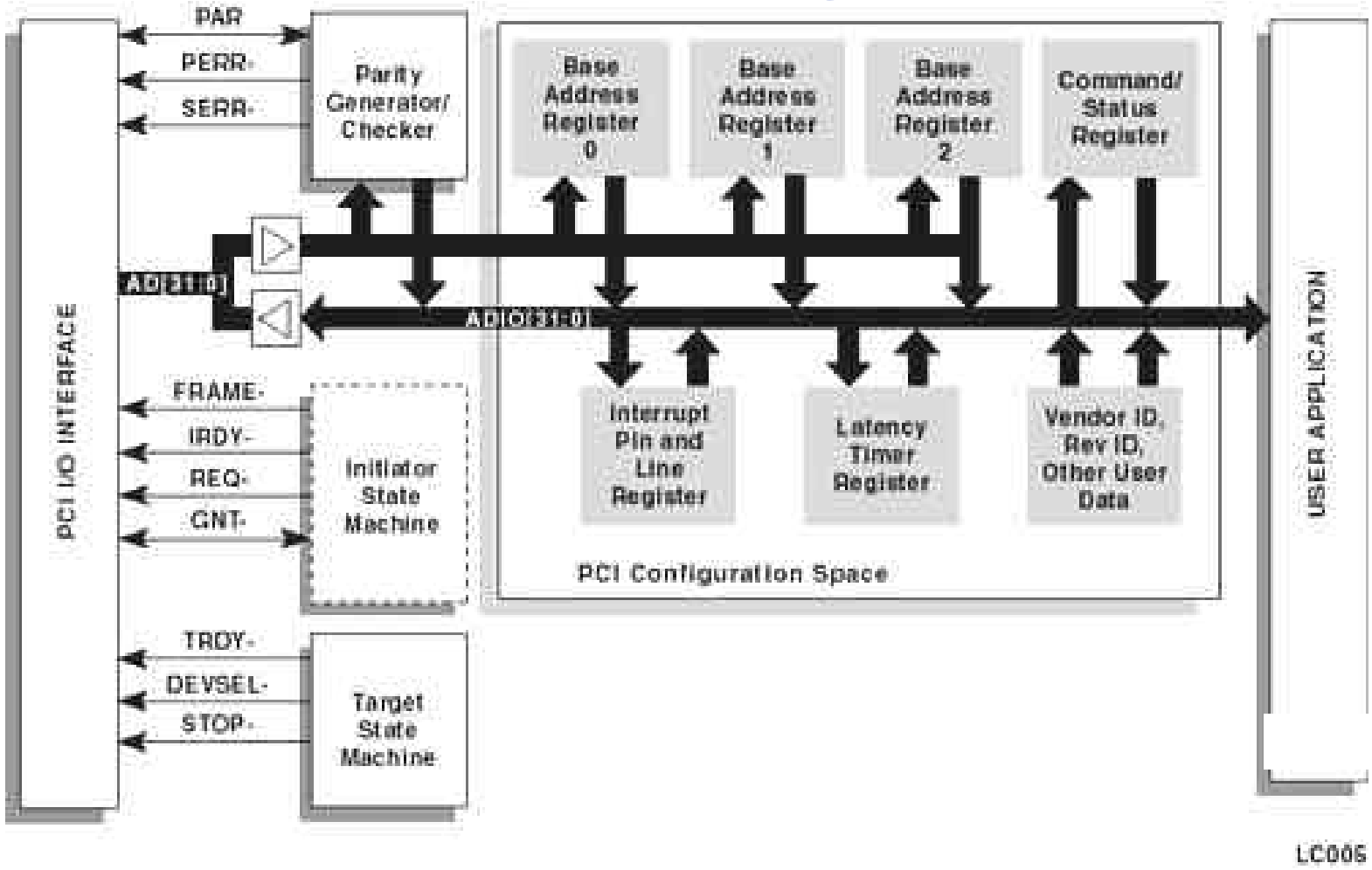


Memory ($9)

Real-PCI from Xilinx

- Real-Compliance
  - Guarantees Setup, Hold and Min/Max Clock-to-Out timing
- Real-Flexibility
  - Supports a wide range of Spartan-II devices allowing for easy device migration
  - Back-end decoupled from the PCI Interface to allow customization without affecting PCI timing
- Real Performance
  - Zero-wait state
  - Up to 264 MB/sec sustained throughput
- Real-Availability - Right Here Right Now!

Spartan-II LogiCORE PCI Block Diagram



Download Over The Internet!

Supported Synthesis Tools

SYNOPSYS®

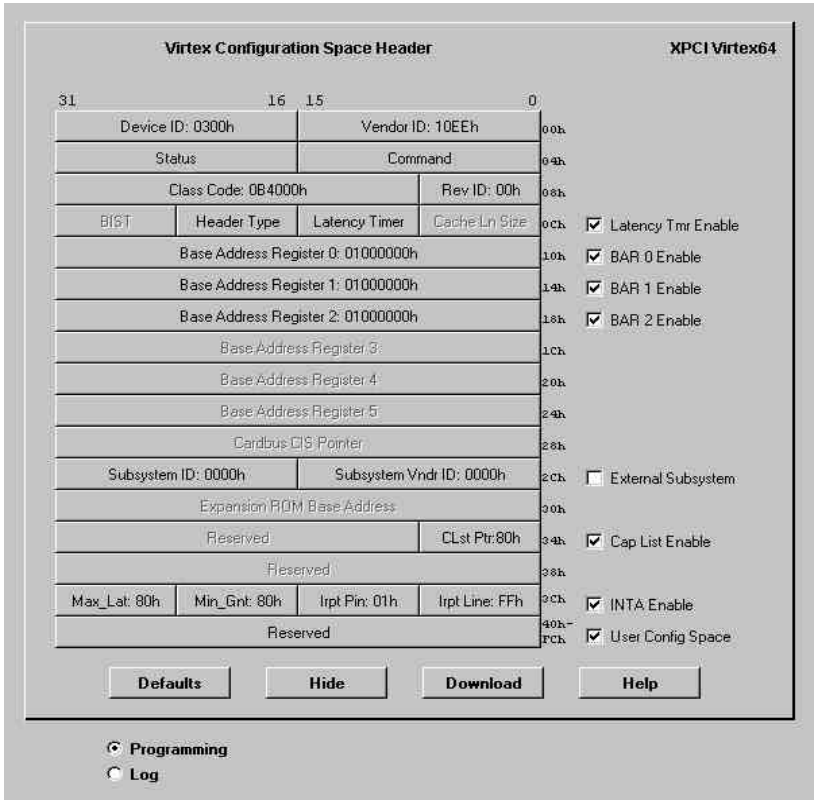
Synplicity®

exemplar

Supported Simulation Tools

Model Technology
A MENTOR GRAPHICS COMPANY

cadence

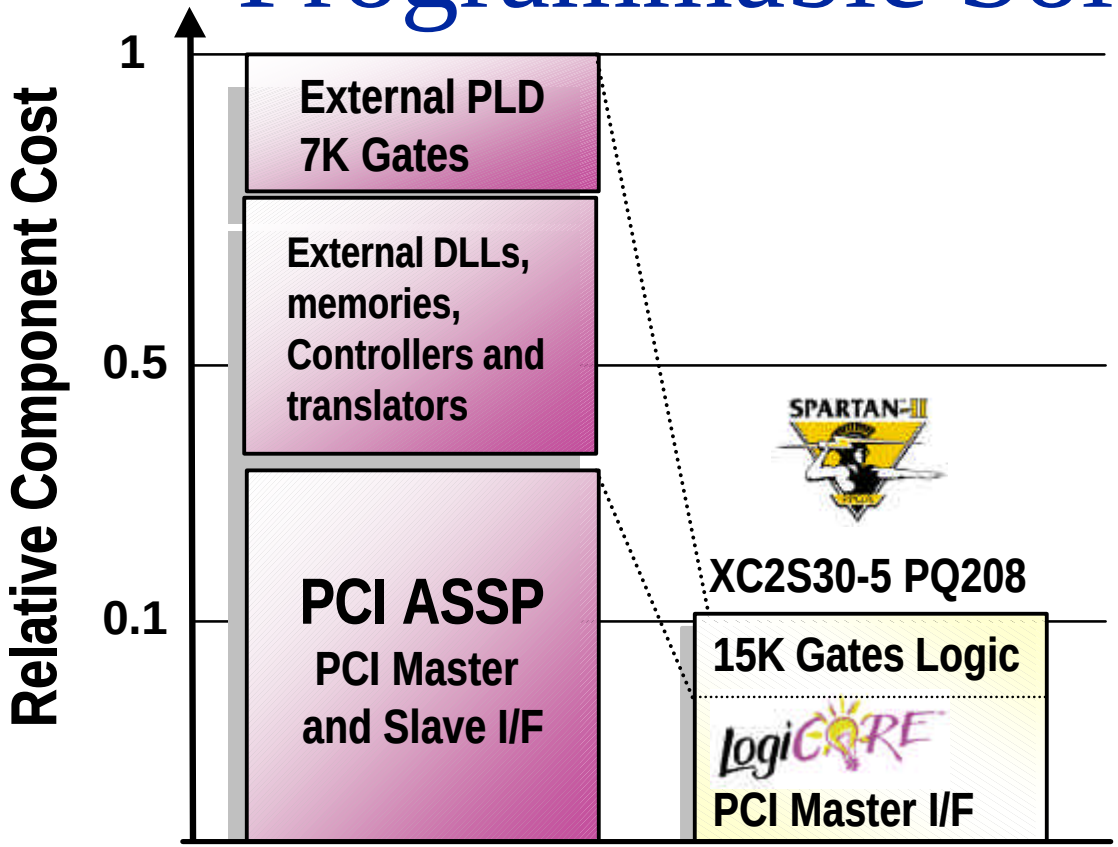


Spartan-II PCI Solutions

Spartan-II Device	PCI core	Speed	Available user-logic (system gates)	Available BlockRAM Bits
2S30	PCI 32	33 MHz 50 MHz	15K	24,576
2S50	PCI 32	33 MHz 50 MHz 66 MHz*	35K	32,768
2S100	PCI 32 PCI 64	33 MHz 50 MHz 66 MHz*	80K-85K	40,960
2S150	PCI 32 PCI 64	33 MHz 50 MHz 66 MHz*	130K-135K	49,152

* PCI32 only. Available from Xilinx PCI XPERTS partners

PCI - A Successful Programmable Solution



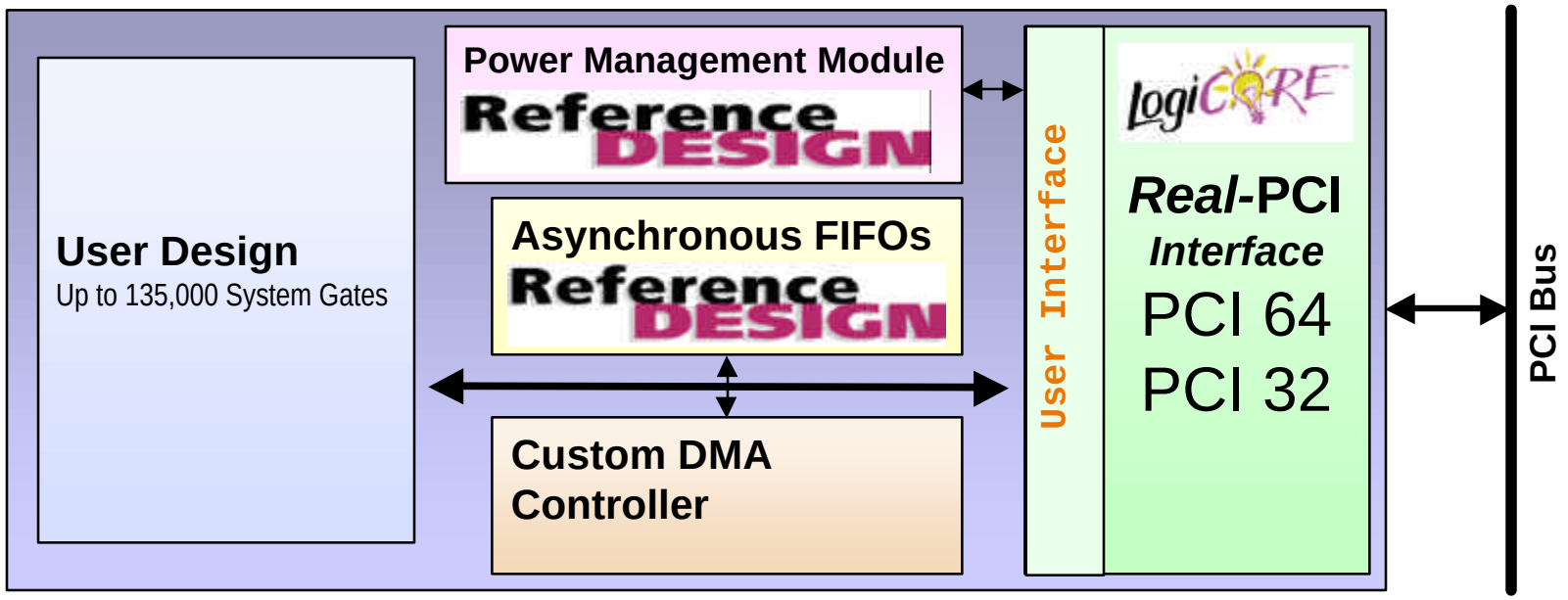
Xilinx PCI

Spartan-II FPGAs Lower Overall System Cost

The Real-PCI™ Solution ≤$6

Supporting Reference Designs

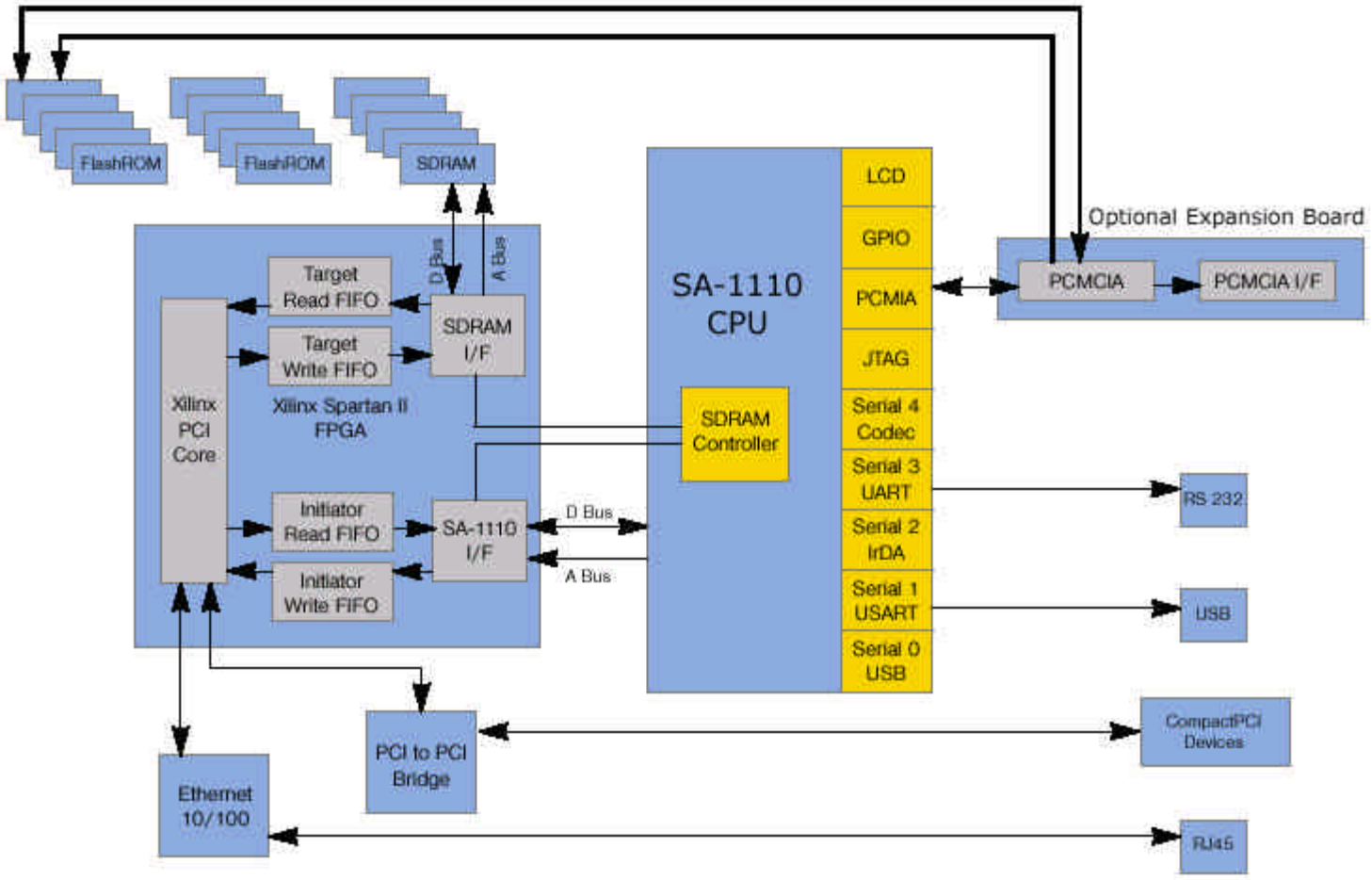
- Asynchronous FIFOs and DMA Controller
- Power Management Module



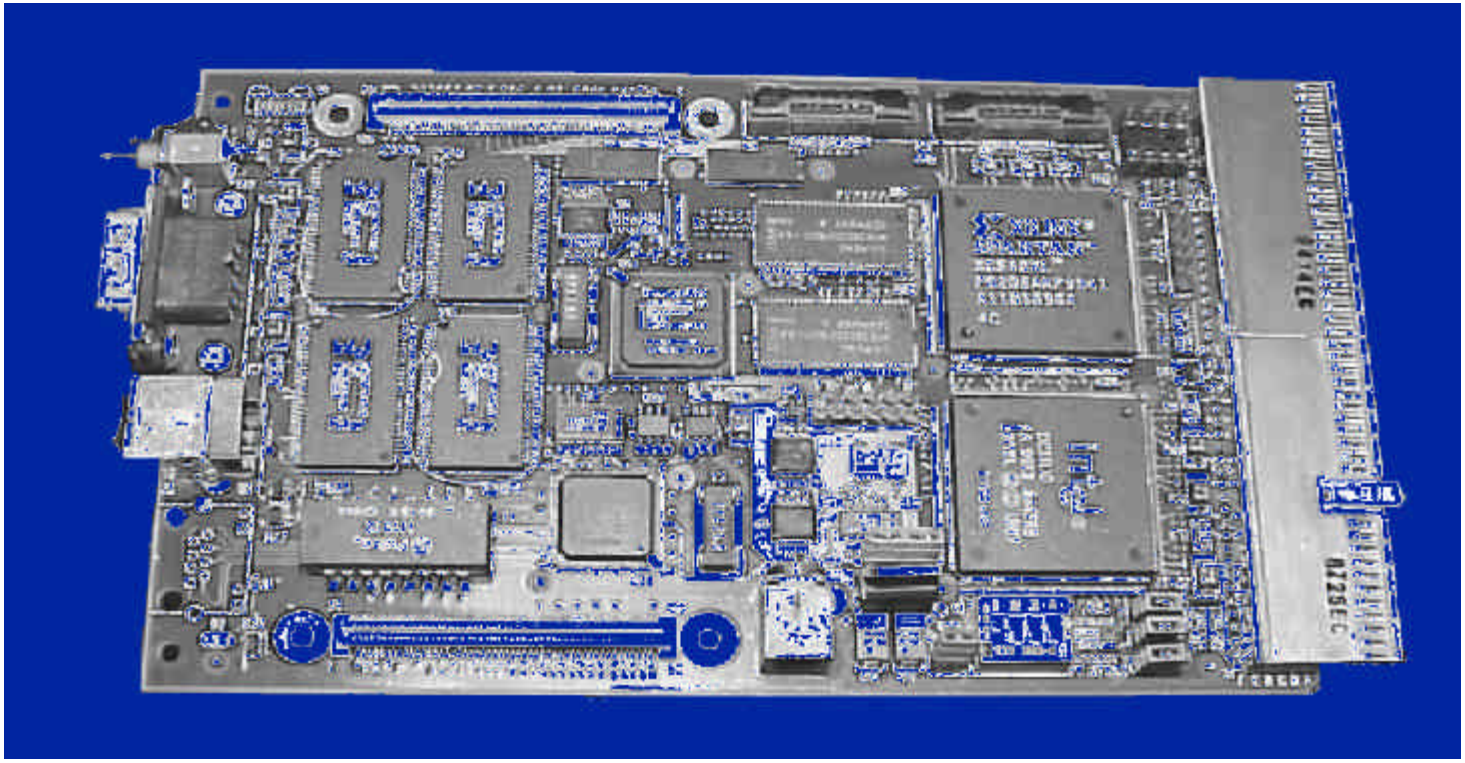
Catalyst StrongARM PCI Development Board

- Brings Time-to-Market Advantage to Embedded Systems Developers
  - Addresses a wide range of end-applications
- Xilinx Spartan-II XC2S100 implements a seamless interface between the SA1110 processor bus and the industry standard PCI bus
- Supported by Avnet Design Services
  - Engineering consulting services to customize your design and further speed your time to market
- Designed to work with Intel and third party development tools

Catalyst StrongARM PCI Development Board



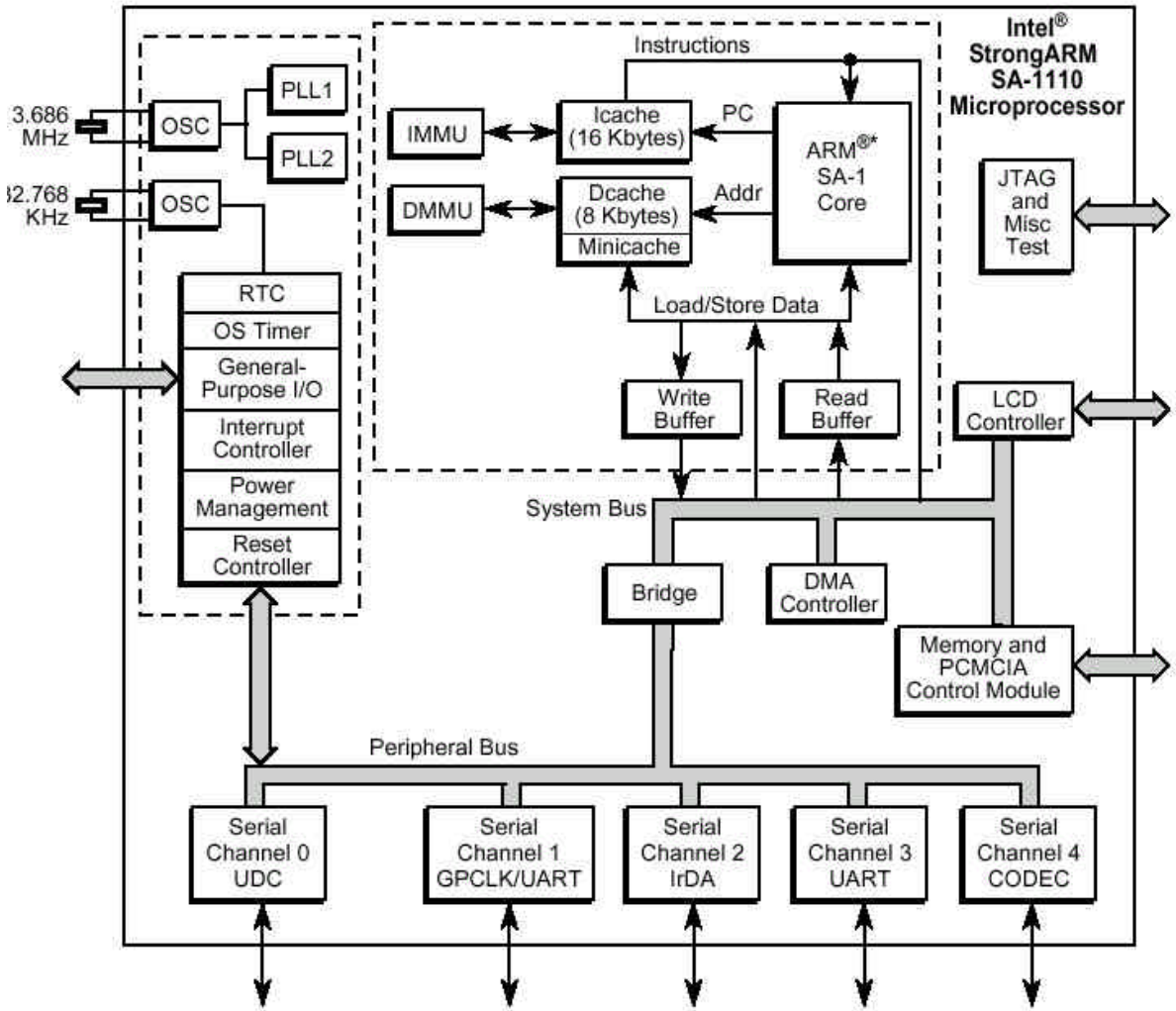
Catalyst StrongARM PCI Development Board



Catalyst StrongARM PCI Development Board

- Hardware Features
  - Intel StrongARM SA-1110
  - Xilinx Spartan II FPGA including Xilinx PCI Core IP
  - 64MB SDRAM (16Mx32)
  - 32MB of System Flash (8Mx32)
  - RS232 Serial port interface
  - Ethernet Port
  - USB client support
  - PCMCIA support cards (adapter card required)
  - IrDA support
  - Stand alone mode of operation
  - WinCE compatible

Intel StrongARM SA1110



Intel StrongARM SA1110

Performance	133 MHz	206MHz
Voltage, Power, Temperature, Process, Packaging	150 Dhrystone 2.1 MIPS	235 Dhrystone 2.1 MIPS
VDD Minimum internal power supply voltage Nominal internal power supply voltage Maximum internal power supply voltage	 1.47 V 1.55 V 1.63 V	 1.65 V 1.75 V 2.10 V
VDDX Minimum external power supply voltage Nominal external power supply voltage Maximum external power supply voltage	 3.00 V 3.30 V 3.60 V	 3.00 V 3.30 V 3.60 V
Typical power dissipation †	Normal mode = <240 mW Idle mode = <75 mW Sleep mode = <50 µA	Normal mode = <400 mW Idle mode = <100 mW Sleep mode = <50 µA
Ambient operating temperature	0°C (32°F) min 70°C (158°F) max.	0°C (32°F) min 70°C (158°F) max.
Storage temperature	–20°C to +125°C (–4°F to +257°F)	–20°C to +125°C (–4°F to +257°F)
Packaging	256 mBGA	256 mBGA
Process technology	.35 µm, 3-layer metal	.35 µm, 3-layer metal
Transistor count	2.5 million	2.5 million
Order number	GDS1110AB	GDS1110BB

† Power dissipation, particularly in idle mode, is strongly dependent on the details of the system design.

Intel StrongARM SA1110

	133 MHz	206 MHz
Unit Performance	150 MIPS	235 MIPS
Supply	1.55 V	1.75 V
USB	12 Mbps	12 Mbps
IrDA	115 Kbps, 4 Mbps	115 Kbps, 4 Mbps
UART	230 Kbps	230 Kbps
Codec	UCB1100, UCB1200, SPI, TI, µWire	UCB1100, UCB1200, SPI, TI, µWire
LCD	1-, 2-, 4-, 8-, 12-, 16-bits/pixel	1-, 2-, 4-, 8-, 12-, 16-bits/pixel
Memory	EDO, DRAM, ROM, Flash, SRAM, SMROM, and SDRAM	EDO, DRAM, ROM, Flash, SRAM, SMROM, and SDRAM
Interrupt	FIQ, IRQ, Wake-up	FIQ, IRQ, Wake-up

Development Kit Contents

- Development Board
- StrongARM PCI Module
- Xilinx PCI Core Software License
- Schematics and Bill of Materials
- 16 hours Technical Support
- Software Manuals & Datasheets

StrongARM PCI Development Kit Strengths

- Flexible Development Environment to Create Designs With the StrongARM Processor
- Variety of System Functions on the Board Make it a Good Starting Point for Most StrongARM Based Embedded Applications
- Adapt to Different Needs
  - Designers can modify the Spartan-II FPGA, to accommodate different needs
  - Something a standard product would not allow

Development Kit Pricing

Part Number	Hardware	Resale
ADS-ISTA-PCI-KIT	ADS Intel StrongARM PCI Development Kit	$8995

For Specific Details Please Visit

http://www.ads.avnet.com/solutions/strongarm/

Summary

- The Catalyst PCI Development Board offers a modular hardware development environment for StrongARM processors
  - Enables customers to speed their time to market
- Spartan-II FPGAs Offer Flexibility, Customization, and Time-to-Market Advantages at Prices lower than ASSPs
  - PCI solution at half the price of equivalent ASSP
  - 100,000 gates for $10
- Avnet Design Services
  - Engineering consulting services to customize your design and further speed your time to market

ADPCM

ADPCM Overview

- Adaptive differential pulse code modulation (ADPCM)
  - Very popular waveform coding technique
- Main application: Telecommunication
  - Speech compression for transmission, storage and reconstruction
  - Reduce the bit data rate while maintaining good voice quality
  - Technique can apply to all waveforms which need high-quality audio, image and modem data

ADPCM Overview

- ADPCM digital transcoding process
  - PCM input bit flow is 64 kbit/s (8 kHz sampling x 8-bit PCM word)
  - Process in real-time to produce a 40, 32, 24 or 16 kbit/s (8 kHz * 5, 4, 3 or 2-bit ADPCM word)
    - International Telecommunications Union
    - (ITU) ADPCM Standards
    - G.726 - 40, 32, 24, 16 kbps
    - G.723 - 40, 32, 24 kbps
    - G.721 - 32 kbps
  - ADPCM encoded voice traffic can be interchanged between packet voice, PSTN, and PBX networks

ADPCM32 Applications

- Applications
  - Wireless Local Loops (WLL) and Radio Local Loops
  - Digital cordless and PCS communication systems
    - DECT, WDCT, CT2 and PHS all specify that G.726 to be used for 32-Kbps voice channels
  - 2.4 GHz/WDCT cordless phones base stations
    - (Worldwide Digital Cordless Telecommunications)
  - Satellite communications
  - Access concentrators
  - Internet phone systems
    - VoIP
    - Voice over ATM/Frame Relay

ADPCM32 Applications

- Applications cont.
  - Computer Telephony systems
    - PBXs
    - Voice mail systems
    - H100/H110 CT
  - Video conferencing systems
    - H.323
  - Digital audio storage
  - Commercial aircraft telephony

Xilinx 32 Channel ADPCM Codec ADPCM32 Core

- Communications speech compression coder/decoder
- LogiCORE Product
  - Licensed from Integrated Silicon Systems, Ltd. (ISS)
- Low cost, fixed function netlist core
  - Virtex-E
  - Virtex
  - SpartanII
  - Future families
- Downloadable over the Internet

ADPCM32 Core Features

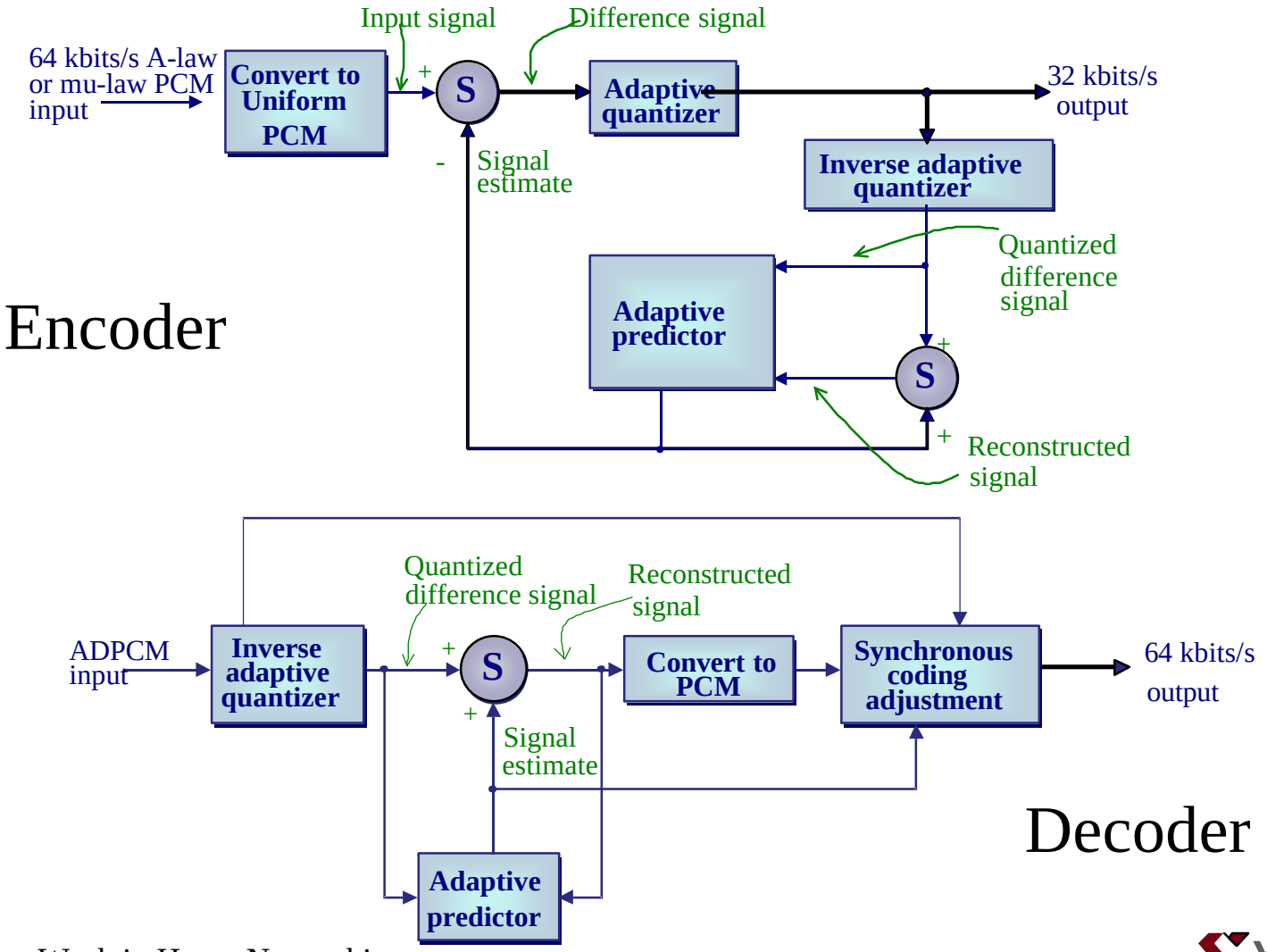
- Fully Compliant with ITU G.726, G.721and G.723
- 32 duplex channels or up to 64 independent single mode channels
- Accepts A-, µ -law and uniform PCM data and 2-5 bit ADPCM data
- On line configurable compression rate between 40,32,24 and 16 kbits/s
- On-line configurable for µ-law and A-law encoding or decoding on a channel to channel basis
- Burst and continuous mode operation
- Global and individual channel reset
- Coding of each data sample complete in 16 cycles
- Optimized for Virtex, Virtex-E and Spartan-II architectures

Example Implementations

Target Device	Virtex xcv200-6	Virtex E xcv200e-8	Spartan II xc2s150-6
Size	1822 Slices	1804 Slices	1728 Slices
Speed	16.6 MHz	21.3 MHz	17.8 MHz

- Obtainable without stringent place and route constraints

ADPCM32 Block Diagram

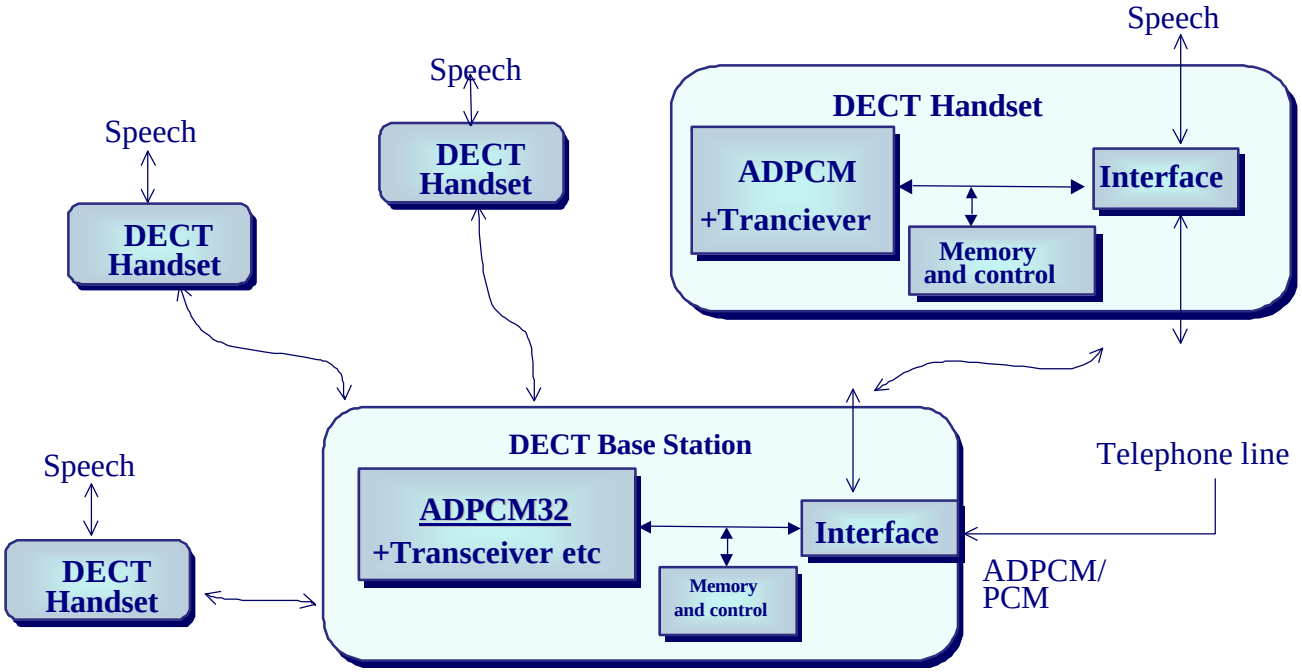


Example Application

- Digital voicemail phone system

Example Application

- DECT phone system



DECT used in a cordless Office

Summary

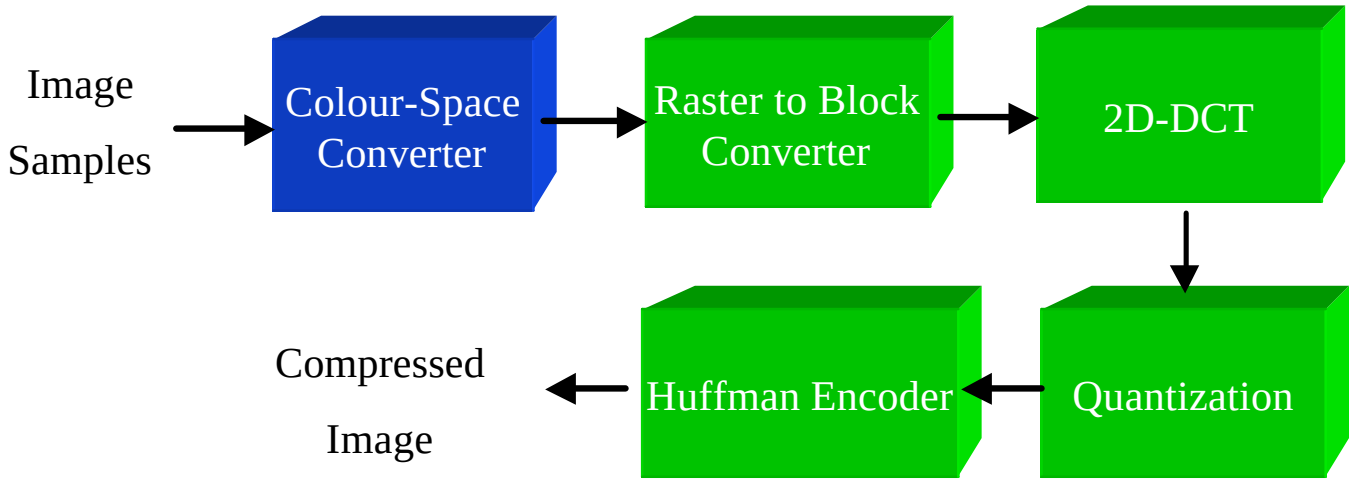
- LogiCORE ADPCM32 provides a high performance solution with a simple interface
- Compliance with all relevant standards
- Downloadable over the internet
- Easy integration into Xilinx tools flow
- Available through Xilinx CORE generator

Color Space Converters

Applications

- Many applications perform video operations in different color spaces
  - RGB : Red Green Blue
    - Color computer graphics, Color TV, Color imaging
  - YUV: Luma, U color difference, V color difference
    - Composite color video standards - PAL, NTSC and SECAM
  - YCrCb : Luma, Chroma Red, Chroma Blue
    - Broadcast television, JPEG schemes
  - Video processing can require switching between these

Example Application
Image Compression System



Implementation

Target Device Family RGB2YCrCb	Spartan II xc2s30-6	Virtex xcv50-6	Virtex-E xcv100e-8
Size	211 Slices	211	211
Speed	>65 MHz	>60 MHz	>90 MHz

Target Device Family YCrCb2RGB	Spartan II xc2s30-6	Virtex xcv50-6	Virtex-E xcv100e-8
Size	186 Slices	186	186
Speed	>70 MHz	>75 MHz	>90 MHz

Implementation

Target Device Family RGB2YUV	Spartan II xc2s30-6	Virtex xcv50-6	Virtex-E xcv100e-8
Size	230 Slices	230	230
Speed	>80 MHz	>75 MHz	>100 MHz

Target Device Family YUV2RGB	Spartan II xc2s15-6	Virtex xcv100-6	Virtex-E xcv100e-8
Size	147 Slices	147	147
Speed	>65 MHz	>75 MHz	>100 MHz

Competitive Analysis

Feature	Perigee Core	Xilinx LogiCore	Perigee Core	Xilinx Logicore
Product/Cores	RGB2YCrCb	RGB2YCrCb	YCrCb2RGB	YCrCb2RGB
Size:				
Virtex / Virtex-E	266 Slices	211 Slices	188 Slices	186 Slices
Synchronous	Full	Full	Full	Full
Supported Family	4000X, Spartan, Spartan-II, Virtex, Virtex-E	Spartan-II, Virtex, Virtex-E	4000X, Spartan, Spartan-II, Virtex, Virtex-E	Spartan-II, Virtex, Virtex-E
Latency	6 Clock Cycles	3 Clock Cycles	6 Clock Cycles	3 Clock Cycles
Performance:				
Virtex	165 MHz	>60 MHz	154 MHz	>75 MHz
Virtex-E	202 MHz	>90 MHz	230 MHz	>90 MHz
SDTV (27 MHz) Time Multiplexed Channels	6 (Virtex) 7 (Virtex E)	2 (Virtex) 3 (Virtex E)	5 (Virtex) 8 (Virtex E)	2 (Virtex) 3 (Virtex E)
HDTV (75 MHz) Time Multiplexed	2 (Virtex) 2 (Virtex E)	N/A (Virtex) 1 (Virtex E)	2 (Virtex) 3 (Virtex E)	1(Virtex) 1 (Virtex E)
Cost	$2,500	$995	$2,500	$995

Summary

- LogiCORE Color Space Converters provide straight forward, accurate high performance conversion useable in a wide range of video/image applications
- More area efficient than existing cores
- Speeds ensure operation in all TV and HDTV applications
- Available through Xilinx Coregen

System Interconnectivity

DMA Controller

Keyboard Display Interface

UARTs

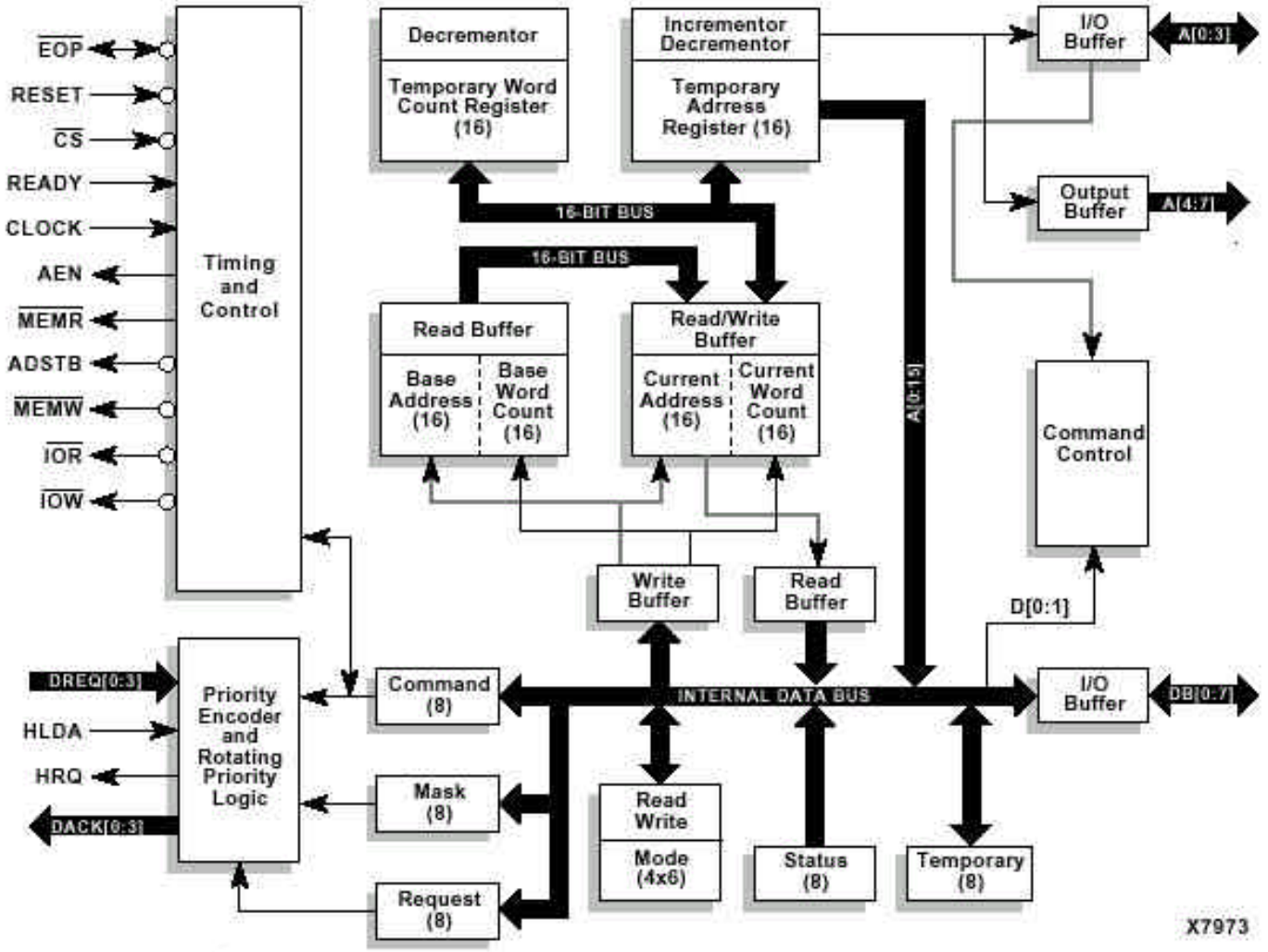
DMA Controller

- Multi-mode Direct Memory Access (DMA) controller
  - IP Core provided by Virtual IP Group
- Applications
  - Multi-mode Programmable, multi-channel DMA
  - Support Controller for Microprocessor based systems

DMA Controller Features

- Functionally compatible to Intel 8237
- Four independent DMA channels
- Independent auto-initialization of all channels
- Directly expandable to any number of channels
- Memory-to-memory transfers
- Memory block initialization
- Software DMA request
- Enable/disable control of individual DMA requests
- Address increment/decrement selection control for all channels
- High performance transfers up to 1.6 MBytes/sec with 5MHz
- End of process input to terminate transfers
- Programmable polarity control for DMA Request and DACK signals

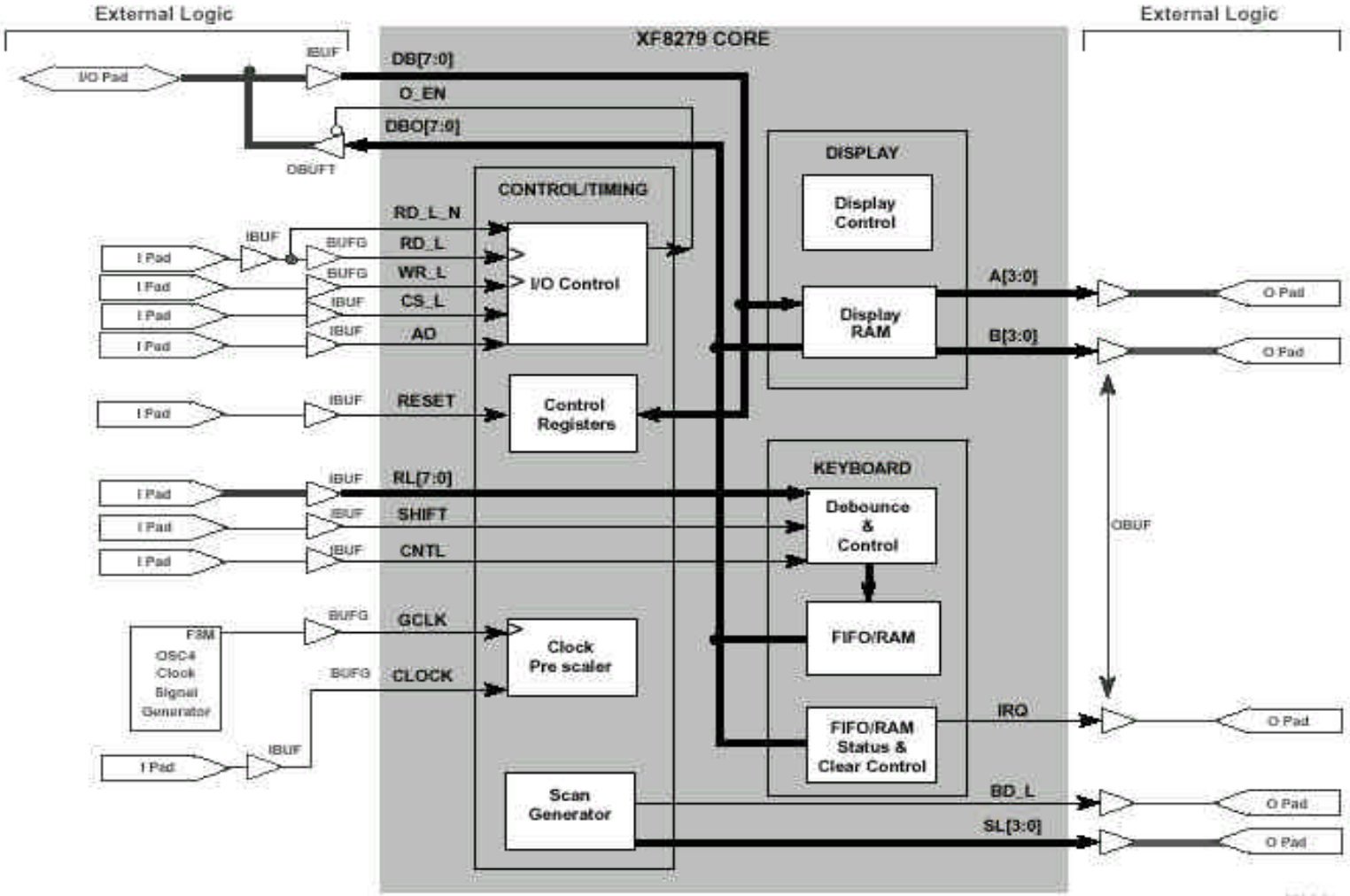
DMA Controller Block Diagram



Keyboard Display Interface

- Programmable keyboard display interface
  - IP core is provided by Memec Design Services
- Application
  - User interface for embedded systems
- Features
  - Compatible with Xilinx CORE Generator tool
  - Simultaneous keyboard & display operations
  - Scanned keyboard mode & scanned sensor mode
  - 8-character keyboard FIFO
  - Dual 4, 8 or 16 numerical display & single 8 or 16 character display

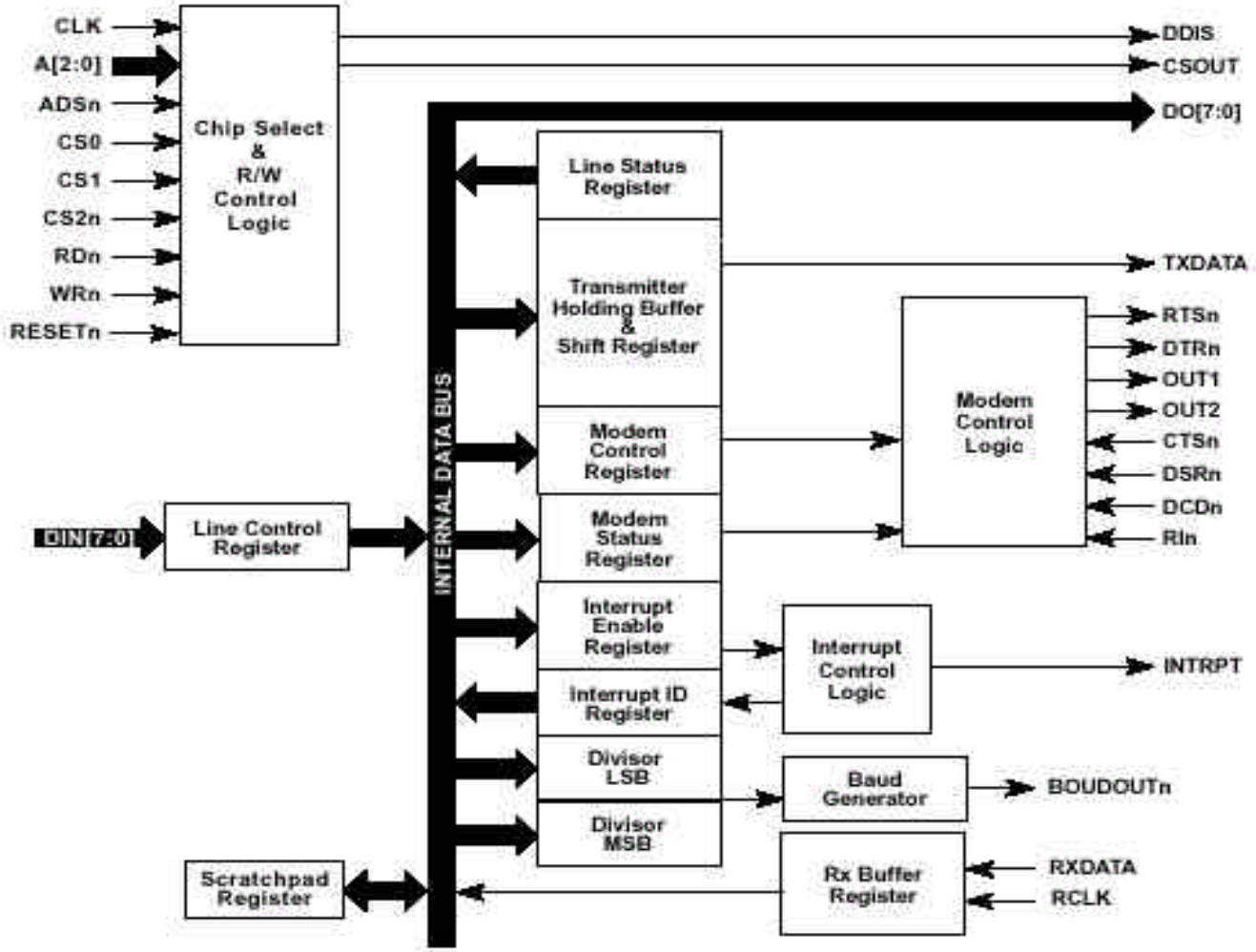
Programmable Keyboard Display Interface Block Diagram



UARTs (Universal Asynchronous Receiver / Transmitter)

- UART variations
  - With FIFOs, with RAM, compact
  - IP providers: CAST, Memec Design Services, Virtual IP Group
- Applications
  - Serial data communications & modems
- Features
  - Full double buffering, asynchronous operation
  - Independently controlled Transmit, Line Status, Receive & data set interrupts
  - Programmable data word length (5 - 8 bit), parity & stop bits
  - Parity, overrun and framing error checking

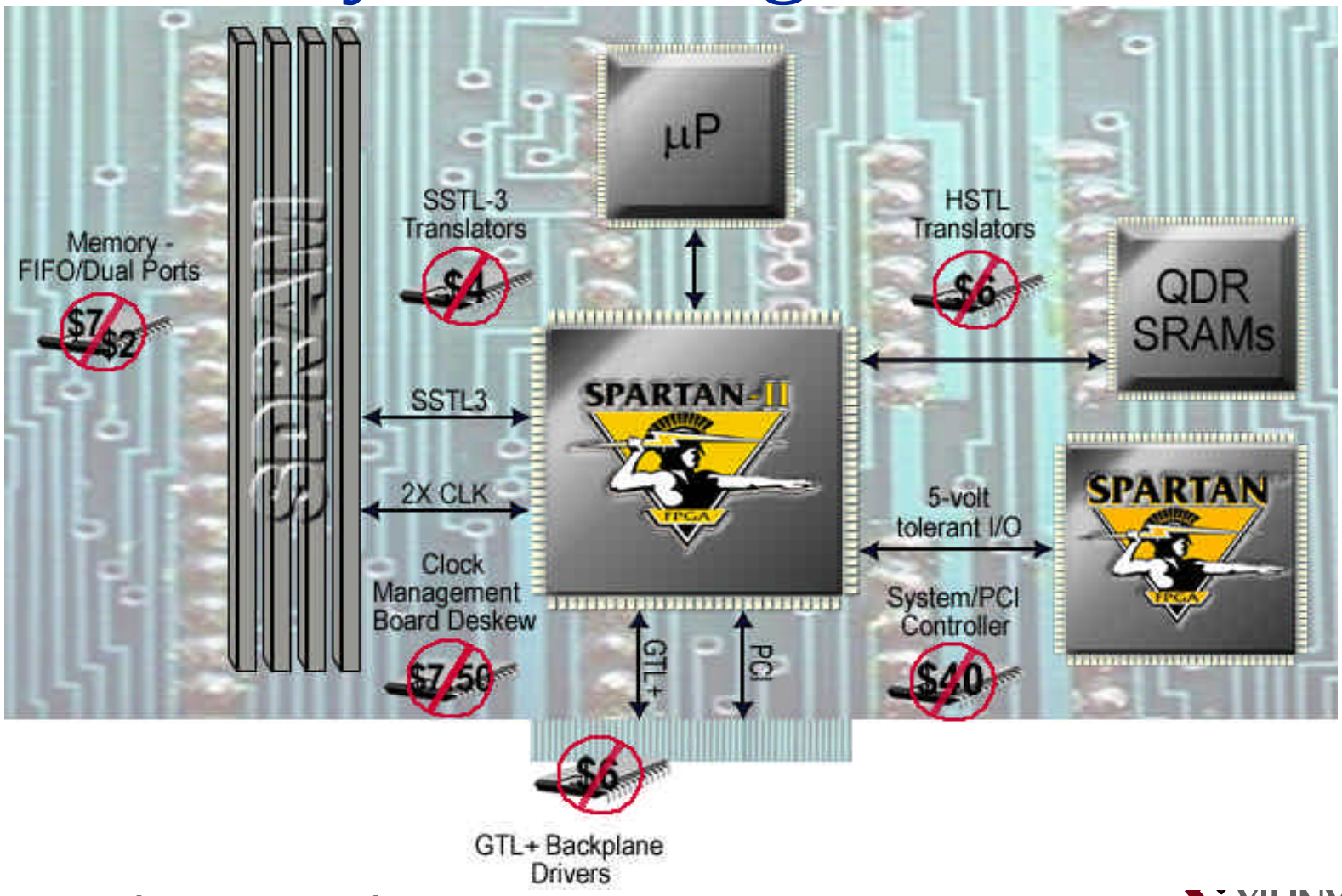
UART Block Diagram



UART Core Implementation Data

Supported Family	Device Tested	CLB Slices[2]	Clock IOBs	IOBs[1]	Performance (MHz)
Virtex	V50-6	225	1	40	66
Virtex-E	V50E-8	225	1	40	77
Spartan-II	2S50-6	225	1	40	60

Spartan-II Features Provide System Integration



Summary

- Spartan-II FPGAs + IP cores enable home networking products
  - Provide solutions (functionality and performance) like ASSPs
  - Provide flexibility that is unparalleled to ASSPs
    - Embedded solutions : FPGA logic not used from IP can be programmed with other IP cores
      - Example: DCT/IDCT and DES/TDES soft IP in a Spartan-II FPGA can be used in multimedia and imaging applications
      - Increases the value proposition and reduces solution cost
  - Features within the Spartan-II FPGAs provide system integration
  - Reprogrammability enables time-to-market & flexibility
  - Internet Reconfigurable Logic allows time-in-market as specs in emerging technologies keep evolving
  - Cost effective

Summary

- I/O control
  - Multiple front end interfaces
  - Multiple back end interfaces
- Hard disk drive interface
- Clock distribution
  - DLLs
- MPEG decoder
- Ethernet MAC
- Error correction
  - Reed-Solomon, Viterbi
- PCI
- Memory solutions
  - On-chip Distributed memory, BlockRAM
  - Memory controllers
- CPU / microcontroller
- HDLC controller
- ADPCM
- Color Space Converters
- Glue logic & system integration
  - LCD controllers, UARTs, DMA controllers