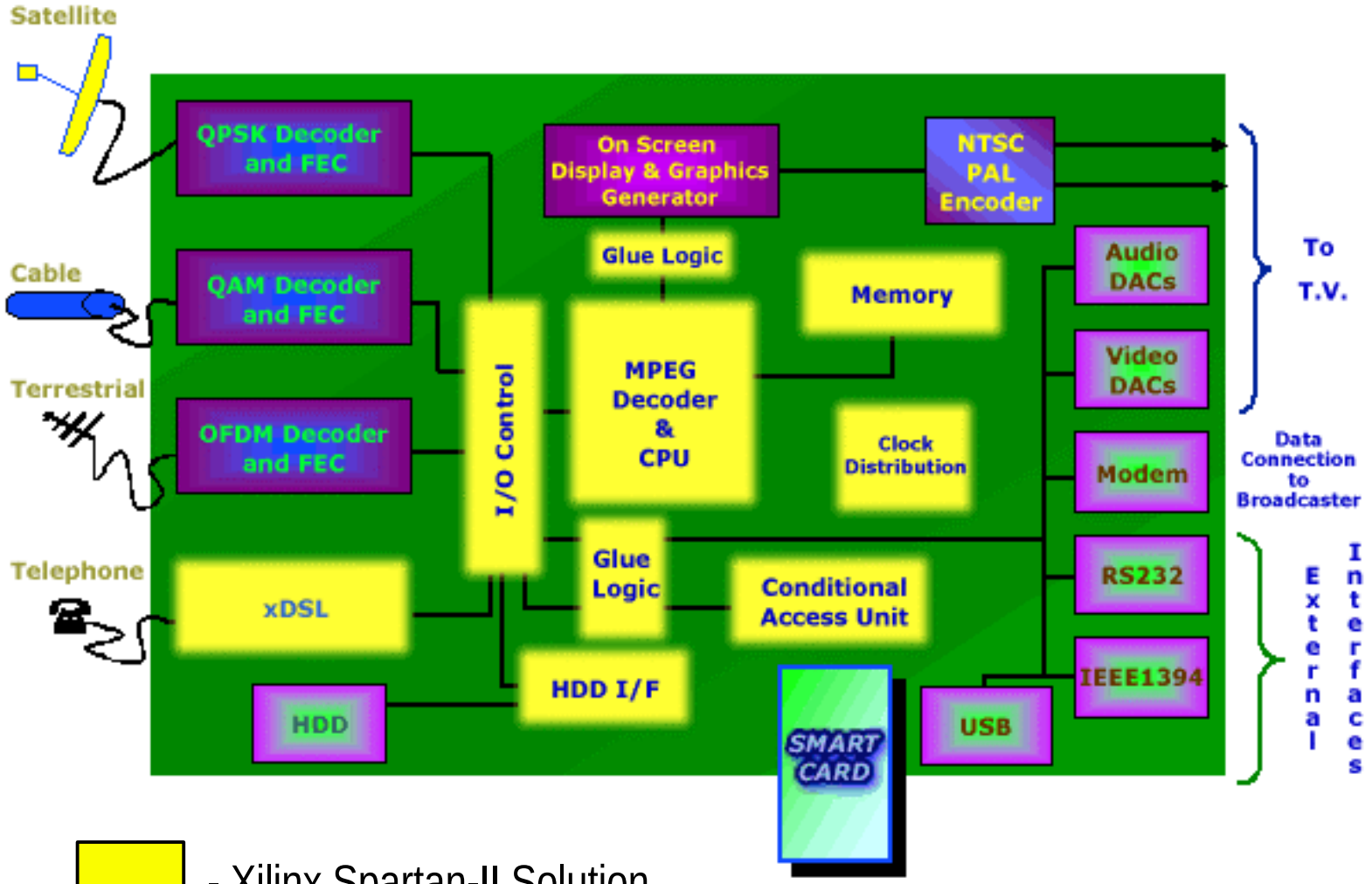
Set-Top Box - Block Diagram

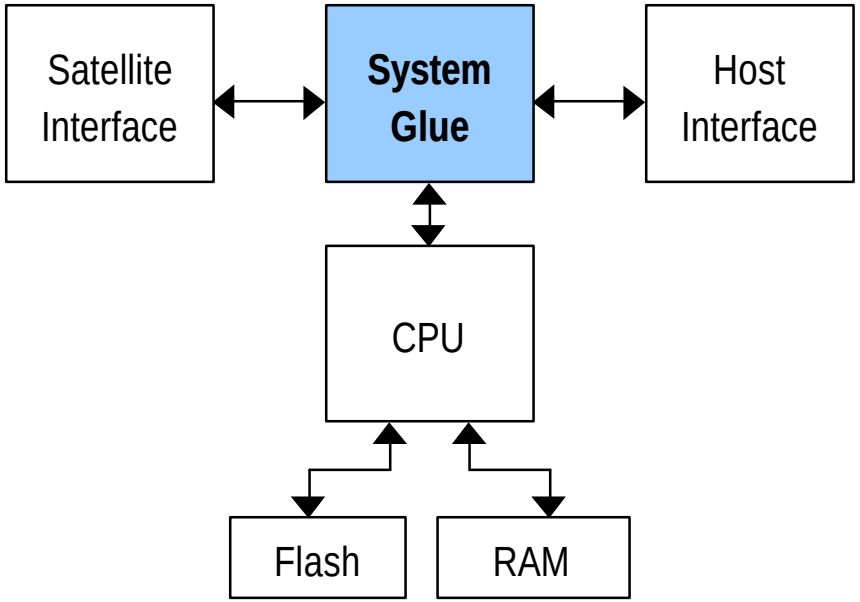


- Xilinx Spartan-II Solution

Set-Top Box Technology

- Cable
  - Uses cable network to supply the TV channels
  - Can use same network connection for PCs
- xDSL
  - Employs adaptive digital modulation technologies to achieve increased data rates (1.5 Mbps - 8 Mbps)
- Satellite
  - Broadcasts to the home via satellite and dish-aerial
- Terrestrial
  - Broadcast via ground based transmitters in the same way as analog TV using old analog aerial

System Block Diagram

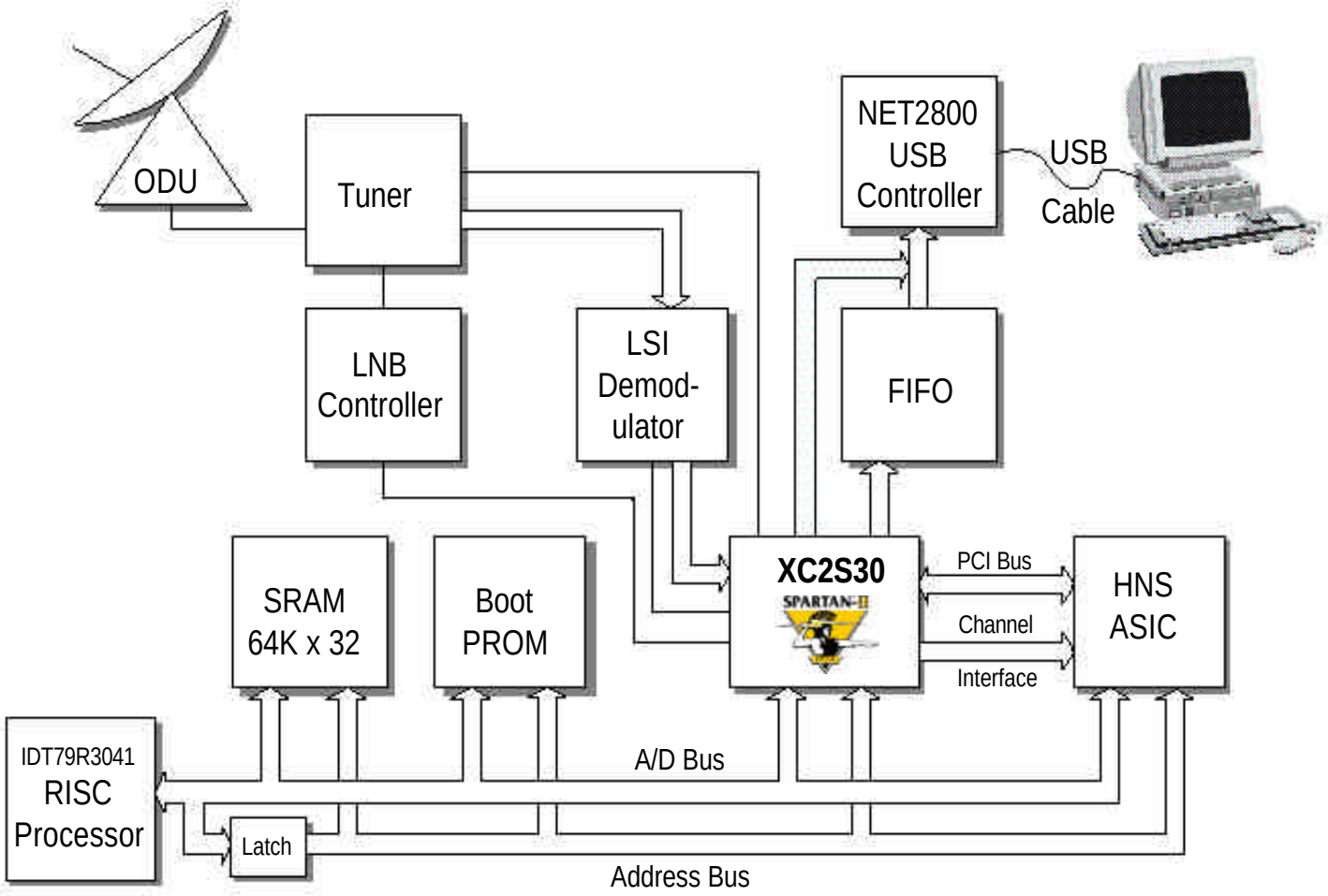


- Key functional blocks
  - Satellite interface
  - CPU complex
  - Host interface
  - Application specific system glue
- Application specific system glue required for interconnecting ASSPs

Satellite Modem Design

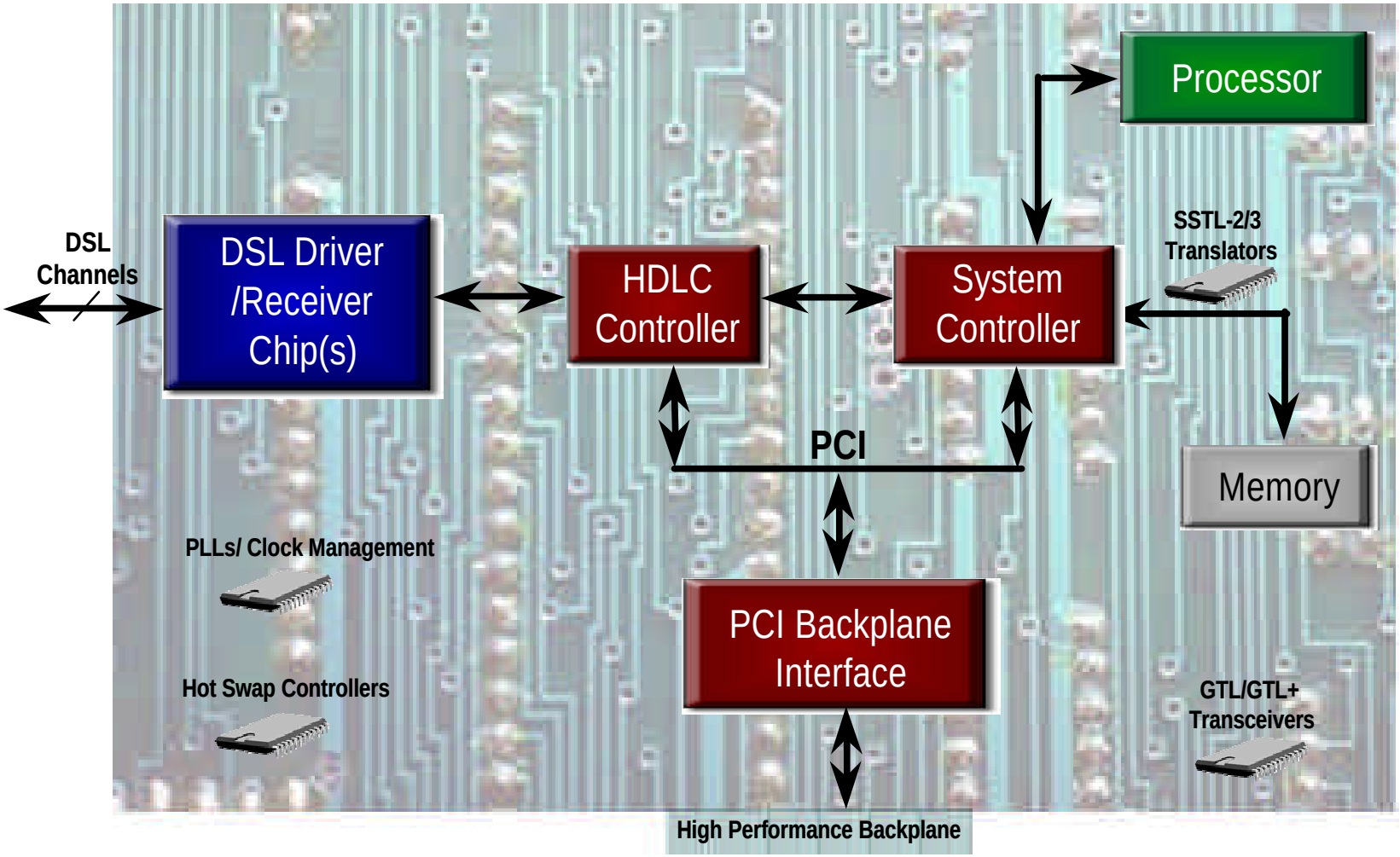
- Hughes Network Systems DirecPC®-USB receiver
- The challenge
  - Add USB interface to satellite modem architecture
  - Leverage ASIC technology developed for PCI card
- Spartan-II XC2S30 used for system level glue, interfaces:
  - CPU
  - Demodulator
  - HNS ASIC
  - USB controller

Satellite Modem Block Diagram

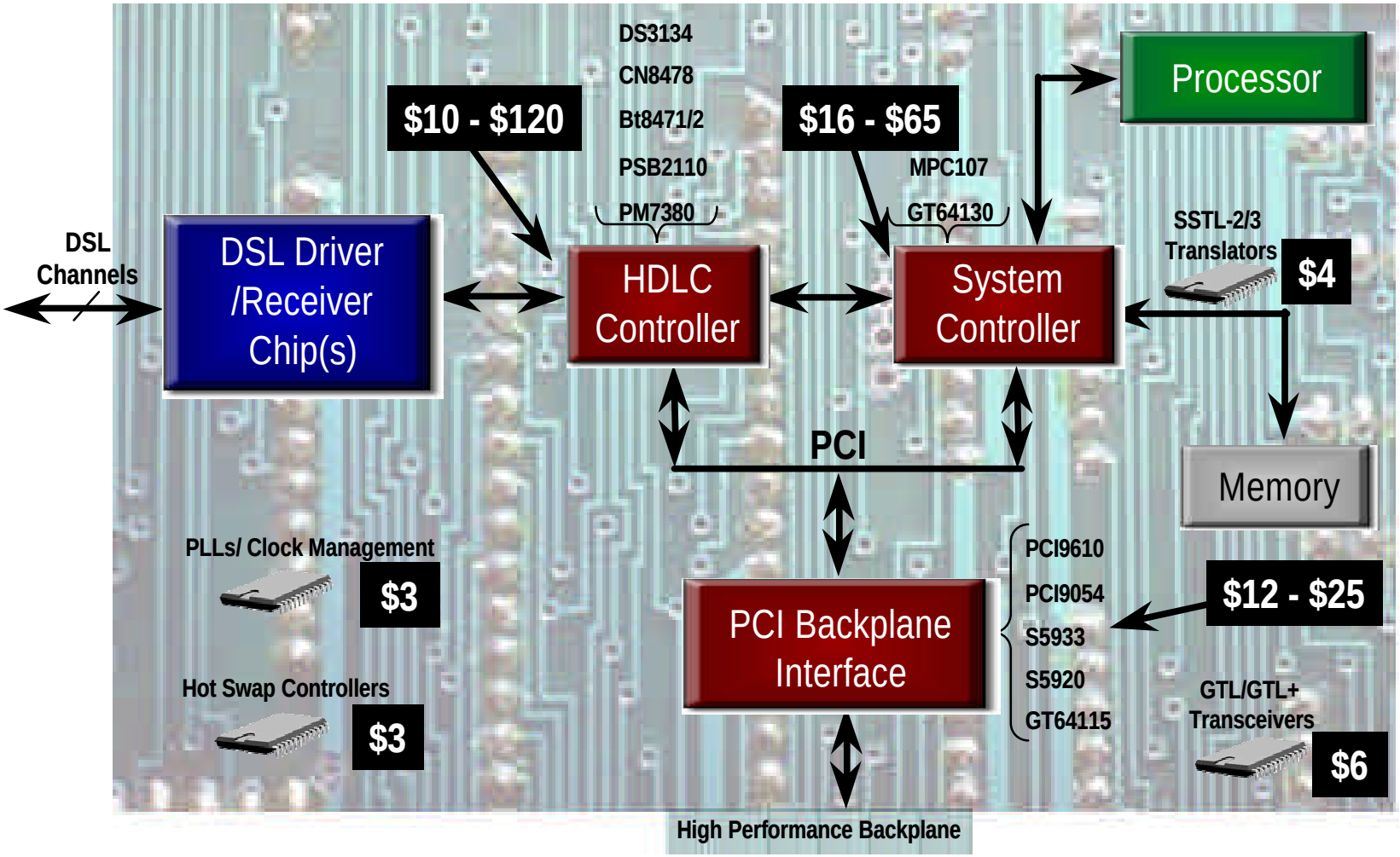


* HNS Proprietary ASIC

Generic DSL Line Card

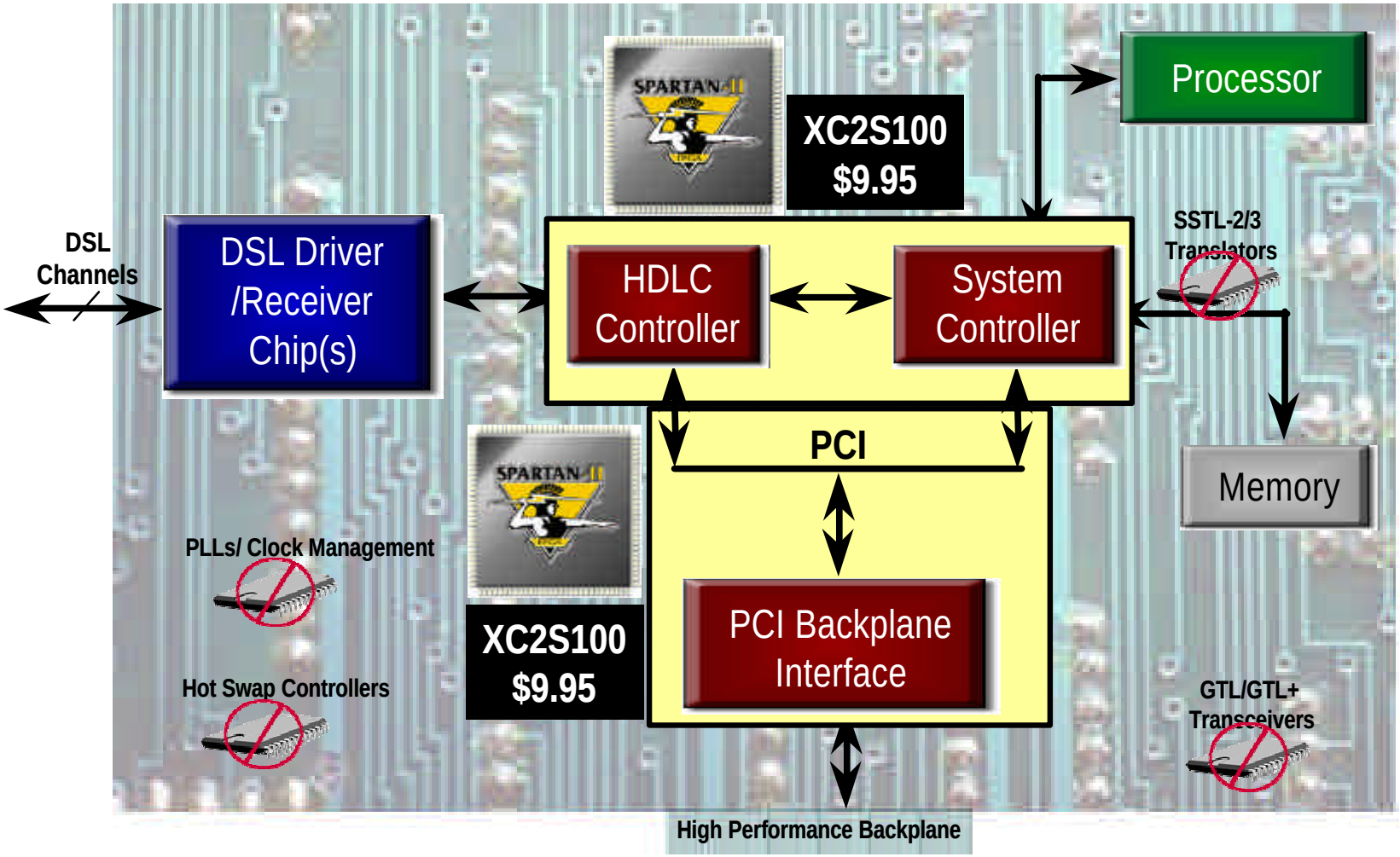


Generic DSL Line Card

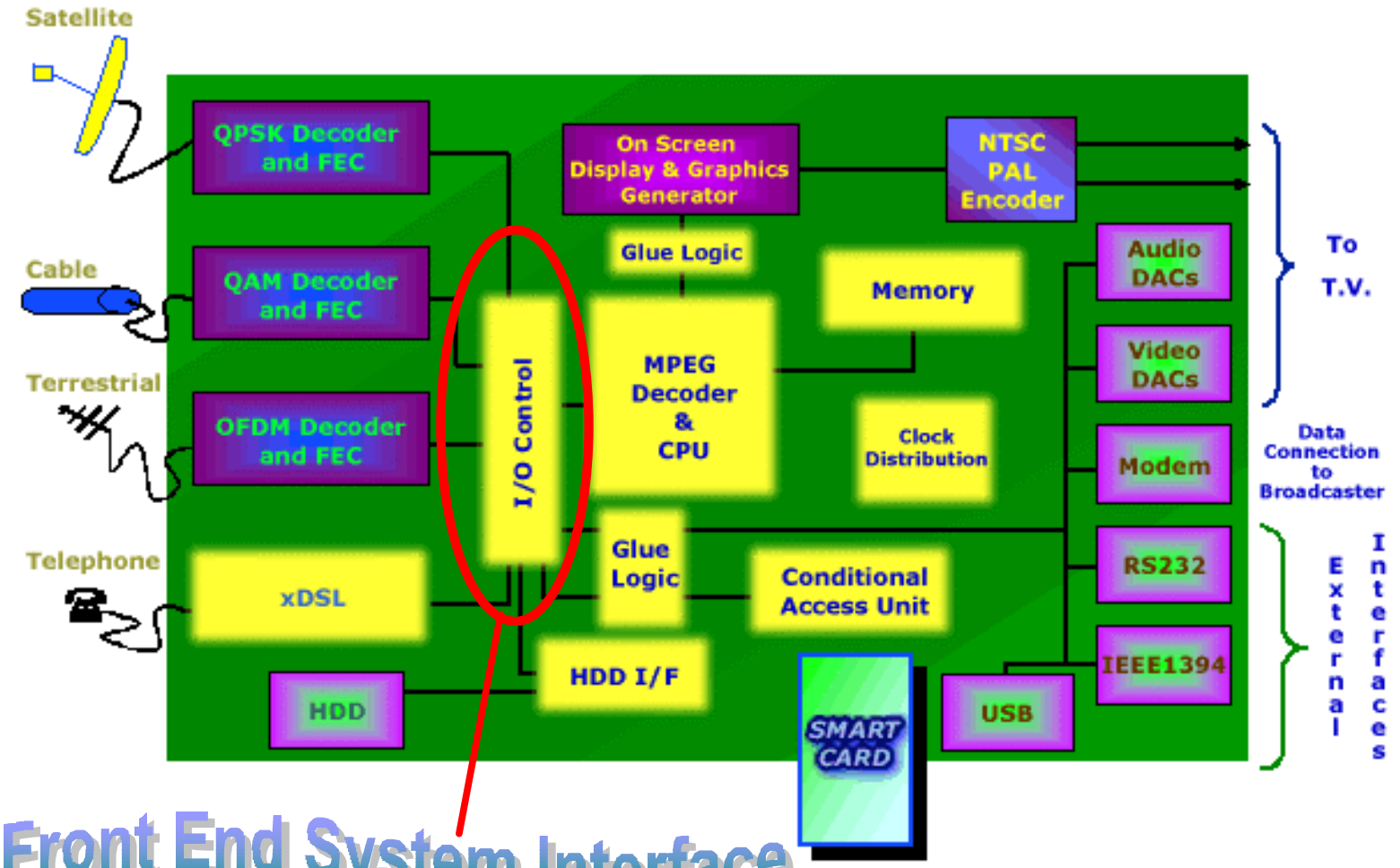


Generic DSL Line Card

Logic and Interface Savings By Using Spartan-II FPGAs

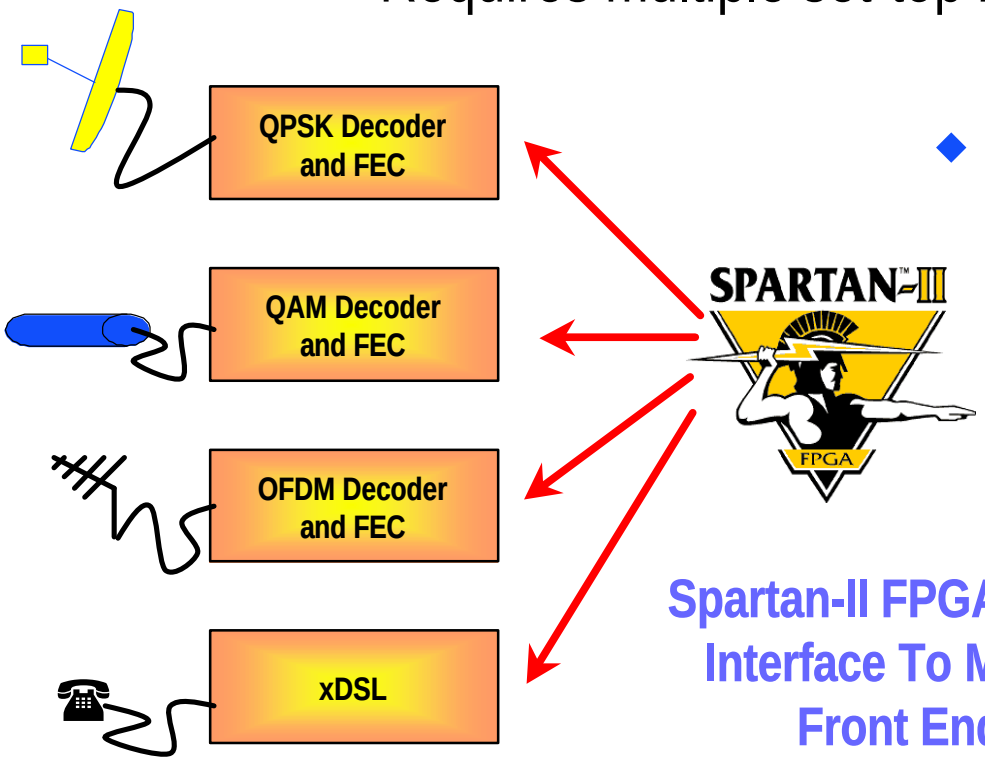


Front End System Interface



Front End Interface

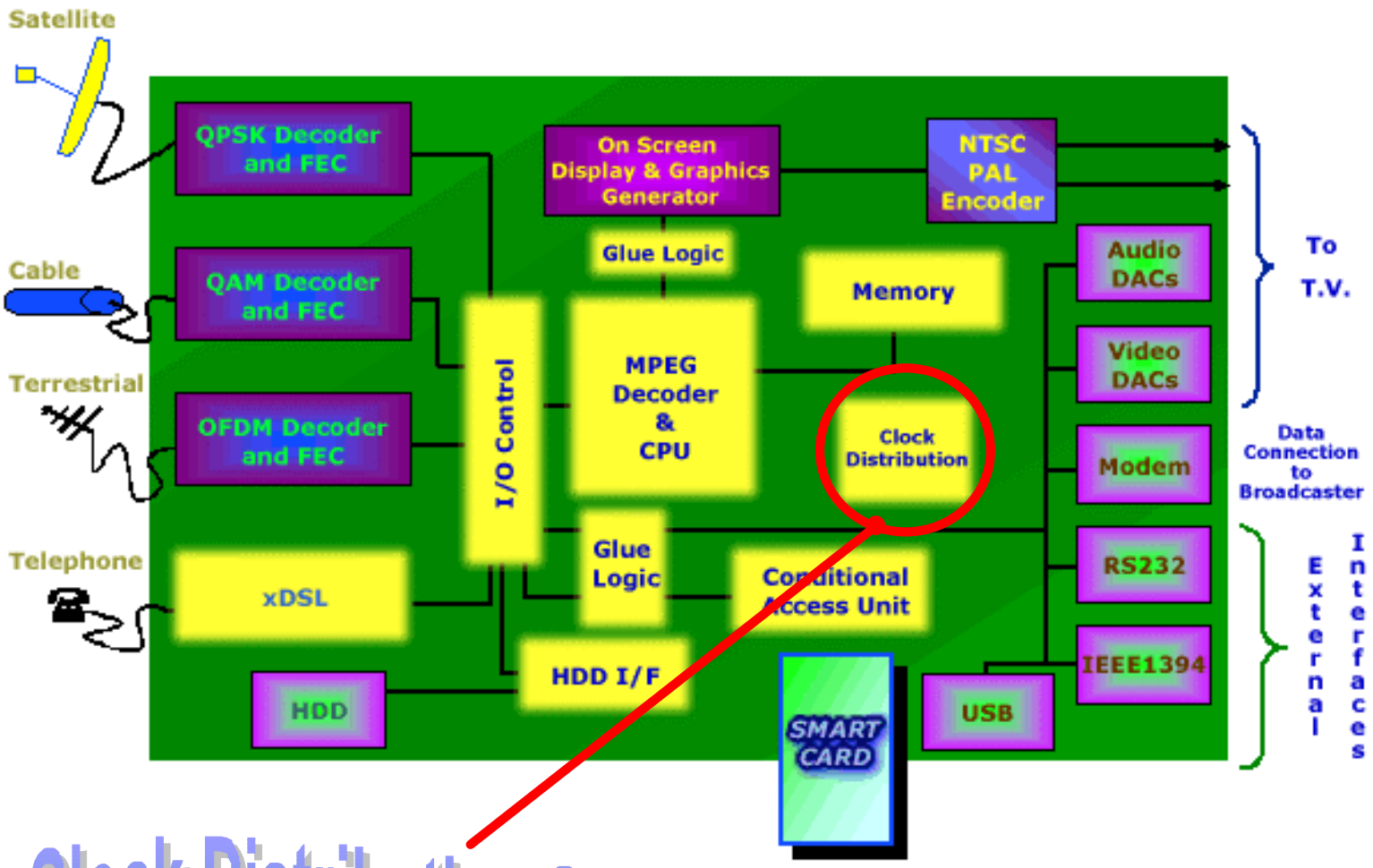
- Not cost effective to support multiple receivers
  - Cable, terrestrial, satellite and xDSL
  - Requires multiple set-top box designs



- Interface required to support multiple ASSPs
  - Choice of ASSP influenced by broadcaster features

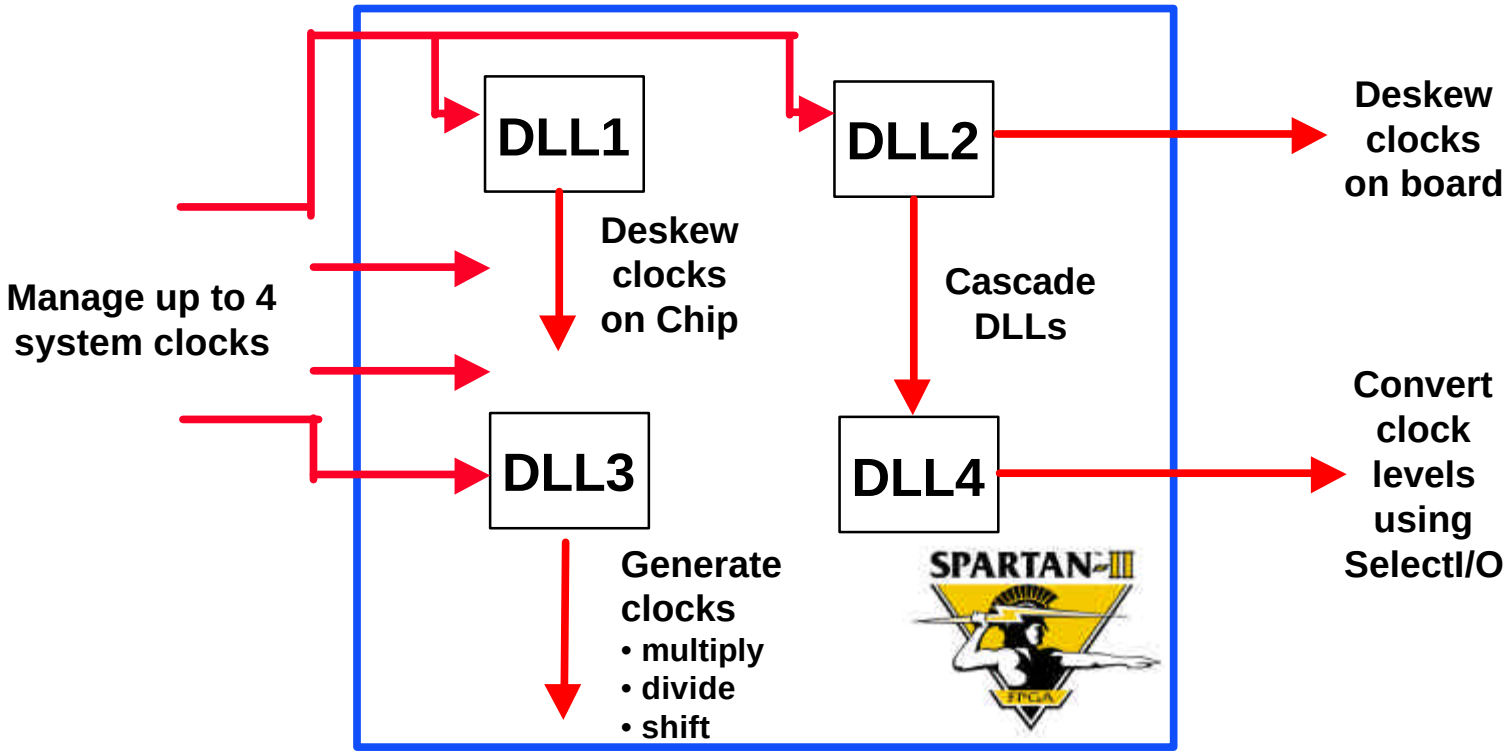
Spartan-II FPGA Allows Interface To Multiple Front Ends

Clock Distribution



Clock Distribution Solutions

Spartan-II Clock Management

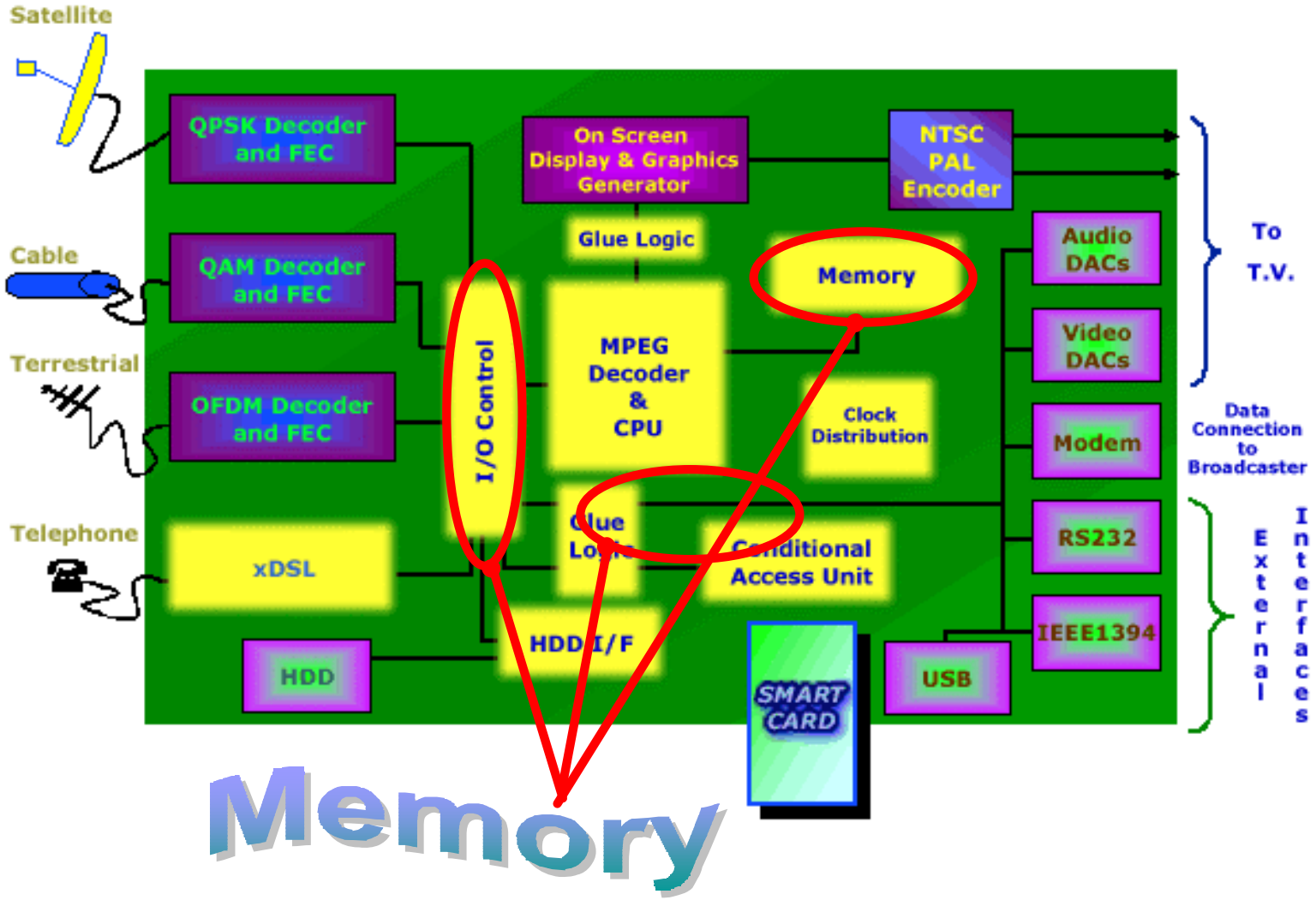


Delay Locked Loops lower memory and board costs

Clock Generation and Distribution

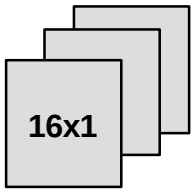
- Spartan-II DLL circuits provide full clock management solution
- Clock generation
  - Synthesizing many clocks from a single reference crystal or clock
- Clock buffering and distribution
  - Providing multiple copies of a single clock
  - SDRAM clocks
- Spread spectrum clocks for EMI reduction
  - DLL circuits allow tolerance for ±2.5% variance

Memory Solutions



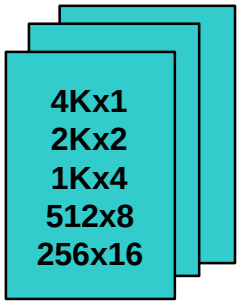
Spartan-II Memory Solutions

Distributed RAM



DSP Coefficients
Small FIFOs

Block RAM



Large FIFOs
Video Line Buffers
Cache Tag Memory

External Memory Interface

SDRAM
SGRAM
PB SRAM
DDR SRAM
ZBT SRAM
QDR SRAM

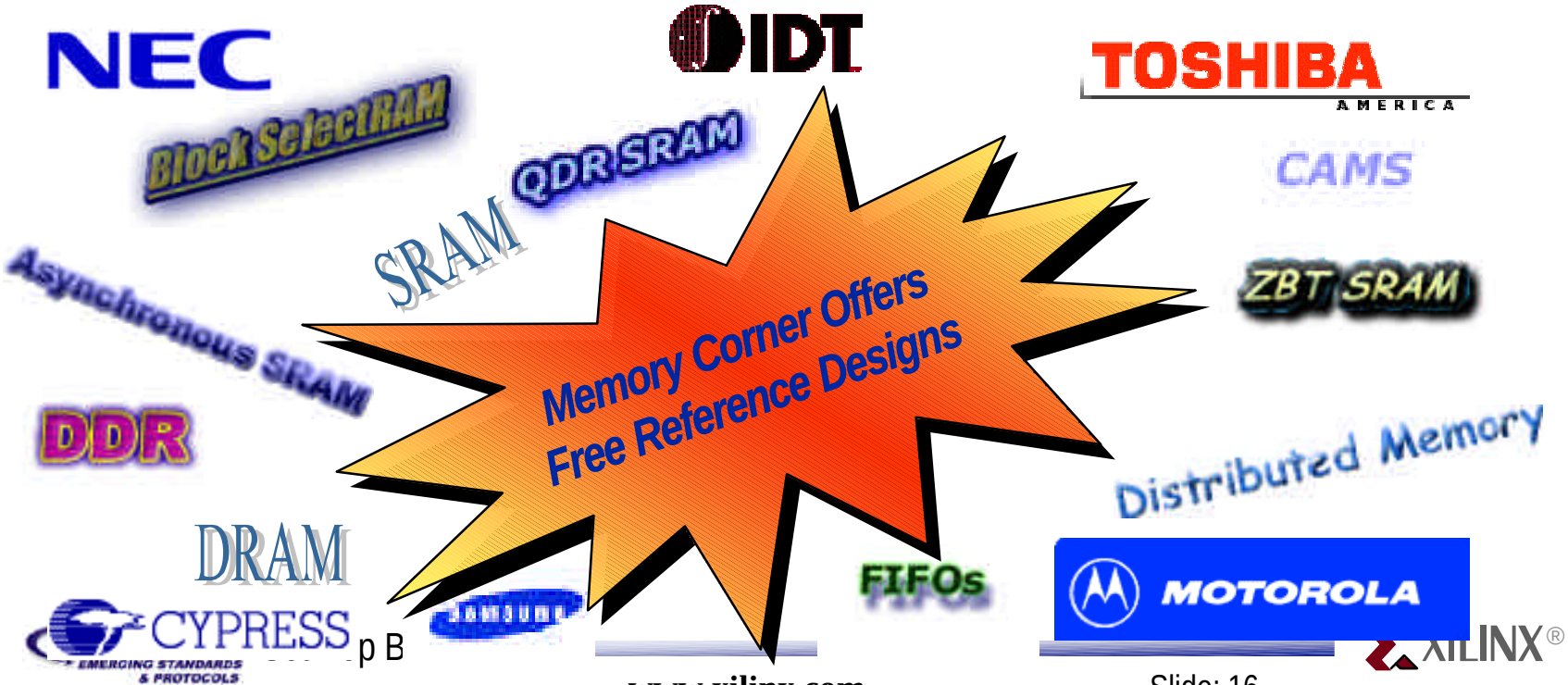
200 MHz Memory Continuum - Transparent Bandwidth

1998 1999 2000

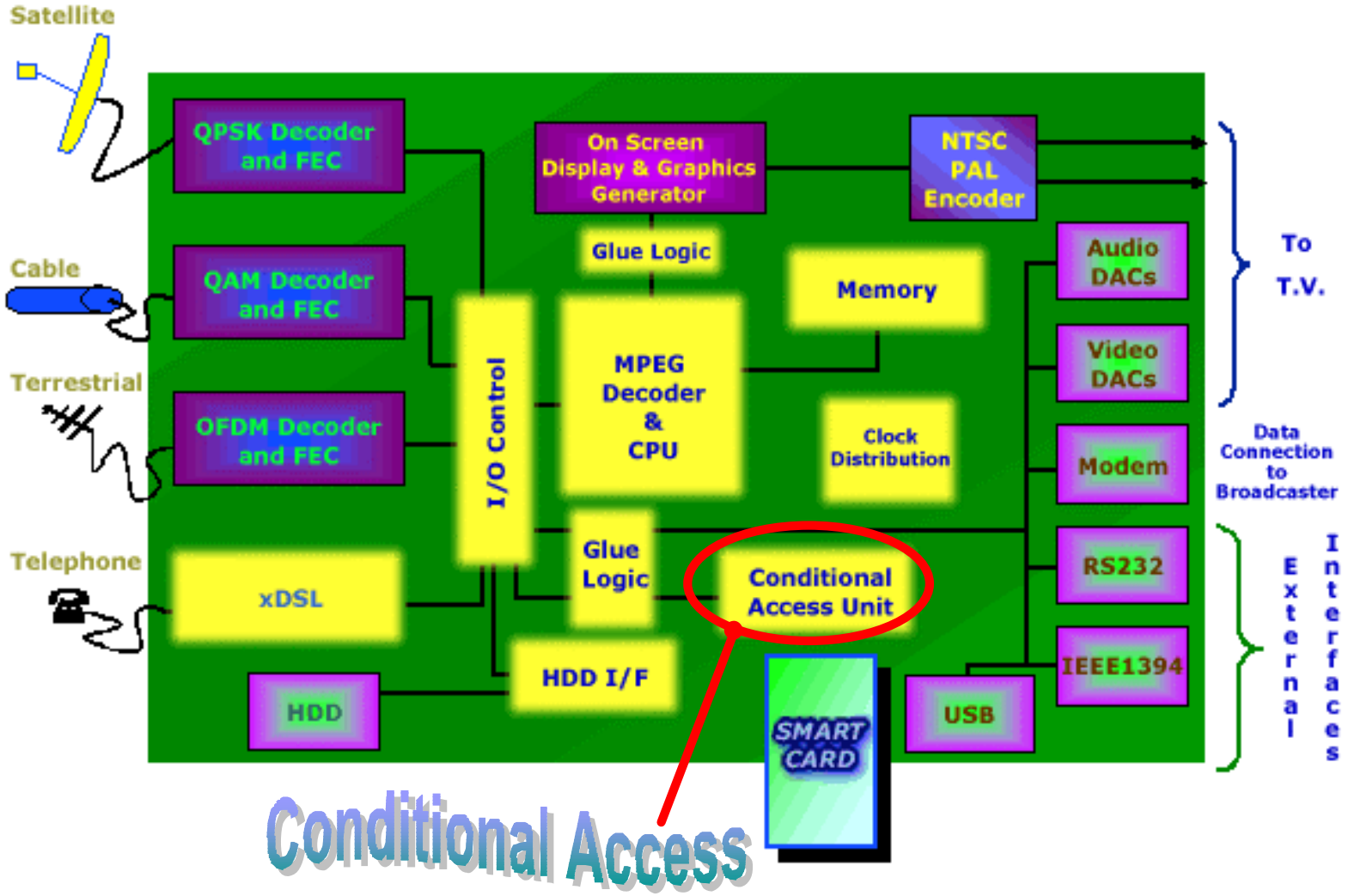
Set-Top Boxes

Memory Corner

- Collaboration between Xilinx and major memory vendors to provide comprehensive web-based memory solutions
  - Free reference designs (VHDL/Verilog)
  - SRAM, DRAM & embedded FPGA memory solutions
  - Data sheets, app notes, tutorials, FAQs, design guidelines



Conditional Access System



Data Encryption

- Motivation for data encryption & cryptography
  - Data privacy
    - Integrity
    - Secrecy
  - Authenticating the source of the information
- Several methods of data encryption exist
  - RSA (Rivest-Shamir-Adleman), Diffie-Hellman, RC4/RC5
  - Secure Hashing Algorithm (SHA), Blowfish
  - Elliptic Curves, ElGamal, LUC (Lucas Sequence)
  - **DES (Data Encryption Standard) & Triple-DES (TDES)**

DES Concept

- The Data Encryption Standard (DES) algorithm
  - Developed by IBM Corporation
  - Most prevalent encryption algorithm
  - Adopted by the US government in 1977, as the federal standard for encryption of commercial and sensitive-yet-unclassified data
  - Is a Block cipher
    - Encryption algorithm that encrypts block of data all at once, and then goes on to the next block
  - Divides 64-bit plaintext into blocks of fixed length (ciphertext)
  - Enciphers using a 56-bit secret internal key

Triple-DES Concept

- Triple-DES concept
  - More powerful & more secure
  - Equivalent to performing DES 3 times on plaintext with 3 different keys
  - TDES use 2 or 3 56-bit keys
  - With one key, TDES performs the same as DES
  - TDES implementation: serial and parallel
    - Parallel improves performance and reduces gate count

Spartan-II “Secure” Applications

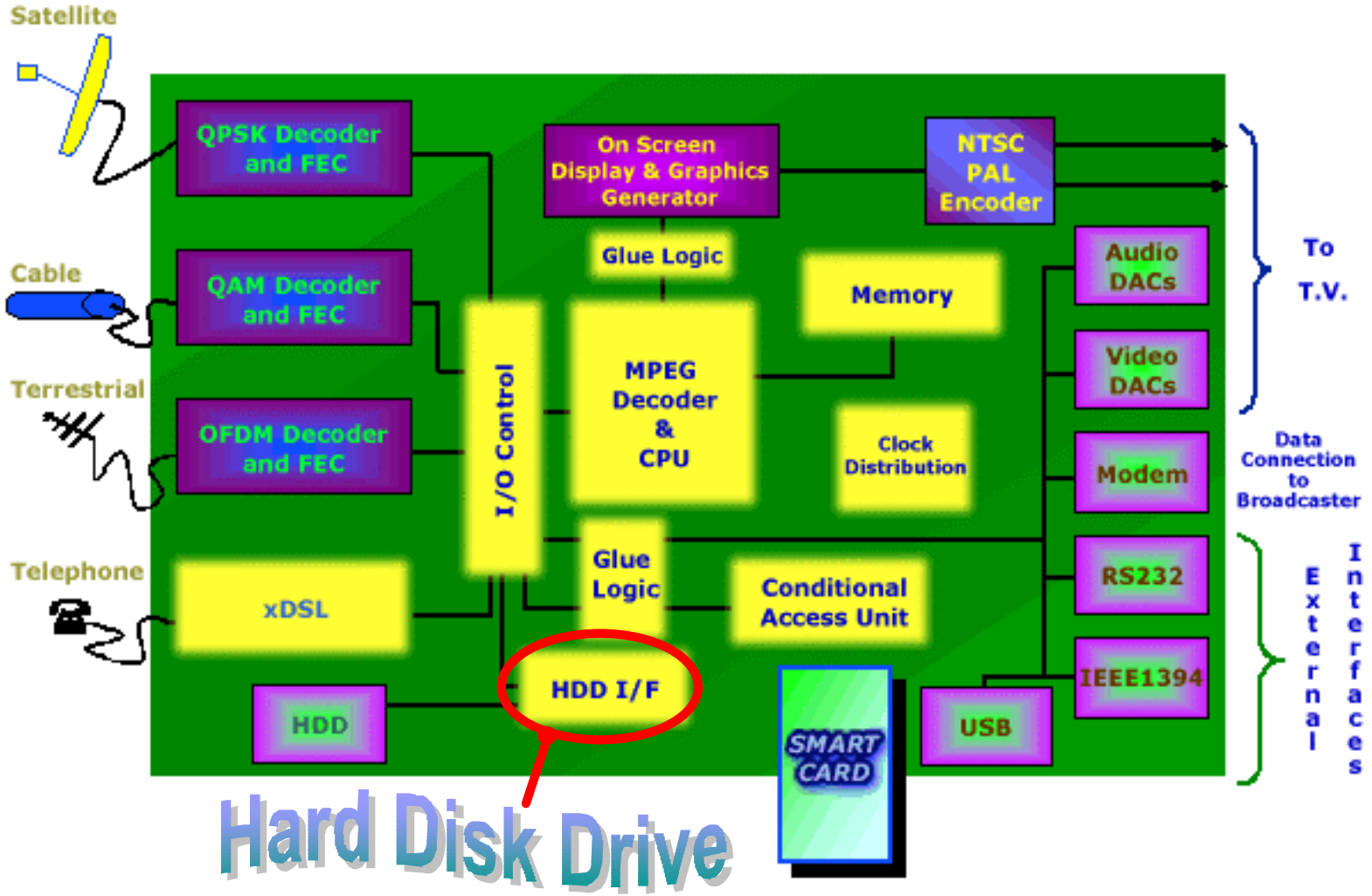
- eCommerce security enabled PCs
- Cable TV
- DVD/Video CD players
- Ultrasound/MRI systems
- Bluetooth wireless systems
- Home networking
- Financial transactions
  - prepaid smart cards
  - personal banking systems
- Graphics/image processing cards
- DBS systems
- HDTV
- Cable modems
- **Set-top boxes**
- Wireless LAN
- Digital VCRs
- Digital camera

Spartan-II DES/TDES Solution

- Spartan-II DES & Triple-DES solutions

Features	Spartan-II Solution	
	DES	Triple - DES
Spartan-II Device	XC2S100-6	XC2S150-6
CLB Slices	235	1611
Clock IOBs	1	1
IOBs	188	244
Performance (MHz)	94	48
Percentage Device (CLBs) Used	19.58%	93.23%

Driving New Technology



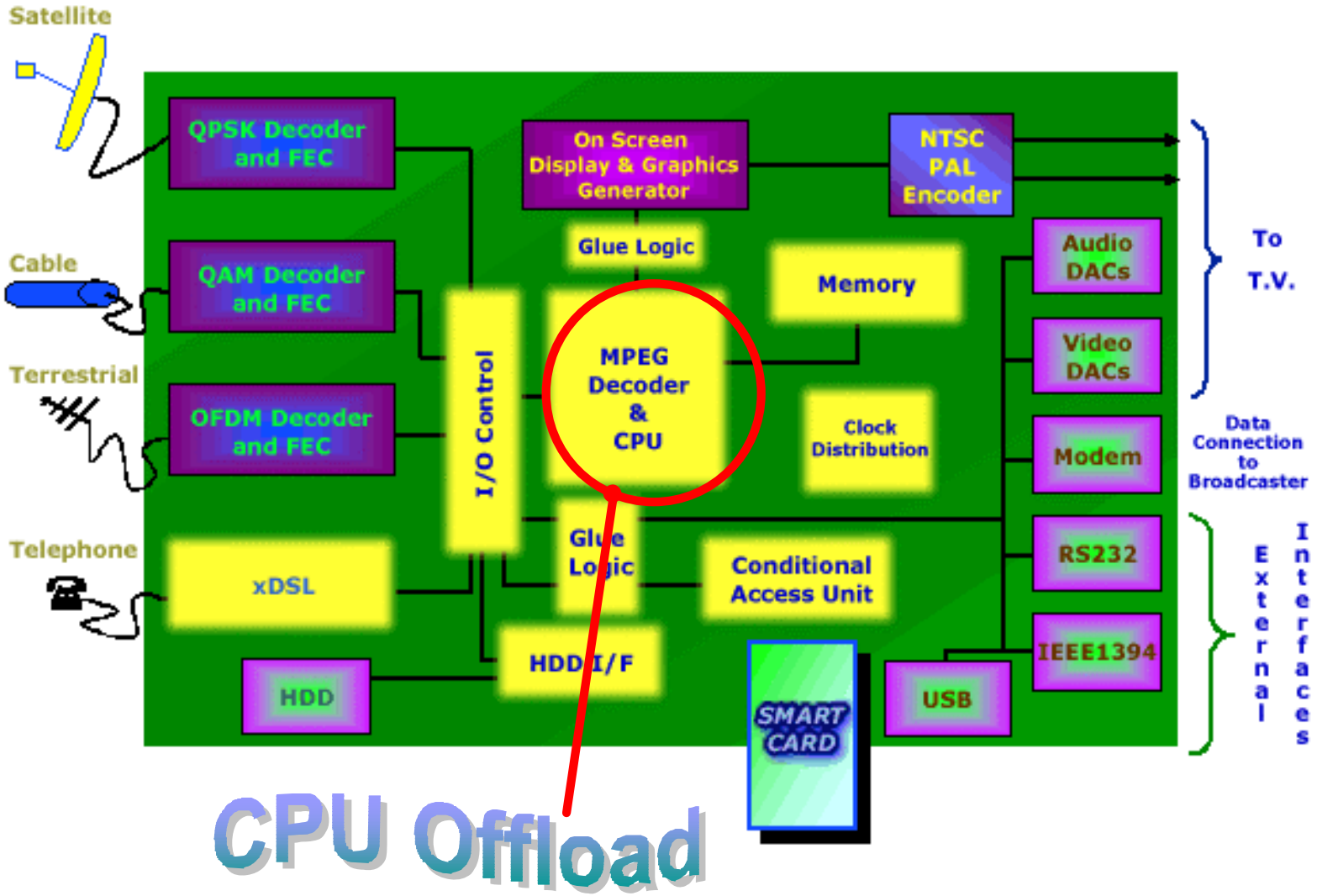
FPGA Drives New STB Features

- Spartan-II FPGA drives a new generation of set-top box
  - Capability to store video on hard disk drives
  - Provides capability to record and view video simultaneously (TiVO, Replay)
- Provides data buffer and disk control logic
  - On-chip memory for FIFOs
- Provides ability to support evolving disk drive technologies
  - Optimized for simultaneous disk read and write
- Enables dual sourcing of multiple types of hard disk drives

Spartan-II FPGA Enables New Set-Top Box Technology

- Spartan-II FPGAs are used to revolutionize the TV experience
  - Pause live TV
  - Instant replay
  - Automatically records favorite programs
  - Advanced TV program search

Top End Set-Top Box



DCT/IDCT Compression

- Compression allows increased throughput through transmission medium
  - Video and audio compression makes multimedia systems very efficient
    - Increases CPU bandwidth
    - Higher video frame rates
    - Better audio quality
    - Enables multimedia interactivity
- DCT and IDCT are widely used in video and audio compression

DCT/IDCT Applications

- List of some end applications
  - DVD/Video CD players
  - Cable TV
  - DBS systems
  - HDTV
  - Graphics/image processing cards
  - Ultrasound/MRI systems
  - Digital VCRs
  - **Set-top boxes**
  - Digital camera

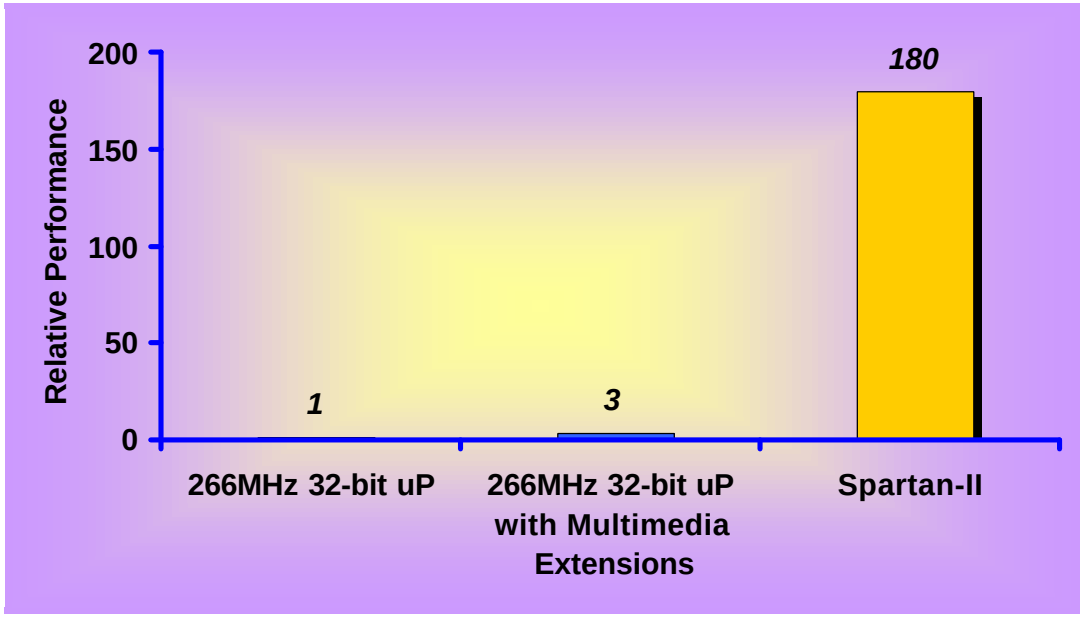
Spartan-II DCT/IDCT Solution Features

Features	Spartan-II
Device	XC2S100-6
CLBs	1026
Clock IOBs	1
IOBs	28
Performance (MHz)	33.3

AllianceCORE Xentec DCT/IDCT Core

Top End Set-Top Box Solution

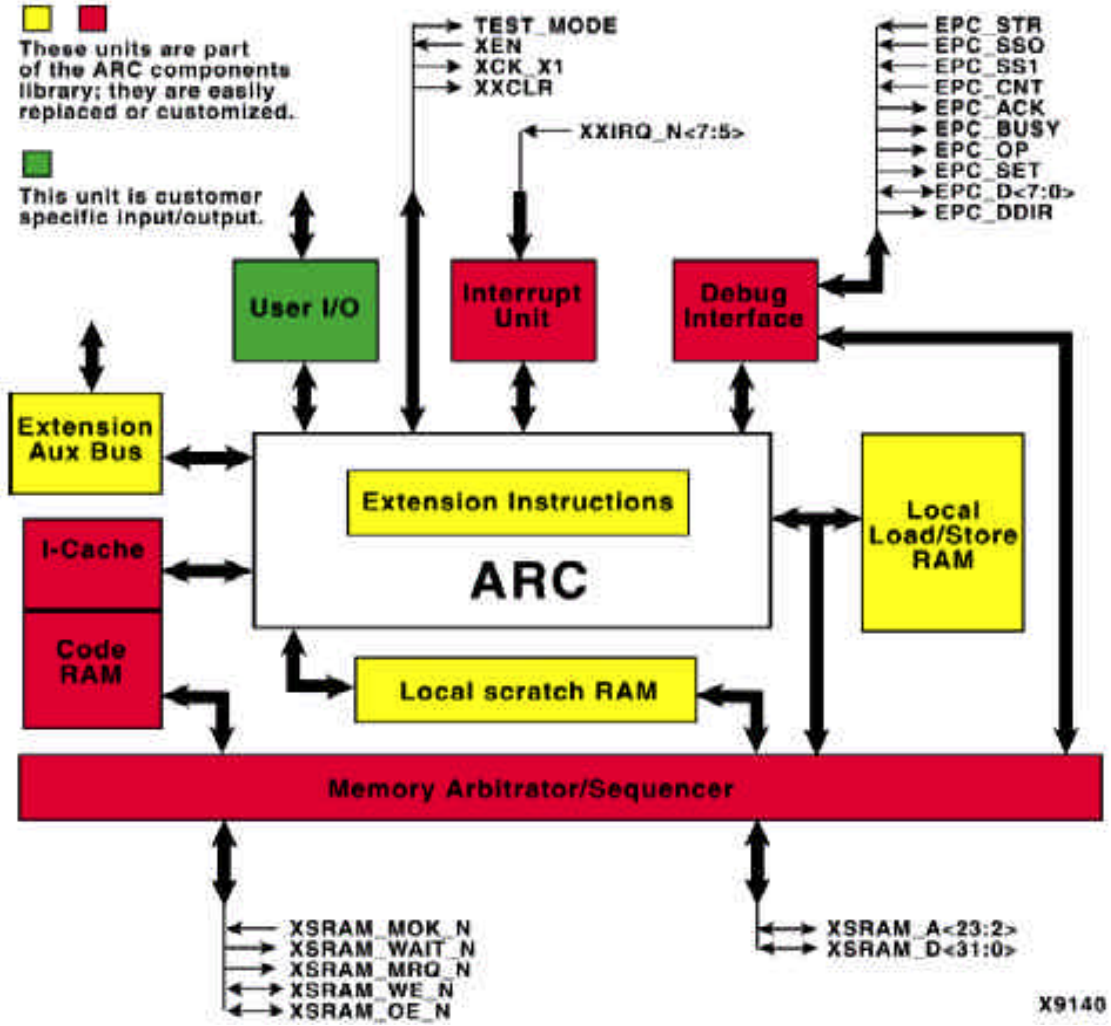
- Spartan-II FPGAs provide low cost, high performance MPEG encoding/decoding
  - DCT/IDCT AllianceCORE IP from Xentec
  - Offload processor for high performance system



ARC Cores - General Description

- ARC is a configurable 32-bit RISC processor technology supplied as two generic pre-configured processor systems
  - First system is a basic (or basecase) configuration that is simply a minimal 32-bit RISC processor
  - Second configuration is a larger, but more powerful, DSP configuration
- Designed to make the addition of custom instructions, condition flags, special registers and custom interfaces very easy

ARC 32-bit RISC Processor System Block Diagram



Implementation Data

Example Implementation	Basecase ARC	Basecase ARC
Device Tested	2S150-6	V400E-8
CLB Slices	1538	1517
Clock IOBs[1]	2	2
IOBs[1]	82	82
Performance (MHz)	37	41
Xilinx Tools	M2.1i SP6	M2.1i SP6
Special Features	9 Block RAMs	9 Block RAMs
ARC Extensions Used	2Kb I-Cache	2Kb I-Cache

Features

- RISC architecture for low gate count & high performance
- Full RISC orthogonal instruction set
- 4-stage pipeline
- 16 single-cycle instructions (basecase)
- 32-bit ALU; all ALU instructions are conditional
- 32-bit data bus
- 32-bit Load/Store address bus
- 32-bit instruction bus
- 24-bit instruction address bus
- 32 general purpose core registers
- 24-bit program counter and stack pointer
- Maskable external interrupts

Features

- Jumps/branches with single instruction delay slot
- Delay slot execution modes
- Zero overhead loops
- Integrated PC parallel port debug interface
  - Allows the debugger to access the processor registers and memory
- C Compiler, debugger, and simulator available from MetaWare Inc.
  - GNU version also available.
- ARCangel™ development system
  - Available for evaluation and rapid product development
- Custom versions of processor available through ARC Certified Design Centers (ACDC)

Applications

- 32-bit processing applications
  - Systems that require a 32-bit processor with custom interfaces or instructions
- DSP applications
- Network processors and routers
- Digital cameras
- **Set-top boxes**
- Bluetooth & Wireless LAN devices
- Cellular base stations