



PRESENTS

NETWORLD INTEROP

an INTEROP event

Programming Network Processors for Time to Performance

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Time to Performance

Achieving target performance and functionality in minimum time requires:

- **System Design Methodology**
 - A systematic development process, supported by a software platform and tools, for the rapid discovery of optimal designs
- **Architecture Flexibility**
 - The ability to (re)map the application logic to the target processor that best ensures performance, headroom and cost
- **Co-processor Support**
 - The ability to accelerate critical functions in dedicated silicon
- **Legacy Software Migration**
 - The ability to leverage existing software in new designs
- **ISV Enablement**
 - Choice of standard software components for a quick start

System Design Methodology

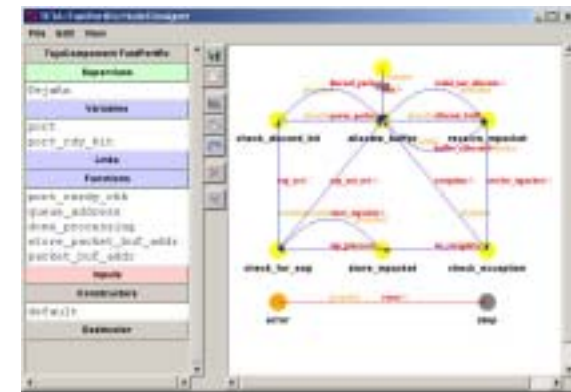
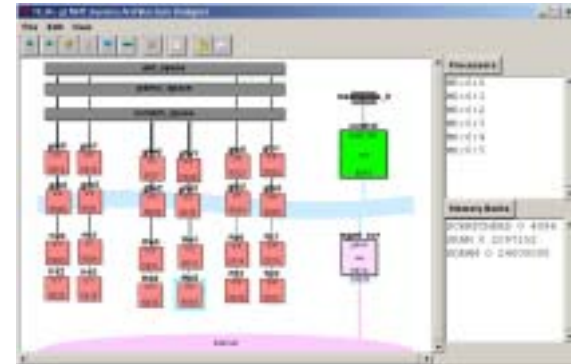
System Architecture Design

Application Logic Design

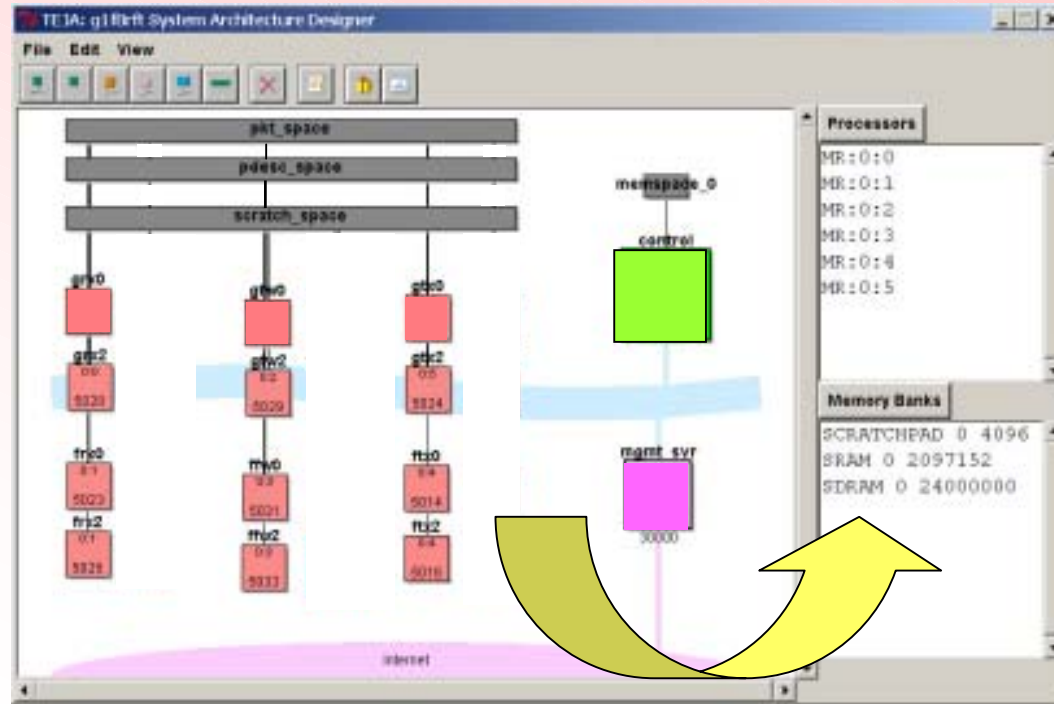
Mapping and Code Generation

Debugging and Tuning

- Iterative, traceable process
- Systematic exploration of design space
- Rapid discovery of optimal design



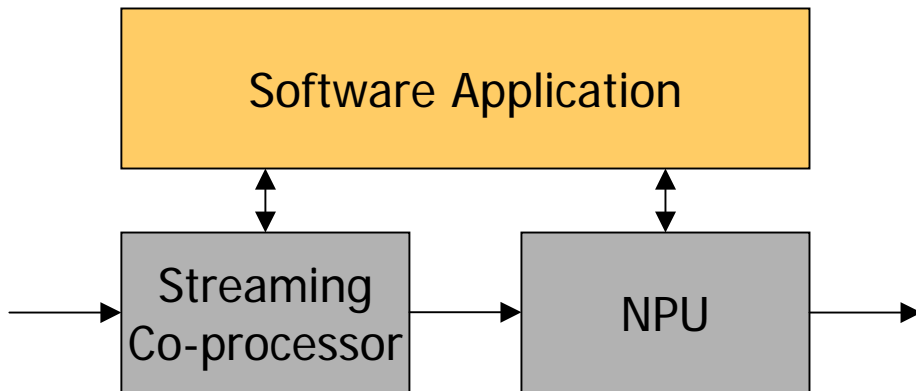
Architecture Flexibility



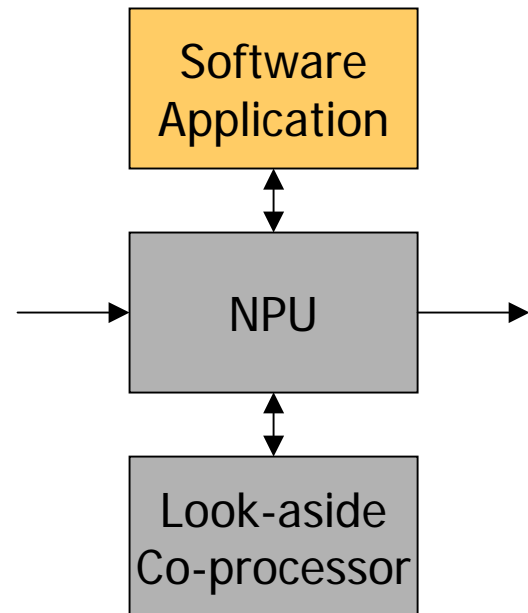
- Flexible assignment of program logic to processors and data structures to memory
- Same software application yields wide choice of price/performance trade-offs
- Increased time in market through hardware upgrades

Co-processor Support

- MAC-like interface to streaming co-processors

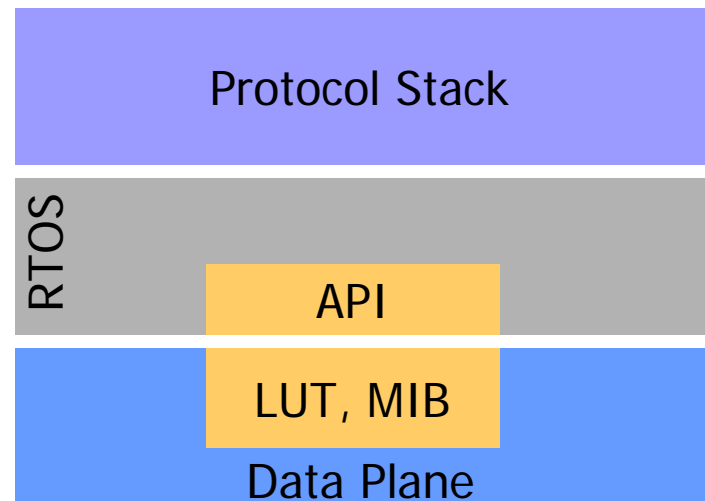
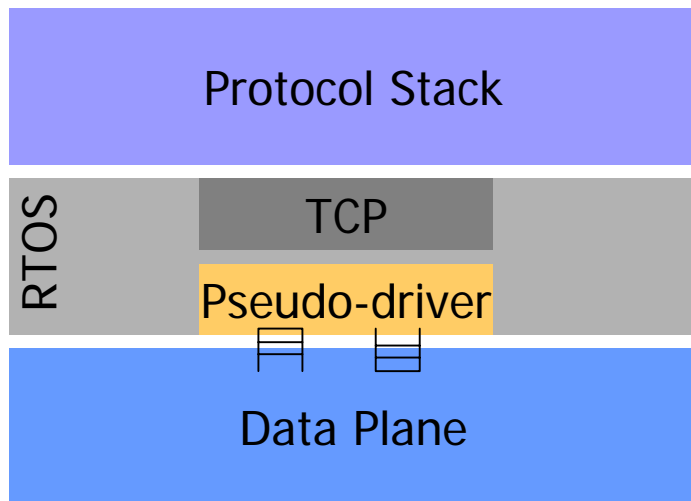


- Function call-like interface to look-aside co-processors



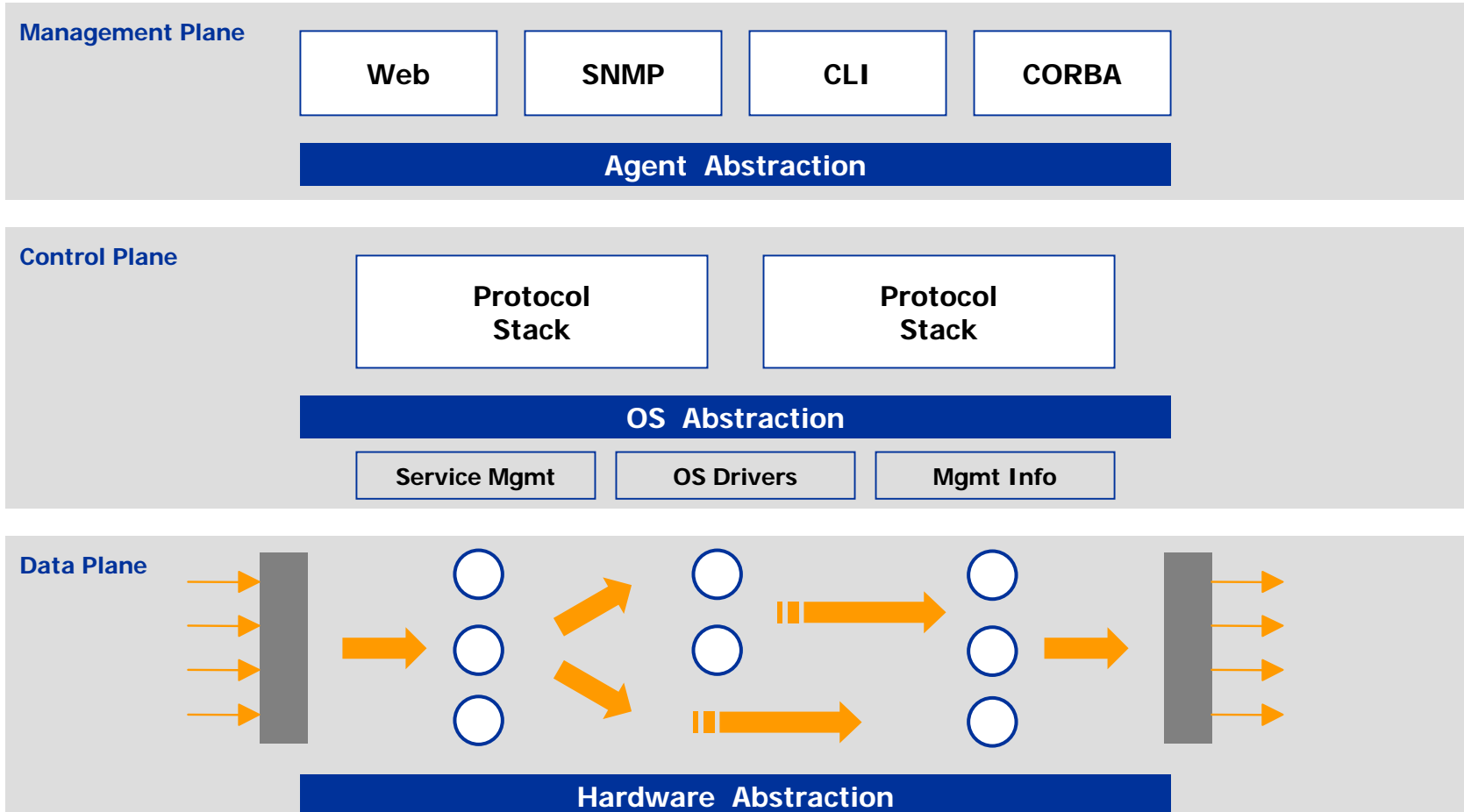
Reusing Control Plane Protocols

- In-band control messages
 - Pseudo-driver interface
- Table, MIB management
 - Control/data plane API



Accelerate network protocols with minimum rework

ISV Enablement



- Modular, integrated platform architecture
- Plug-in components from ISVs