GMII Timing and Electrical Specification

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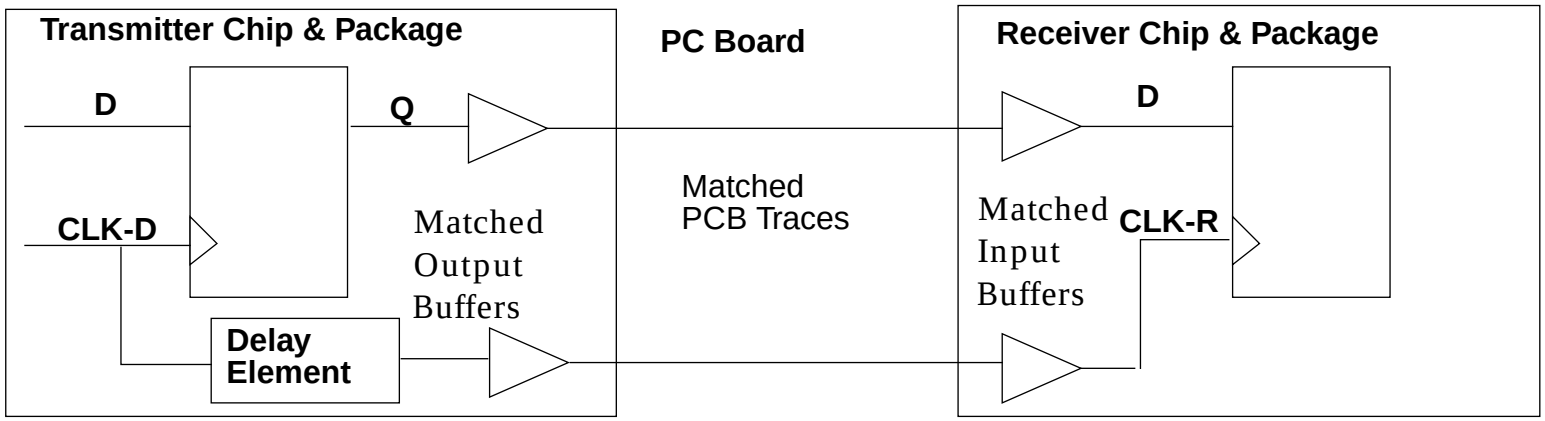
Objectives

- Recommend clocking methodology for GMII
- Afford flexibility in clock specification for MAC and PHY designs
- Define GMII timing specification
- Demonstrate compatibility with MII and external serializer-deserializer chip
- Merge Gigabit 10b Interface and MII electrical specifications for GMII

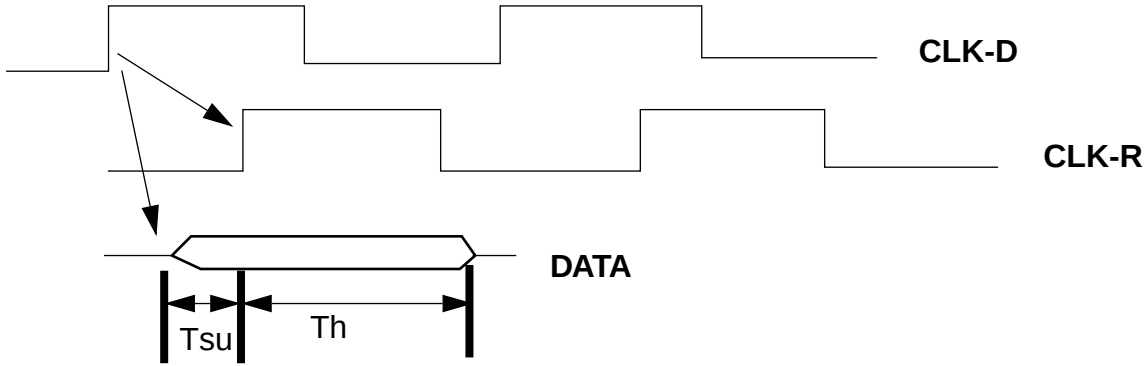
Source Synchronous Clocking Concept:



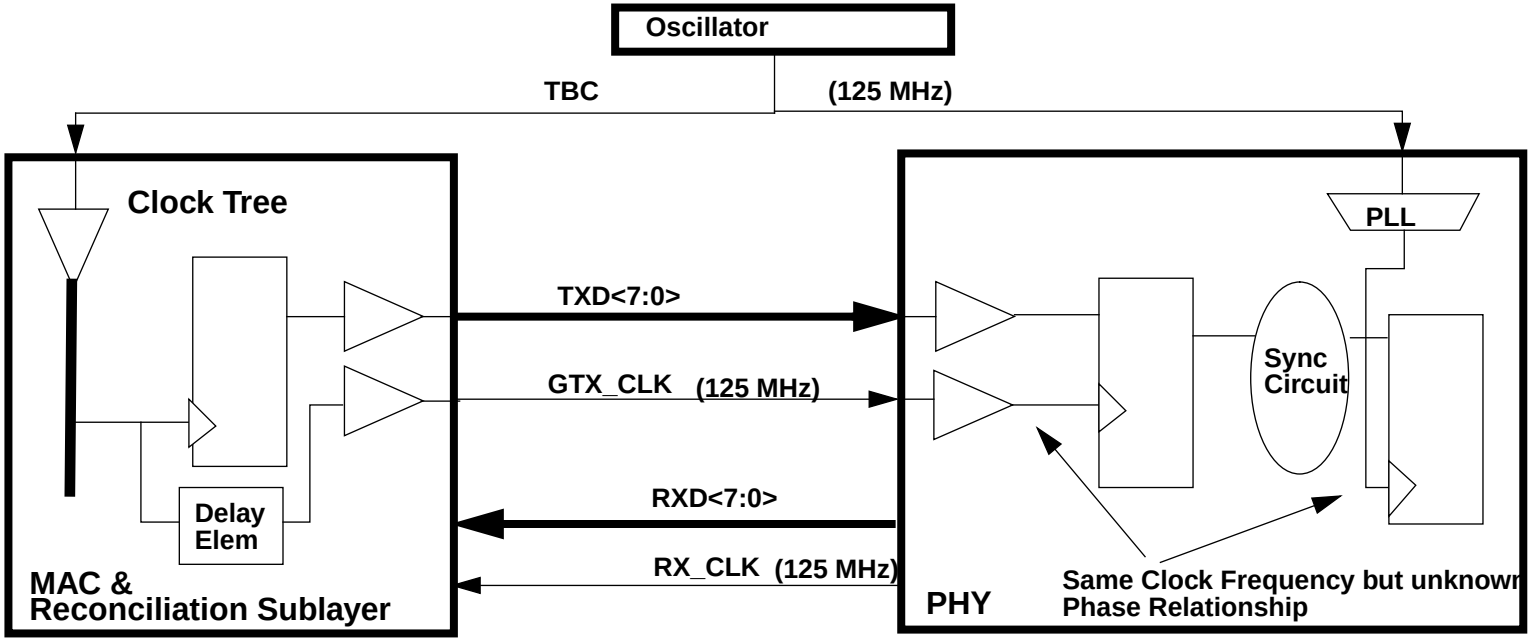
Implementation I Timing:

Cycle Time = $[T_{cq} + dT_{dr}] + [dT_{brd}] + [dT_{rcv} + T_{is}] + [Trsk]$

T_{cq} is the clock to Q delay; dT_{dr}, dT_{brd} and dT_{rcv} are the timing skews for driver, board and receiver; T_{is} is the Input Setup time; Trsk is the clock risetime skew.

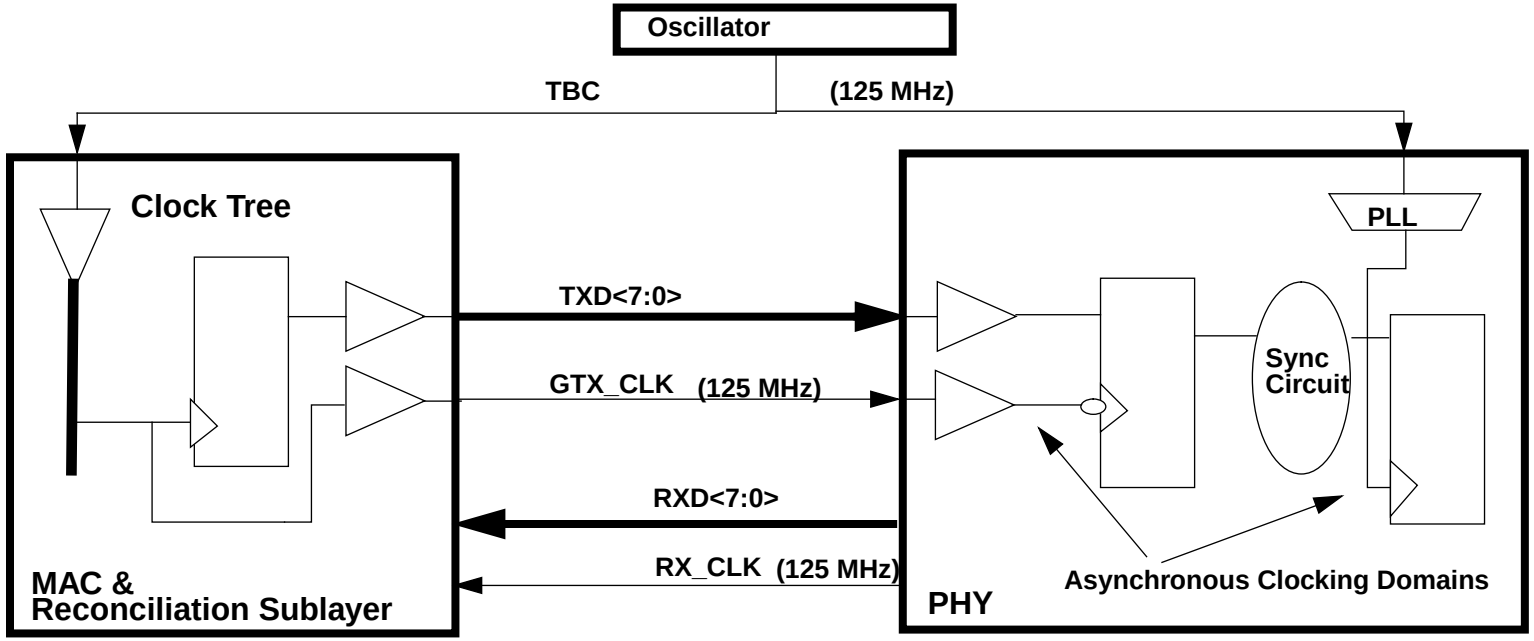


Source Synchronous GMII Clocking:Implemention I

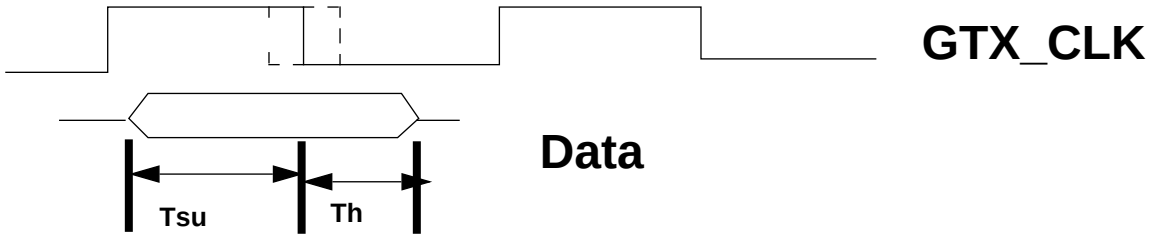


- In PHY, GTX_CLK and PLL clocks have the same frequency but unknown phase relationship.
- Need to account for the synchronization delay in PHY in the Bit Budget calculation.
- Clocking is done at the rising edge only. The setup and hold times are guaranteed based on the delay element.

Source Synchronous GMII Clocking: Implemention II

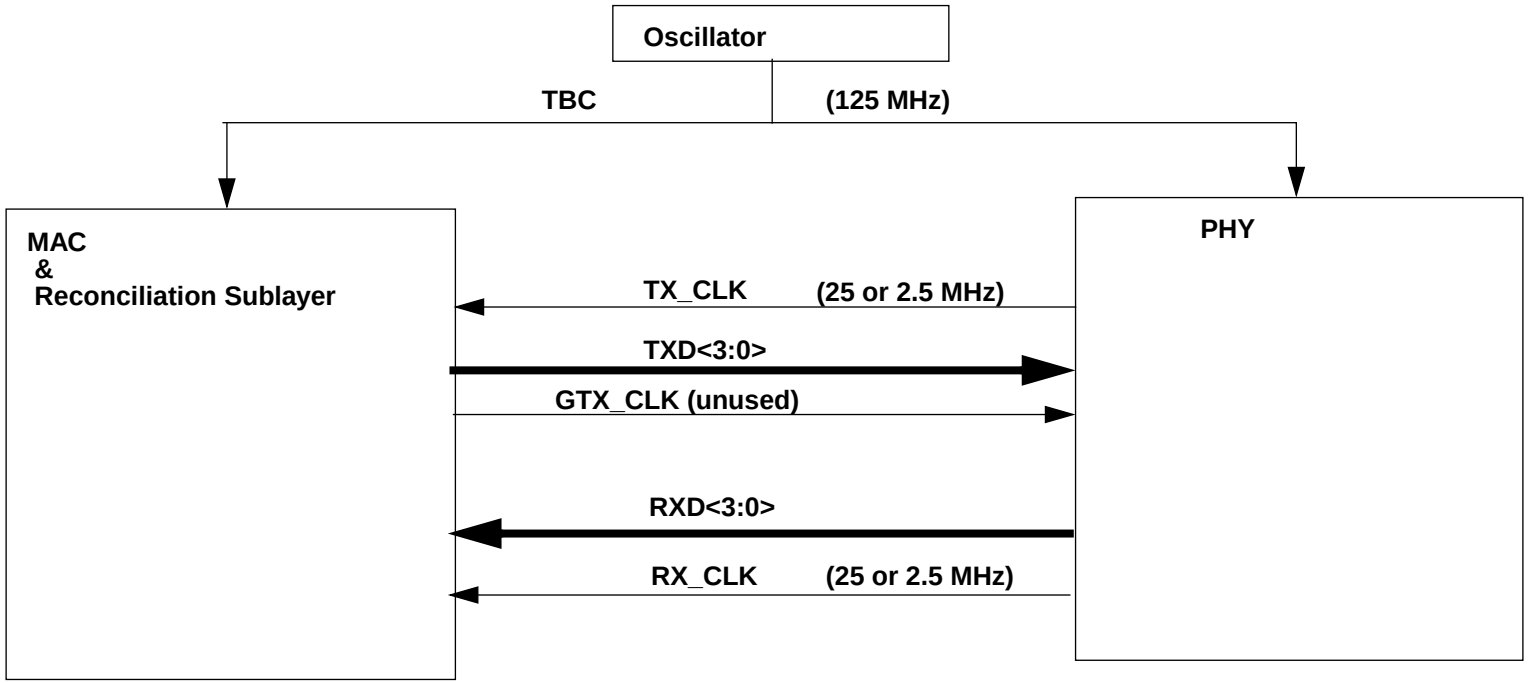


Data Clocking: **Launch at Rising clock edge & latch at the falling clock edge.**

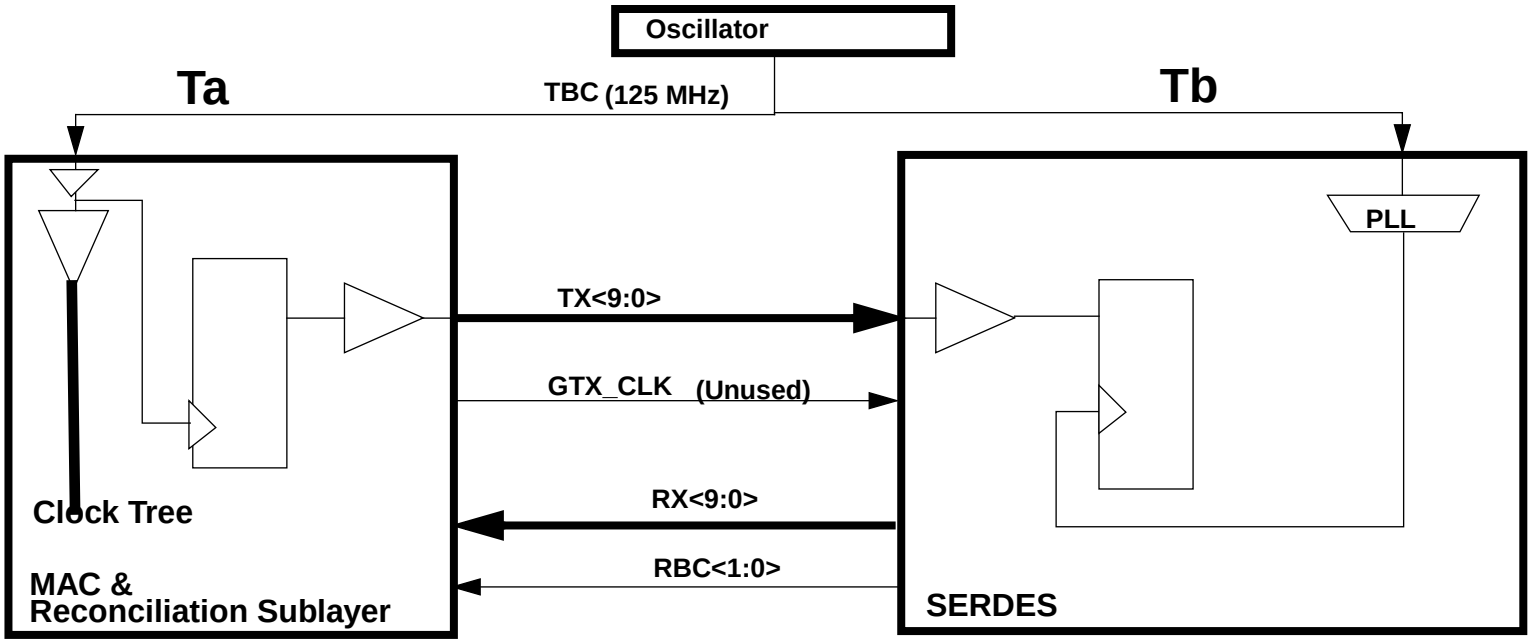


- The duty cycle for GTX_CLK needs to within 40 to 60% and its rise and fall times should be bounded as in Gigabit-10b interface to be from 0.7 to 2.4ns.

GMII Clocking Schematics for MII Compatibility



Clocking for Serializer-Deserializer Compatibility

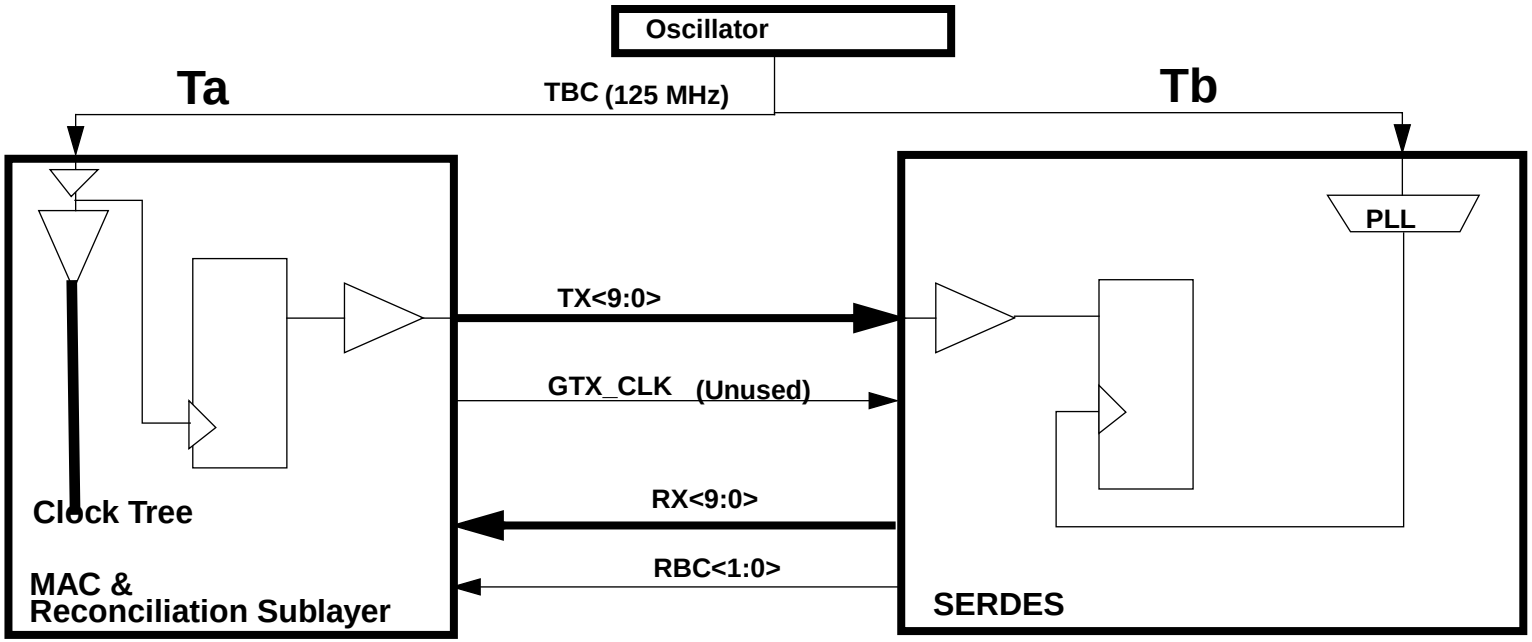


Implementation I Timing: PLL in SERDES, MAC without PLL

Cycle Time = Tcid + Tco + Tbrd + Tis + Tcsk - (Tb-Ta)

Tcid is the Clock Insertion Delay; Tco is the Clock to Data Out including the Output Buffer Delay; Tbrd is the Board Propagation Delay; Tis is the Input Setup time including the Input Buffer delay, Tcsk is the System Clock Skew including the Sending Clock, Receiving Clock as well as the skew on the board; and the (Tb-Ta) term signifies that clock to SERDES is delayed by 0.5ns compared to that of MAC.

Clocking for Serializer-Deserializer Compatibility



Recommended Timing:

Slow Path: 3.5ns + 2ns + 0.5ns + 1.5ns + 1ns - (0.5ns) = 8ns

Slow Path assumes positive clock skew.

Fast Path: 1.8ns + 1ns + 0.2ns - 1ns - (0.5ns) = 1.5ns=Hold Time

Fast Path assumes negative clock skew.

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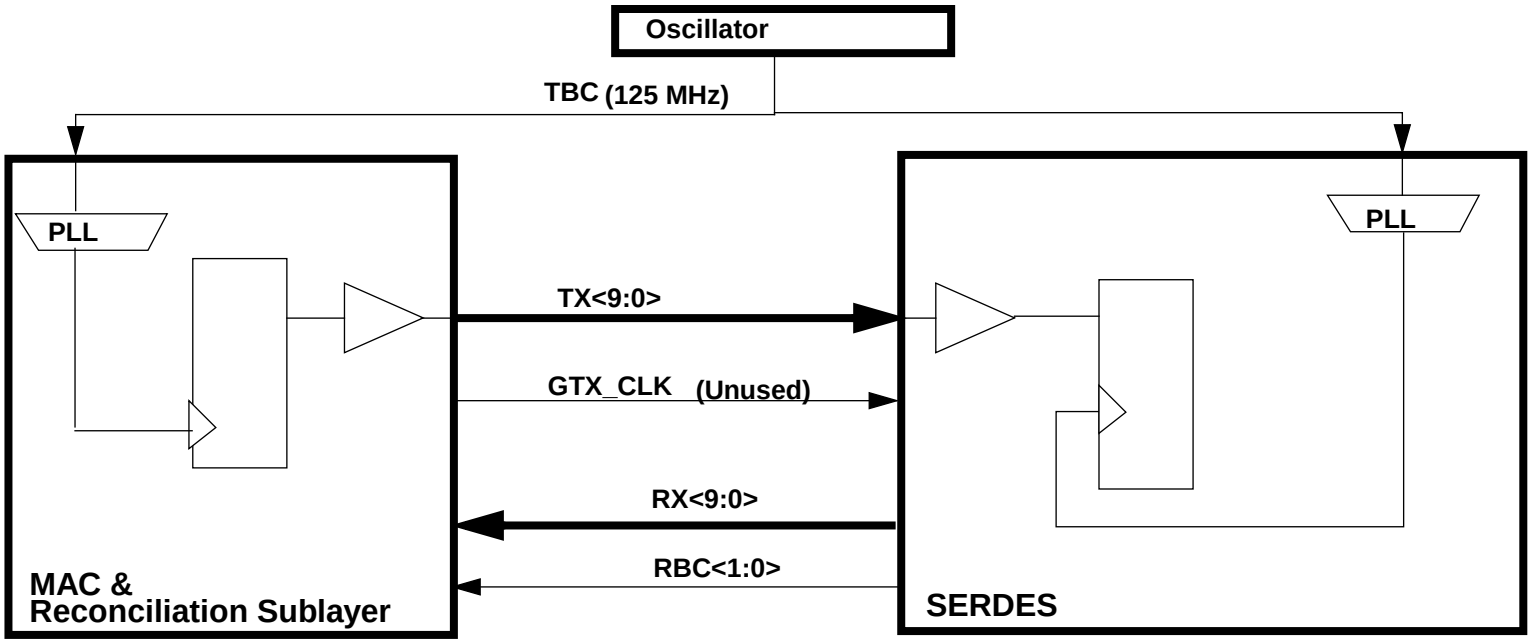
Clocking for Serializer-Deserializer Compatibility



Implementation II Timing: PLL in SERDES and MAC

Cycle Time = Tco + Tbrd + Tis + Tcsk

Slow Path: 4.5ns + 1ns + 1.5ns + 1ns = 8ns

Slow Path assumes positive clock skew.

Fast Path: 2ns + 0.5ns - 1ns = 1.5ns = Hold Time

Fast Path assumes negative clock skew.

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GMII Electrical Interface Specification

- Merge the MII electrical specifications in terms of input and output buffer strengths, TTL Level signalling and compatibility with 5V and 3.3V supply voltages with the G-10b interface specifications to make up the GMII DC and AC characteristics.
- Electrical Signalling among MII, GMII and G-10b Interfaces is interoperable. They all use TTL levels for sampling.

Signal Termination

- Like the MII signals, the GMII signals will be source terminated to preserve the signal integrity per the following equation:

Rd (Buffer Impedance) + Rs (Source Termination Impedance = Z0 (Transmission Line Impedance)

GMII and G-10b Electrical Characteristics

DC Specification

Symbol	Parameter	G-10b Min.	G-10b Max.	GMII Min.	GMII Max
Voh	Output High Voltage	2.4V @ Ioh= -400uA	Vcc @ Ioh= -400uA	2.4V @ Ioh=-4mA	
Vol	Output Low Voltage	GND @ Iol=1mA	0.6V @ Iol=1mA		0.4V @ Iol=4mA
Vih	Input High Voltage	2.0V	5.5V	2.0V	
Vil	Input Low Voltage	GND	0.8V		0.8V
Iih	Input High Currrent		40uA @Vin=2.4V		200uA @Vin=5.25V
Iil	Input Low Current		-600uA @Vin=0.4V	-20uA @ Vin=0V	
Cin	Input Capacitance		4.0pF		8pF
trc	Clock Risetime	0.7ns (0.8-2.0V)	2.4ns (0.8-2.0V)	0.7ns (0.8-2.0V)	2.4ns (0.8-2.0V)
tfc	Clock Falltime	0.7ns (2.0-0.8V)	2.4ns (2.0-0.8V)	0.7ns (2.0-0.8V)	2.4ns (2.0-0.8V)
trd	Data Risetime	0.7ns (0.8-2.0V)		0.7ns (0.8-2.0V)	
tfd	Data Falltime	0.7ns (2.0-0.8V)		0.7ns (2.0-0.8V)	

Caveat on Board Design

- Due to common signal mappings among G-10b interface, GMII and MII, an implementation of External SERDES and a PHY on the same board would result in the presence of stubs and signal integrity problems.