

# Reduced MII interface

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## 1.0 Overview and Architecture

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This document specifies a low pin count (Reduced) Media Independent Interface (RMII) intended for use between Ethernet PHYs and Switch or Repeater ASICs. Under IEEE 802.3u [2] an MII comprised of 16 pins for data and control is defined. In devices incorporating many MACs or PHY interfaces such as Switches or port switched repeaters, the number of pins can add significant cost as the port counts increase. Typical switch products in the industry today offer 12 to 24 ports in a single device. At 6 pins per port and 1 pin per switch ASIC, the proposed RMII would save 119 pins plus the extra power and ground pins to support those additional pins for a 12 port switch ASIC.

The purpose of this interface is to provide a low cost alternative to the IEEE 802.3u [2] MII interface (hereafter referred to as simply "MII"). Architecturally, the Reduced MII interface is an additional reconciliation layer on either side of the MII but can be implemented in the absence of an MII.

The management interface (MDIO/MDC) is assumed to be identical to that defined in IEEE 802.3u [2]. It is assumed that the reader is familiar with IEEE 802.3 [1] and IEEE 802.3u [2].

This interface has the following characteristics:

1. It is capable of supporting 10Mb/s and 100Mb/s data rates
2. A single clock reference is sourced from the MAC to PHY (or from an external source)
3. It provides independent 2 bit wide (di-bit) transmit and receive data paths
4. It uses TTL signal levels, compatible with common digital CMOS ASIC processes

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## 2.0 Application

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This interface has been optimized for use in high port density interconnect devices which require independent treatment of the data paths. The primary motivator is a switch ASIC which requires independent data streams between the MAC and PHY. Port switched repeater ASICs which integrate more than one repeater core and provide a mapping function between PHY interfaces and internal repeater segments may also find this interface useful.

The implementation of the interface is assumed to be a chip-to-chip interface implemented with traces on a printed circuit board. While other implementations are not precluded, no provision is made in this document for an exposed interface (i.e. no connector is specified).

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## 3.0 RMII Design Goals and Trade-offs

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In choosing the signaling for the RMII, the following criteria was applied:

1. Clock frequency of 50 MHz or less to minimize EMI and IC I/O requirements
2. Pin count independent of port density of the PHY
3. Single synchronous clocking
4. Reduction of required control pins

By doubling the clock frequency 4 pins are saved on the data path alone without substantially impacting ASIC I/O capabilities or requiring clock frequencies of 100MHz which can cause significant system level challenges with respect to EMI performance.

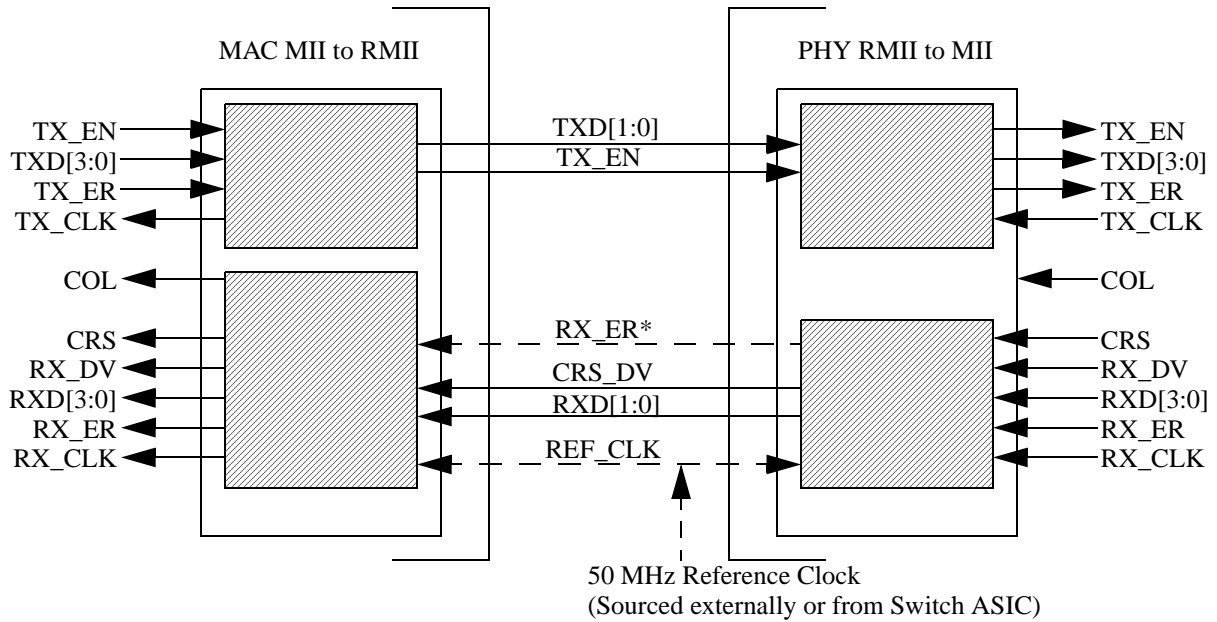
Further, as long as Start of Packet and End of Packet timing information is preserved across the interface, the MAC is able to derive the COL signal from the receive and transmit data delimiters. Of significant impact is preserving Start of Packet information in both 10 and 100 Mb/s operation since there can be a relatively large delta between the assertion of CRS and RX\_DV on the standard IEEE 802.3u MII [2]. However, CRS can be collapsed together with RX\_DV if some additional reconciliation assumptions are made.

RX\_ER is important for meeting Hamming Distance requirements. However, PHYs have the possibility of introducing data replacement to guarantee that the CRC offers adequate protection. Similarly, in switch applications there is no need for TX\_ER since a MAC will never generate errored data. The one case where TX\_ER is used is with repeaters that need to ensure propagation of errors. When used in conjunction with data corruption by the PHY on RX\_ER, this becomes a non-issue.

A single synchronous reference clock for transmit, receive, and control is used. This corresponds to one output from the switch ASIC. Alternatively, the clock reference could be sourced from an external device and may correspond to one input to the switch ASIC. Each PHY provides a clock reference input. However, only one input is required for multiple PHYs on a single IC. PHYs must provide enough buffering to account for worst case variation between local and recovered clock.

Since data is not looped back from transmit to receive, the codes corresponding to RXD[1:0] values and TXD[1:0] while TX\_EN and/or RX\_DV are de-asserted may be used for out of band MAC/PHY signalling.

FIGURE 1. MII to RMII Reconciliation Map



\*Note:RX\_ER is a required output of the PHY. The switch ASIC may choose to use this input.

#### 4.0 Conformance

This document follows IEEE 802 conventions in that the word “shall” indicates a requirement for conformance to this specification. The word “may” indicates a choice or an allowable implementation. All other text is background, explanatory, or recommendation.

## 5.0 RMI Signal Definition

The PHY shall implement and conform to the requirements for REF\_CLK, CRS\_DV, RXD[1:0], TX\_EN, TXD[1:0], and RX\_ER. The MAC/repeater shall implement and conform to the requirements for REF\_CLK, CRS\_DV, RXD[1:0], TX\_EN and TXD[1:0].

TABLE 1.

Reduced MII Signals

Signal Name	Direction (with respect to the PHY)	Direction (with respect to the MAC)	Use
REF_CLK	Input	Input or Output	Synchronous clock reference for receive, transmit and control interface
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data
TX_EN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data
RX_ER	Output	Input (Not required)	Receive Error

### 5.1 REF\_CLK

Reference Clock

REF\_CLK is a continuous clock that provides the timing reference for CRS\_DV, RXD[1:0], TX\_EN, TXD[1:0], and RX\_ER. REF\_CLK is sourced by the MAC or an external source. Switch implementations may choose to provide REF\_CLK as an input or an output depending on whether they provide a REF\_CLK output or rely on an external clock distribution device. Each PHY device shall have an input corresponding to this clock but may use a single clock input for multiple PHYs implemented on a single IC.

The REF\_CLK frequency shall be 50 MHz +/- 100 ppm with a duty cycle between 35% and 65% inclusive.

While the PHY may recover clock from the incoming data stream, the receiver shall account for differences between the local REF\_CLK and the recovered clock through use of sufficient elasticity buffering. The elasticity buffer design shall not affect the Inter-Packet Gap (IPG) for received IPGs of 36 bits or greater. To tolerate the clock variations specified here for Ethernet MTUs, the elasticity buffer shall be a minimum of 10 bits.\*

\*Note:Some vendors desire toleration of MTUs greater than the Ethernet MTU.

### 5.2 CRS\_DV

Carrier Sense/Receive Data Valid

This signal operates in much the same way that the traditional CRS signal on the 7-wire 10 Mb/s Ethernet NRZ interface. While this interface was not standard in IEEE 802.3 [1], it has been used extensively in the industry since the invention of Ethernet.

CRS\_DV shall be asserted by the PHY when the receive medium is nonidle. The specifics of the definition of idle for 10BASE-T and 100BASE-X are contained in IEEE 802.3 [1] and IEEE 802.3u [2]. CRS\_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. That is, in 10BASE-T mode, when squelch is passed or in 100BASE-X mode when 2 non-contiguous zeroes in 10 bits are detected carrier is said to be detected.

Loss of carrier shall result in the deassertion of CRS\_DV synchronous to REF\_CLK. So long as carrier criteria are being met, CRS\_DV shall remain asserted continuously from the first recovered di-bit of the frame through the final recovered di-bit and shall be negated prior to the first REF\_CLK that follows the final di-bit.

The data on RXD[1:0] is considered valid once CRS\_DV is asserted. However, since the assertion of CRS\_DV is asynchronous relative to REF\_CLK, the data on RXD[1:0] shall be “00” until proper receive signal decoding takes place (see definition of RXD[1:0] behavior).

\*Note:CRS\_DV is asserted asynchronously in order to accomodate repeater applications which require the earliest possible indication of carrier.

### **5.3 RXD[1:0]**

Receive Data [1:0]

RXD[1:0] shall transition synchronously to REF\_CLK. For each clock period in which CRS\_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. In some cases (e.g. before data recovery or during error conditions) a pre-determined value for RXD[1:0] is transferred instead of recovered data. RXD[1:0] shall be “00” to indicate idle when CRS\_DV is deasserted. Values of RXD[1:0] other than “00” when CRS\_DV is deasserted are reserved for out-of-band signalling (to be defined). Values other than ‘00’ on RXD[1:0] while CRS\_DV is de-asserted shall be ignored by the MAC/repeater. Upon assertion of CRS\_DV, the PHY shall ensure that RXD[1:0]=00 until proper receive decoding takes place.

#### **5.3.1 RXD[1:0] in 100 Mb/s mode**

For normal reception following assertion of CRS\_DV, RXD[1:0] shall be “00” until the receiver has determined that the receive event has a proper Start of Stream Delimiter.



### 5.3.3 RXD[1:0] and Receive Error Detection

The MII provides the RX\_ER signal to ensure propagation of errors when the 100BASE-X PHY cannot decode the receive signal properly. To eliminate the requirement for this signal and still meet the requirements for undetected error rate, RXD[1:0] shall replace the decoded data in the receive stream with “01” until the end of carrier activity. By replacing the data in the remainder of the frame with a particular pattern, the CRC check is guaranteed to reject the packet as errored (an exact mathematical analysis of impact to undetected error rate will be added in a later revision).

Switches perform CRC checking and will not propagate errored packets. Repeaters do not perform CRC checking and will propagate the errored frame as presented by the 100BASE-X PHY. However, repeaters will propagate the errored packet until it reaches an end station where CRC checking is performed and the packet is discarded. It should also be noted that the need for TX\_ER is also obviated since its purpose was to enable repeaters to ensure error propagation without requiring repeaters to alter the data flowing through them.

In order to ensure the CRC error count is not affected, the PHY shall provide a 16 bit receive error counter that increments upon detection of RX\_ER as defined in IEEE 802.3u [2] at most once per carrier event. It is recommended that the receive error counter be located at 15h within the standard MII register space. If address 15h is not used, the receive error counter register shall be contained between 10h and 1Fh such that IEEE 802.3u [2] MII register space is not affected.

### 5.4 TX\_EN

Transmit Enable

TX\_EN indicates that the MAC is presenting di-bits on TXD[1:0] on the RMII for transmission. TX\_EN shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented to the RMII. TX\_EN shall be negated prior to the first REF\_CLK following the final di-bit of a frame. TX\_EN shall transition synchronously with respect to REF\_CLK.

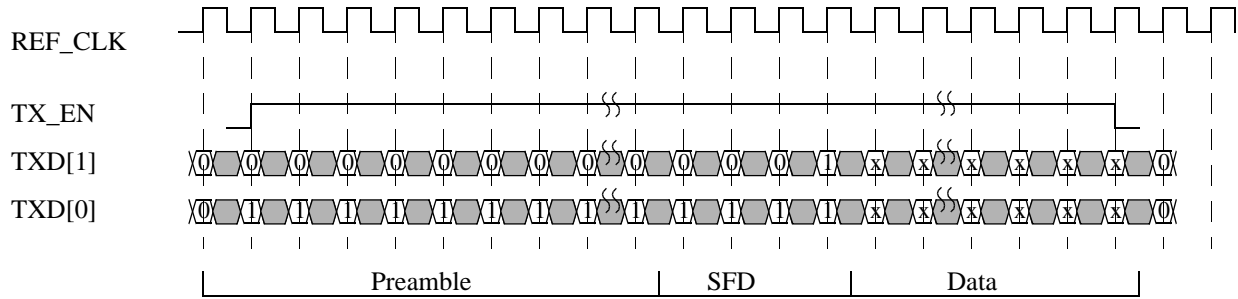
### 5.5 TXD[1:0]

Transmit Data

TXD[1:0] shall transition synchronously with respect to REF\_CLK. When TX\_EN is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD[1:0] shall be “00” to indicate idle when TX\_EN is deasserted. Values of TXD[1:0] other than “00” when TX\_EN is deasserted are reserved for out-of-band signalling (to be defined). Values other than “00” on TXD[1:0] while TX\_EN is deasserted shall be ignored by the PHY.

**5.5.1 TXD[1:0] in 100 Mb/s mode**

TXD[1:0] shall provide valid data for each REF\_CLK period while TX\_EN is asserted.



**FIGURE 4.** 100 Mb/s Transmission

**5.5.2 TXD[1:0] in 10 Mb/s mode**

As the REF\_CLK frequency is 10 times the data rate in 10Mb/s mode the value on TXD[1:0] shall be valid such that TXD[1:0] may be sampled every 10th cycle, regardless of the starting cycle within the group and yield the correct frame data.

**5.6 Collision Detection**

Since the definition of CRS\_DV and TX\_EN both contain an accurate indication of the start of frame, the MAC can reliably regenerate the COL signal of the MII by ANDing TX\_EN and CRS\_DV.

During the IPG time following the successful transmission of a frame, the COL signal is asserted by some transceivers as a self-test. The Signal Quality Error (SQE) function will not be supported by the reduced MII due to the lack of the COL signal. Historically, SQE was present to indicate that a transceiver located physically remote from the MAC was functioning. Since the reduced MII only supports chip-to-chip connections on a PCB, SQE functionality is not required.

**5.7 RX\_ER**

The PHY shall provide RX\_ER as an output according to the rules specified in IEEE 802.3u [2] (see Clause 24, Figure 24-11 - Receive State Diagram). RX\_ER shall be asserted for one or more REF\_CLK periods to indicate that an error (e.g. a coding error or any error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY. RX\_ER shall transition synchronously with respect to REF\_CLK. While CRS\_DV is de-asserted, RX\_ER shall have no effect on the MAC.



\*Note: A switch ASIC is not required to use an input corresponding to the RX\_ER signal provided by the PHY. The reduced MII interface provides data replacement that ensures receive errors are caught by CRC checking in the MAC and are not propagated. The RX\_ER signal is provided for those applications (such as repeaters) that may require its functionality.

### 5.8 Loopback

During normal operation the reduced MII shall not loopback TXD[1:0] to RXD[1:0] or TX\_EN to CRS\_DV. Loopback for diagnostics is unspecified in this document.

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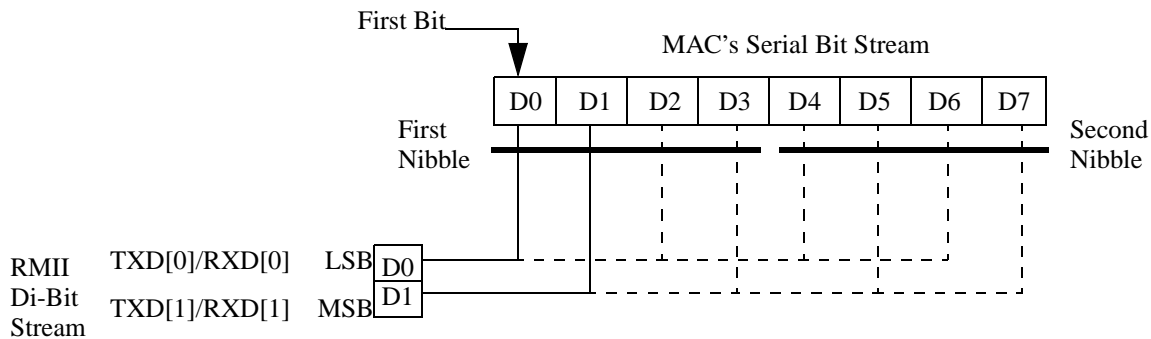
## 6.0 Frame Structure

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Data frames transmitted through the RMI shall have the following frame format:

<inter-frame><preamble><sfd><data><efd>

For the RMI, transmission and reception of each octet shall be done a di-bit at a time with the order of di-bit transmission and reception as shown below.



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## 7.0 Electrical Characteristics

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The electrical characteristics are very similar to those provided for in IEEE 802.3u [2] Clause 22. In many cases the exact text from that clause has been used. This has been done to achieve maximum electrical interoperability by leveraging a proven electrical interfacing standard. The AC and DC requirements listed below shall be met.

### 7.1 Signal Levels

The RMI uses TTL signal levels, which are compatible with devices operating at a nominal supply voltage of either 5.0 or 3.3V. In order to allow interfacing of 3.3V RMI devices and 5.0V RMI devices, all inputs shall be able to tolerate input potentials of 5.5V.

### 7.2 Signal Paths

All connections are intended to be point-to-point connections on PCBs. Typically these connections can be treated as electrically short paths and transmission line reflections can be safely ignored. Neither a connector or a characteristic impedance for electrically long PCB traces is within the scope of this specification.

The output drive is recommended to be kept as low as possible to minimize board level noise and EMI.

### 7.3 DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	Vih		2.0			V
Input Low Voltage	Vil				0.8	V
Input High Current	Iih	Vi=5.5V			200	uA
	Iih	Vi=3.6V			200	uA
Input Low Current	Iil	Vi=0.0	-20			uA

### 7.4 AC Characteristics

Parameter	Min	Typ	Max	Units
REF_CLK Fre- quency		50		MHz
REF_CLK Duty Cycle	35		65	%
TXD[1:0], TX_EN Data Setup to REF_CLK rising edge	2			ns
TXD[1:0], TX_EN Data hold from REF_CLK rising edge	2			ns
REF_CLK rising edge to RXD[1:0], CRS_DV, RX_ER output delay	5.5		14.5	ns

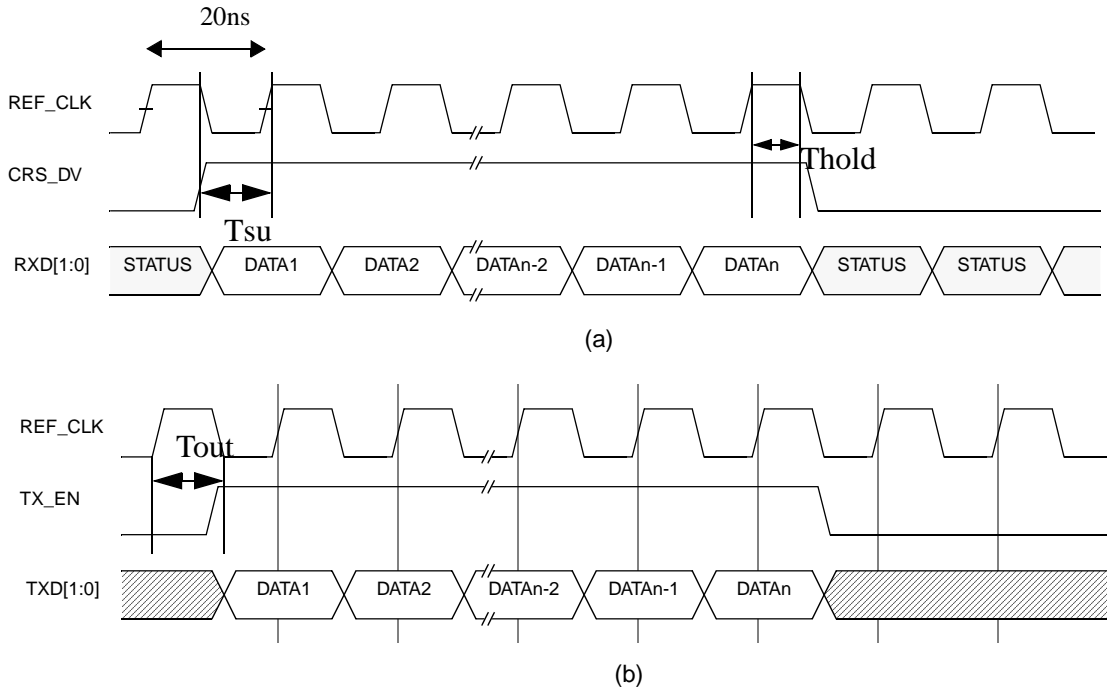


Figure 4-1. Reduced MII Interface Operating at 100Mbps for (a) Receive Data and (b) Transmit Data

## 8.0 System Considerations

### 8.1 Bit Budget Impact

The PHY interface is terminated into a DTE (MAC) when the RMII is used in a switch application. Therefore, additional latency due to the RMII is not significant.

If RMII is used with repeaters, there can be some impact to the bit budget and care must be taken in such a design not to exceed the standard delay parameters for the system. In practice, the repeater will need to be re-designed to accommodate the RMII if desired. Such designs can take advantage of the fact that less de-serialization is done with RMII than MII, thus saving bit times. The PHY may also take advantage of this property and offer less latency in conjunction with an MII.

In the case where a device simply provides a mapping between the MII and the RMII at both the PHY and the MAC/Repeater, the bit budget may be affected. System integrators should check the specifications of MAC/Repeater and PHY chips in determining whether the bit budgets in IEEE 802.3u [2] are met.

## **8.2 Transmit IPG**

Since the reduced MII is an inherently full duplex interface (i.e. there is no loopback of data or carrier from transmit to receive), the delay through the PHY may increase the IPG as seen on the wire if the MAC uses a local timer that corresponds to the IPG timing parameters in IEEE 802.3 [1] and IEEE 802.3u [2]. While it is not a violation to increase this gap, switches are often measured by their ability to achieve “wire speed”.

An alternative to increasing the IPG due to lack of feedback of PHY delay across the reduced MII interface is to allow the MAC’s IPG timer to be smaller than the required parameter by a programmable amount that can be modified to account for the PHY delay such that “wire speed” performance is possible. Note that this is typically the case for “wire speed” devices today.

The architecture of MACs which rely on feedback through loopback of TX\_EN to CRS may be preserved by performing an internal loopback in Half Duplex mode with a delay element that can be programmed to match the delay through the PHY.

## **8.3 Receive IPG**

In order to provide a single synchronous clock reference for all the data interfaces in a multiple port system, some buffering in the PHY is required to account for differences in local versus recovered clock. The depth of this buffer has the potential to increase the IPG if no other precautions were taken. In order to avoid changing IPG as seen by the MAC, this buffer must be smaller than the minimum IPG encountered in real networks.

While the IEEE 802.3 standard [1] ensures that no MAC transmitter ever creates an IPG of less than 96 bits, there are real world scenarios where IPG shrinks (e.g. through repeaters). In no case should an IPG shrink below 36 bits. 36 bits gives sufficient margin for implementations to deal with clock variances over stream lengths consistent with Ethernet framing.

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## **9.0 Future Considerations**

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This specification as written provides a comprehensive solution to reducing the pin count of the MII interface. It has been written to be forward compatible with ideas that are currently beyond the scope of this specification. It is envisioned that this specification may be updated or have an addendum which covers additional desired functionality.

### **9.1 Out of Band Signalling**

The MII’s MDIO/MDC management interface to the PHY provides a standard way to access registers within the PHY. It has been noted that a more real-time interface may be desirable. The values of TXD[1:0]/RXD[1:0] while TX\_EN/CRS\_DV are de-asserted represent unused code space. This specification specifically reserves this code space for future use. Of particular use is transferring speed, link, duplex mode information either from Auto-Negotiation to the MAC or from the MAC to configure the PHY.

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**10.0 References**

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- [1] ISO/IEC 8802-3: 1996, Information technology - Telecommunications and information exchange between systems - Local and metropolitan area networks - Specific requirements - Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications.
- [2] IEEE Std 802.3U, 1995, IEEE Standards for Local and Metropolitan Area Networks: Media Access Control (MAC) Parameters, Physical Layer, Medium Attachment Units, and Repeater for 100 Mb/s Operation, Type 100BASE-T.