HOGESCHOOL VOOR WETENSCHAP & KUNST | DE NAYER INSTITUUT
SINT-KATELIJNE-WAVER

DE NAYER Instituut
J. De Nayerlaan 5
B-2860 Sint-Katelijne-Waver
Tel. (015) 31 69 44
Fax. (015) 31 74 53
e-mail: ppe@denayer.wenk.be
ddr@denayer.wenk.be
tti@denayer.wenk.be
website: emsys.denayer.wenk.be

- OVERVIEW -

AMBA
AVALON
CORECONNECT
WISHBONE

Version 1.1

HOBU-Fonds
Project IWT 020079

Titel	:	Embedded Systeemontwerp op basis van Soft- en Hardcore FPGA's
Projectleider	:	Ing. Patrick Pelgrims
Projectmedewerkers	:	Ing. Dries Driessens Ing. Tom Tierens

AMBA

busname	AMBA
owner	ARM
status	Open, but requires a restrictive agreement
version	Rev. 2.0
url	http://www.arm.com
operating frequency	User defined

Introduction

The Advanced Microcontroller Bus Architecture (AMBA) specification, developed by ARM, defines an on-chip communications standard for designing high-performance embedded microcontrollers.

Three distinct buses are defined within the AMBA specification:

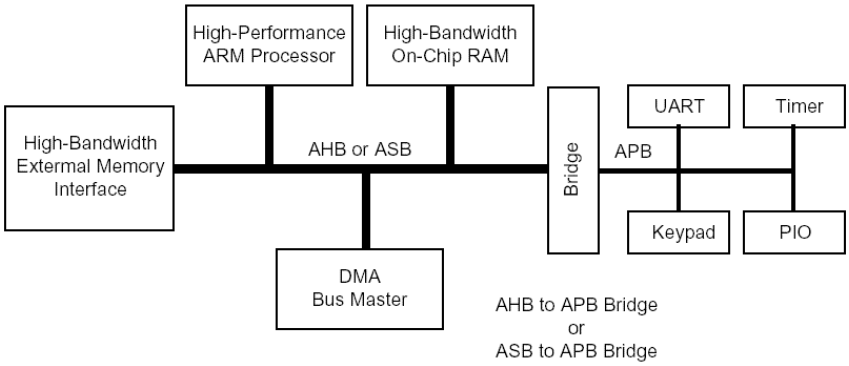
- *Advanced High-performance Bus (AHB)*
  The AMBA AHB is for high-performance, high-clock-frequency system modules.
- *Advanced System Bus (ASB)*
  The AMBA ASB is for high-performance system modules. where the high-performance features of AHB are not required.
- *Advanced Peripheral Bus (APB)*
  AMBA APB is optimised for minimal power consumption and reduced interface complexity to support peripheral functions. APB can be used in conjunction with either version of the system bus.

Depending on the requirements, the system designer has to choose which busses he will use. The choice between AHB and ASP will not be easy, as they try to address the same type of devices. It will be a difficult choice when you keep in mind that there's no clear path integrating devices between ASP and AHB.

busname	AMBA AHB (new generation bus)
data bus width	32- 64- 128- 256-bit
address bus width	32 bit
architecture	(Multi) MASTER / (Multi) SLAVE
	arbitration logic interface well defined Single cycle bus master handover possible
data bus protocol	Single READ/WRITE transfer
	burst transfer (4 – 8 – 16 beats)
	Pipelined
	split transactions supported
	Byte/half-word/word transfer support
data ordering	No dynamic endianess
timing	Synchronous, well defined timing specs
interconnection	multiplexed implementation
supported interconnections	Non-tristate
	Separate data read & write bus required
technology	Technology independent

busname	AMBA ASP (first generation bus)
data bus width	32- 64- 128- 256-bit
address bus width	32 bit
architecture	(Multi) MASTER / (Multi) SLAVE
	arbitration logic interface well defined Single cycle bus master handover possible
data bus protocol	Single READ/WRITE transfer
	burst transfer
	Pipelined
	Byte/half-word/word transfer support
data ordering	Bi-endian possible
timing	Synchronous, well defined timing specs
interconnection	Not defined
supported interconnections	Tristate-bus
	Common data read & write bus required
technology	Technology independent

busname	AMBA APB
data bus width	8-16-32-bit
address bus width	32 bit
tagging	No tagging
architecture	(Single) MASTER (bridge) / (Multi) SLAVE
	No arbitration logic needed
data bus protocol	2 cycle single READ/WRITE transfer
	No burst transfer
	Non-Pipelined
timing	Synchronous, well defined timing specs
interconnection	Not defined
supported interconnections	Non-tristate-bus recommended
	Separate data read & write bus recommended
technology	Technology independent
power	Zero power when not in use



AVALON

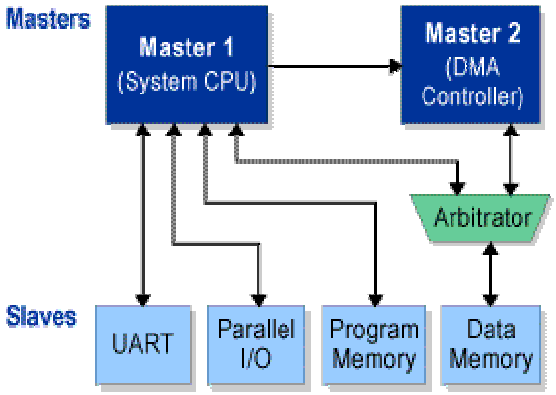
busname	AVALON
owner	Altera
status	Propietary
version	1.2
url	http://www.altera.com
operating frequency	User defined

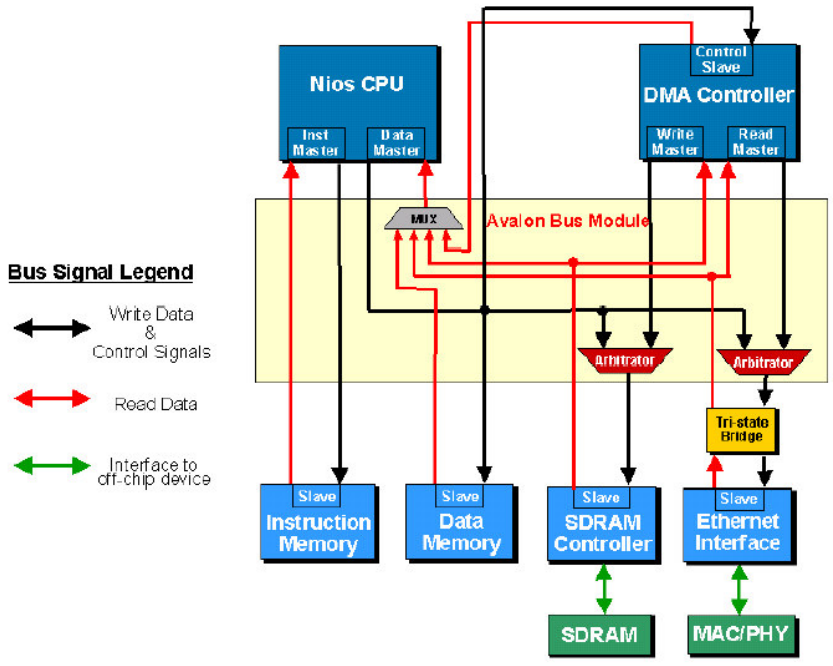
Busname	AVALON
data bus width	8, 16 or 32 bits
address bus width	32-bit
architecture	multi-master / multi slave
	multi-master arbitration logic
specific features	interrupt-priority assignment
	wait-state generation
	read & write transfers with latency
data bus protocol	one or more bus cycles
	streaming transfers (burst)
	single byte, half word or word transfers
	fixed- or peripheral-controlled wait states
	with or without setup time
timing	all signals synchronous with Avalon clock
	simple timing behavior
size	minimal FPGA resources
supported interconnections	separate address, data and control lines
	tri-state signals (external) only with bridge
technology	Altera Avalon can only be implemented on Altera devices using SOPC Builder

Introduction

Avalon is Altera's parameterized interface bus used by the Nios embedded processor. The Avalo switch fabric has a set of pre-defined signal types with which a user can connect one or more intellectual property (IP) blocks.

The wizard-based Altera's SOPC Builder system development tool automatically generates the Avalon switch fabric logic. The generated switch fabric logic includes chipselect signals for data-path multiplexing, address decoding, wait-state generation, interrupt-priority assignment, dynamic-bus sizing, multi-master arbitration logic and advanced switch fabric transfers. The advanced transfers include streaming transfers, read transfers with latency and bus control signals. Avalon masters and slaves interact with each other based on a technique called slave-side arbitration. Slave-side arbitration determines which master gains access to a slave, in the event that multiple masters attempt to access the same slave at the same time.





CORECONNECT

busname	CORECONNECT		
owner	IBM		
status	free, but requires a restrictive license agreement		
version	2.9 (32-bit) 3.5 (64-bit)		
url	http://www.ibm.com/chips/products/coreconnect/		
PLB width	32-bit	64-bit	128-bit
Max. Freq.	66 MHz	133 MHz	183 MHz
Max. Bandwidth	264 MB/s	800 MB/S	2,9 GB/s

Introduction

CoreConnect is an IBM-developed on-chip bus-communications link that enables chip cores from multiple sources to be interconnected to create entire new chips. The CoreConnect technology eases the integration and reuse of processor, system, and peripheral cores within standard product platform designs to achieve overall greater system performance.

The CoreConnect bus architecture includes:

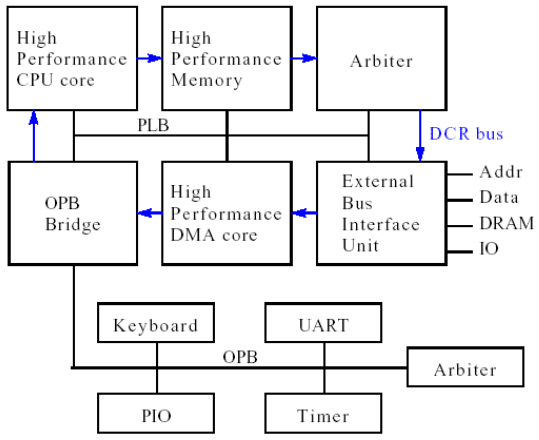
- *processor local bus (PLB)*
  The PLB bus addresses the high performance, low latency system modules and provides the design flexiblity needed in a highly integrated SOC.
- *on-chip peripheral bus (OPB)*
  The OPB bus is optimised to connect to lower speed peripherals and low power consumption.
- *device control register bus (DCR)*
  The Device Control Register (DCR) bus is designed to transfer data between the CPU's general purpose registers (GPRs) and the DCR slave logic's device control registers (DCRs). The DCR bus removes configuration registers from the memory address map, which reduces loading and improves bandwidth of the PLB. The fully synchronous DCR bus provides 10-bit address bus and 32-bit data bus. The DCR bus is typically implemented as a distributed mux across the chip.

CoreConnect is a complete and versatile solution, as it is well thought trough and has a good architecture. It clearly targets high performance systems, thus raising the complexity and offering many features that might be overkill in simple embedded applications.

busname	CORECONNECT PLB
data bus width	32-, 64-, 128-,256-bit
address bus width	32-bit (with address pipelining, reducing latency)
architecture	(Multi) MASTER [MAX 8]/ (Multi) SLAVE
	Arbiters with different priority schemes available as soft-core
data bus protocol	Single READ/WRITE transfer
	Overlapped READ & WRITE (2transfers/cycle)
	Burst transfer (16-64 byte bursts)
	pipelining
	Split transfer support
	Special DMA modes (flyby,…)
timing	Fully synchronous
interconnection	multiplexed implementation (=crossbar switch)
supported interconnections	Non tri-state
	Separate data read & write bus
technology	Technology independent

busname	CORECONNECT OPB
data bus width	8-, 16-,32-bit
address bus width	32-bit
architecture	(Multi) MASTER / (Multi) SLAVE
	Arbiters with different priority schemes available as soft-core
	Dynamic bus sizing possible
data bus protocol	Single READ/WRITE transfer
	Burst support
	Retry support
	Single byte, half word or word transfers
	DMA support
timing	Fully synchronous
interconnection	multiplexed implementation
supported interconnections	Non tri-state
	Separate data read & write bus
technology	Technology independent
power	Bus parking support

busname	CORECONNECT DCR
data bus width	32-bit
address bus width	10-bit
Interconnection	multiplexed implementation
purpose	Transfer data between the CPU's general purpose registers (GPR) and other (peripheral) registers, not meant for real data transfers Designed to reduce load on PLB and OPB



WISHBONE

busname	WISHBONE
owner	Silicore Corporation
status	Open standard, no license required
version	Rev. B.3
url	http://www.opencores.org/wishbone
Operating Frequency	User defined

Introduction

The WISHBONE System-on-Chip (SoC) Interconnect Architecture for Portable IP Cores is a portable interface for use with semiconductor IP cores. Its purpose is to foster design reuse by alleviating system-on-a-chip integration problems. This is accomplished by creating a common, logical interface between IP cores. This improves the portability and reliability of the system, and results in faster time-to-market for the end user.

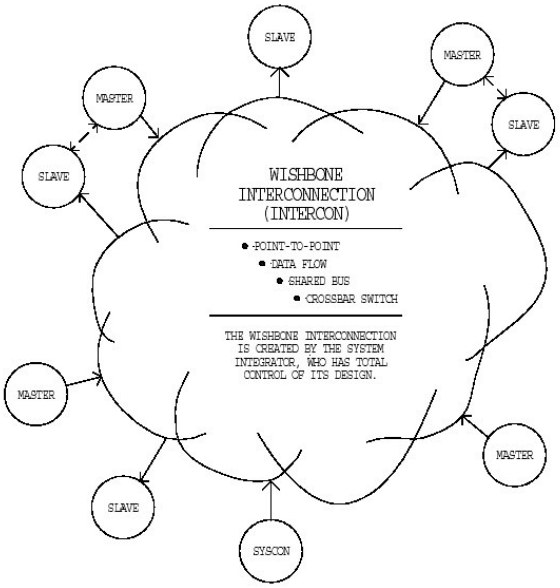
The WISHBONE System-on-Chip Interconnect is recommended by OpenCores as the interface to all cores that require interfacing to other cores inside a chip (FPGA, ASIC, etc.).

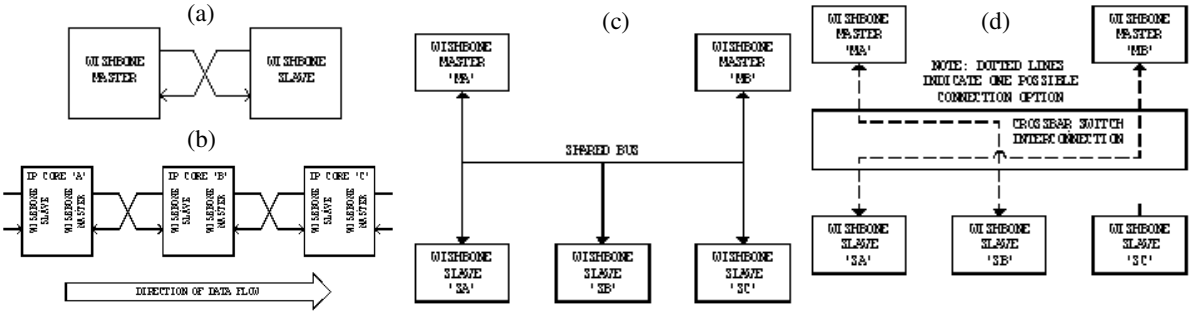
The Wisbone specification is different from other specifications, as it makes use of RULES, RECOMMENDATIONS, SUGGESTIONS, PERMISSIONS and OBSERVATIONS. This allows Wishbone to be a simple, open, highly configurable interface.

Where others have separate interfaces for high- and low speed peripherals, Wishbone defines only one interface. This shouldn't create a problem, as when you need a high- and low speed bus, you can create 2 separate wishbone interfaces.

Because of the highly configurable interface, users might have to create their own substandard of wishbone, specifying data order, meaning of tags, and additional features. This is probably also the cause why e.g. a generic Wishbone-to-AMBA bridge still hasn't been developed yet.

busname	Wishbone
data bus width	8 to 64 bits
address bus width	8 to 64 bits
tagging	address, data-in and out, cycle tags are user defined
architecture	(Multi) MASTER / (Multi) SLAVE
	arbitration logic is user defined (priority, round-robin,… arbiter)
data bus protocol	single READ / WRITE cycle
	BLOCK transfer cycle
	RMW (read-modify-write) cycle
	EVENT cycle
	Up to one data transfer per clock cycle.
data ordering	LITTLE and BIG ENDIAN support
timing	synchronous (simple design, ease of test)
	simple timing specs
size	very few logic gates (dependant on architecture)
Interconnection	point to point (a)
	Data flow (b)
	shared bus (c)
	Crossbar switch (d)
supported interconnections	unidirectional bus
	bi-directional bus
	Multiplexer based interconnections
	Tristate based interconnections
	off-chip I/O
	…
technology	Technology independent





References

AMBA

- http://www.arm.com
- AMBA Specification (Rev. 2.0)
- AMBA AHB lite overview

Avalon

- http://www.altera.com
- Avalon Bus Specification Reference Manual v1.2

Coreconnect

- http://www.ibm.com/chips/products/coreconnect
- http://www.xilinx.com - Coreconnect specification documents (available after registration at the Xilinx Coreconnect lounge)
- The CoreConnect Bus Architecture (Coreconnect short overview document, available at the IBM website)

Wishbone

- http://www.opencores.org/wishbone
- WISHBONE specification Rev. B.3
- Wishbone FAQ

General

- Soc bus comparison (Rudolf Usselmann)
- Advanced bus and interface markets and trends (electronic trend publications, Inc 2001)