

5

Logic Families

Digital integrated circuits are produced using several different circuit configurations and production technologies. Each such approach is called a specific logic family. In this chapter, we will discuss different logic families used to hardware-implement different logic functions in the form of digital integrated circuits. The chapter begins with an introduction to logic families and the important parameters that can be used to characterize different families. This is followed by a detailed description of common logic families in terms of salient features, internal circuitry and interface aspects. Logic families discussed in the chapter include transistor transistor logic (TTL), metal oxide semiconductor (MOS) logic, emitter coupled logic (ECL), bipolar-CMOS (Bi-CMOS) logic and integrated injection logic (I²L).

5.1 Logic Families – Significance and Types

There are a variety of circuit configurations or more appropriately various approaches used to produce different types of digital integrated circuit. Each such fundamental approach is called a *logic family*. The idea is that different logic functions, when fabricated in the form of an IC with the same approach, or in other words belonging to the same logic family, will have identical electrical characteristics. These characteristics include supply voltage range, speed of response, power dissipation, input and output logic levels, current sourcing and sinking capability, fan-out, noise margin, etc. In other words, the set of digital ICs belonging to the same logic family are electrically compatible with each other.

5.1.1 Significance

A digital system in general comprises digital ICs performing different logic functions, and choosing these ICs from the same logic family guarantees that different ICs are compatible with respect to each

other and that the system as a whole performs the intended logic function. In the case where the output of an IC belonging to a certain family feeds the inputs of another IC belonging to a different family, we must use established interface techniques to ensure compatibility. Understanding the features and capabilities of different logic families is very important for a logic designer who is out to make an optimum choice for his new digital design from the available logic family alternatives. A not so well thought out choice can easily underkill or overkill the design with either inadequate or excessive capabilities.

5.1.2 Types of Logic Family

The entire range of digital ICs is fabricated using either bipolar devices or MOS devices or a combination of the two. Different logic families falling in the first category are called bipolar families, and these include diode logic (DL), resistor transistor logic (RTL), diode transistor logic (DTL), transistor transistor logic (TTL), emitter coupled logic (ECL), also known as current mode logic (CML), and integrated injection logic (I^2L). The logic families that use MOS devices as their basis are known as MOS families, and the prominent members belonging to this category are the PMOS family (using P-channel MOSFETs), the NMOS family (using N-channel MOSFETs) and the CMOS family (using both N- and P-channel devices). The Bi-MOS logic family uses both bipolar and MOS devices.

Of all the logic families listed above, the first three, that is, diode logic (DL), resistor transistor logic (RTL) and diode transistor logic (DTL), are of historical importance only. Diode logic used diodes and resistors and in fact was never implemented in integrated circuits. The RTL family used resistors and bipolar transistors, while the DTL family used resistors, diodes and bipolar transistors. Both RTL and DTL suffered from large propagation delay owing to the need for the transistor base charge to leak out if the transistor were to switch from conducting to nonconducting state. Figure 5.1 shows the simplified schematics of a two-input AND gate using DL [Fig. 5.1(a)], a two-input NOR gate using RTL [Fig. 5.1(b)] and a two-input NAND gate using DTL [Fig. 5.1(c)]. The DL, RTL and DTL families, however, were rendered obsolete very shortly after their introduction in the early 1960s owing to the arrival on the scene of transistor transistor logic (TTL).

Logic families that are still in widespread use include TTL, CMOS, ECL, NMOS and Bi-CMOS. The PMOS and I^2L logic families, which were mainly intended for use in custom large-scale integrated (LSI) circuit devices, have also been rendered more or less obsolete, with the NMOS logic family replacing them for LSI and VLSI applications.

5.1.2.1 TTL Subfamilies

The TTL family has a number of subfamilies including standard TTL, low-power TTL, high-power TTL, low-power Schottky TTL, Schottky TTL, advanced low-power Schottky TTL, advanced Schottky TTL and fast TTL. The ICs belonging to the TTL family are designated as 74 or 54 (for standard TTL), 74L or 54L (for low-power TTL), 74H or 54H (for high-power TTL), 74LS or 54LS (for low-power Schottky TTL), 74S or 54S (for Schottky TTL), 74ALS or 54ALS (for advanced low-power Schottky TTL), 74AS or 54AS (for advanced Schottky TTL) and 74F or 54F (for fast TTL). An alphabetic code preceding this indicates the name of the manufacturer (DM for National Semiconductors, SN for Texas Instruments and so on). A two-, three- or four-digit numerical code tells the logic function performed by the IC. It may be mentioned that 74-series devices and 54-series devices are identical except for their operational temperature range. The 54-series devices are MIL-qualified (operational temperature range: -55°C to $+125^\circ\text{C}$) versions of the corresponding 74-series ICs (operational temperature range: 0°C to 70°C). For example, 7400 and 5400 are both quad two-input NAND gates.

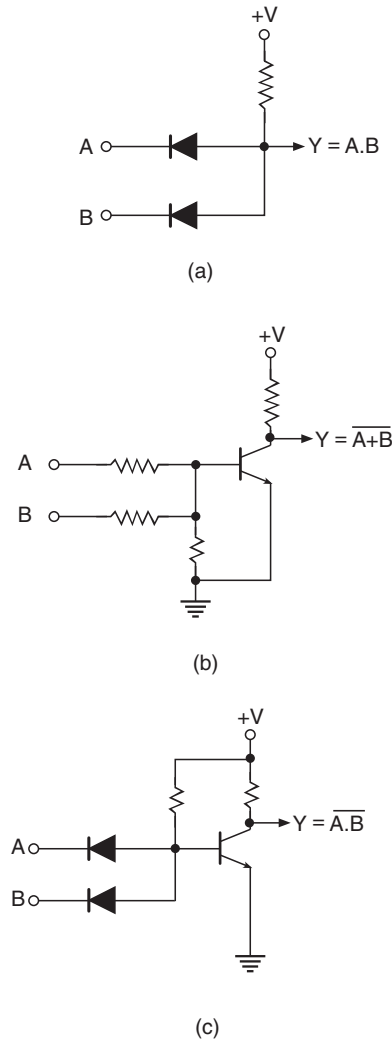


Figure 5.1 (a) Diode logic (b) resistor transistor logic and (c) diode transistor logic.

5.1.2.2 CMOS Subfamilies

The popular CMOS subfamilies include the 4000A, 4000B, 4000UB, 54/74C, 54/74HC, 54/74HCT, 54/74AC and 54/74ACT families. The 4000A CMOS family has been replaced by its high-voltage versions in the 4000B and 4000UB CMOS families, with the former having buffered and the latter having unbuffered outputs. 54/74C, 54/74HC, 54/74HCT, 54/74AC and 54/74ACT are CMOS logic families with pin-compatible 54/74 TTL series logic functions.

5.1.2.3 ECL Subfamilies

The first monolithic emitter coupled logic family was introduced by ON Semiconductor, formerly a division of Motorola, with the MECL-I series of devices in 1962, with the MECL-II series following it up in 1966. Both these logic families have become obsolete. Currently, popular subfamilies of ECL logic include MECL-III (also called the MC 1600 series), the MECL-10K series, the MECL-10H series and the MECL-10E series (ECLinPS and ECLinPSLite). The MECL-10K series further divided into the 10 100-series and 10 200-series devices.

5.2 Characteristic Parameters

In this section, we will briefly describe the parameters used to characterize different logic families. Some of these characteristic parameters, as we will see in the paragraphs to follow, are also used to compare different logic families.

- **HIGH-level input current, I_{IH} .** This is the current flowing into (taken as positive) or out of (taken as negative) an input when a HIGH-level input voltage equal to the minimum HIGH-level output voltage specified for the family is applied. In the case of bipolar logic families such as TTL, the circuit design is such that this current flows into the input pin and is therefore specified as positive. In the case of CMOS logic families, it could be either positive or negative, and only an absolute value is specified in this case.
- **LOW-level input current, I_{IL} .** The LOW-level input current is the maximum current flowing into (taken as positive) or out of (taken as negative) the input of a logic function when the voltage applied at the input equals the maximum LOW-level output voltage specified for the family. In the case of bipolar logic families such as TTL, the circuit design is such that this current flows out of the input pin and is therefore specified as negative. In the case of CMOS logic families, it could be either positive or negative. In this case, only an absolute value is specified.

HIGH-level and LOW-level input current or loading are also sometimes defined in terms of *unit load* (UL). For devices of the TTL family, 1 UL (HIGH) = 40 μA and 1 UL (LOW) = 1.6 mA.

- **HIGH-level output current, I_{OH} .** This is the maximum current flowing out of an output when the input conditions are such that the output is in the logic HIGH state. It is normally shown as a negative number. It tells about the current sourcing capability of the output. The magnitude of I_{OH} determines the number of inputs the logic function can drive when its output is in the logic HIGH state. For example, for the standard TTL family, the minimum guaranteed I_{OH} is $-400 \mu\text{A}$, which can drive 10 standard TTL inputs with each requiring 40 μA in the HIGH state, as shown in Fig. 5.2(a).
- **LOW-level output current, I_{OL} .** This is the maximum current flowing into the output pin of a logic function when the input conditions are such that the output is in the logic LOW state. It tells about the current sinking capability of the output. The magnitude of I_{OL} determines the number of inputs the logic function can drive when its output is in the logic LOW state. For example, for the standard TTL family, the minimum guaranteed I_{OL} is 16 mA, which can drive 10 standard TTL inputs with each requiring 1.6 mA in the LOW state, as shown in Fig. 5.2(b).
- **HIGH-level off-state (high-impedance state) output current, I_{OZH} .** This is the current flowing into an output of a tristate logic function with the ENABLE input chosen so as to establish a high-impedance state and a logic HIGH voltage level applied at the output. The input conditions are chosen so as to produce logic LOW if the device is enabled.

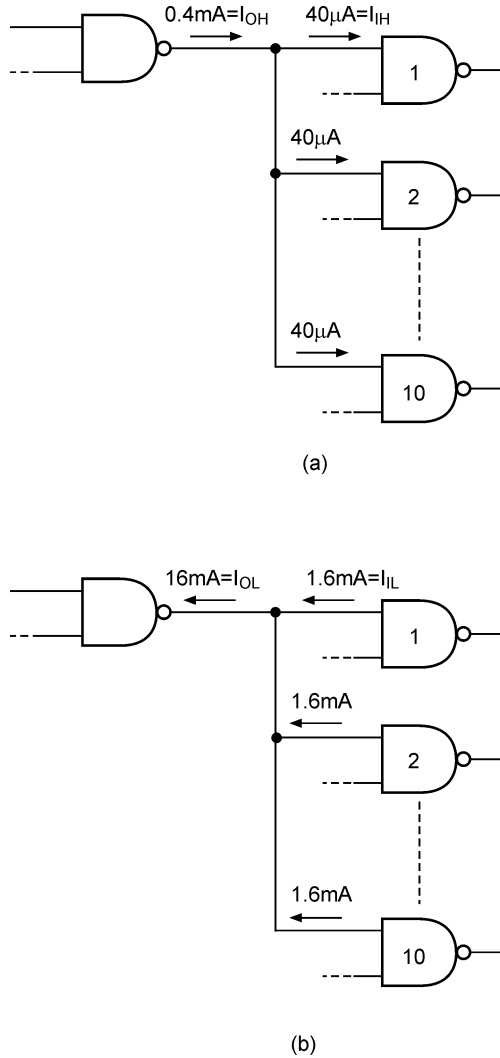


Figure 5.2 Input and output current specifications.

- **LOW-level off-state (high-impedance state) output current, I_{OZL} .** This is the current flowing into an output of a tristate logic function with the ENABLE input chosen so as to establish a high-impedance state and a logic LOW voltage level applied at the output. The input conditions are chosen so as to produce logic HIGH if the device is enabled.
- **HIGH-level input voltage, V_{IH} .** This is the minimum voltage level that needs to be applied at the input to be recognized as a legal HIGH level for the specified family. For the standard TTL family, a 2 V input voltage is a legal HIGH logic state.

- **LOW-level input voltage, V_{IL} .** This is the maximum voltage level applied at the input that is recognized as a legal LOW level for the specified family. For the standard TTL family, an input voltage of 0.8 V is a legal LOW logic state.
- **HIGH-level output voltage, V_{OH} .** This is the minimum voltage on the output pin of a logic function when the input conditions establish logic HIGH at the output for the specified family. In the case of the standard TTL family of devices, the HIGH level output voltage can be as low as 2.4 V and still be treated as a legal HIGH logic state. It may be mentioned here that, for a given logic family, the V_{OH} specification is always greater than the V_{IH} specification to ensure output-to-input compatibility when the output of one device feeds the input of another.
- **LOW-level output voltage, V_{OL} .** This is the maximum voltage on the output pin of a logic function when the input conditions establish logic LOW at the output for the specified family. In the case of the standard TTL family of devices, the LOW-level output voltage can be as high as 0.4 V and still be treated as a legal LOW logic state. It may be mentioned here that, for a given logic family, the V_{OL} specification is always smaller than the V_{IL} specification to ensure output-to-input compatibility when the output of one device feeds the input of another.

The different input/output current and voltage parameters are shown in Fig. 5.3, with HIGH-level current and voltage parameters in Fig. 5.3(a) and LOW-level current and voltage parameters in Fig. 5.3(b). It may be mentioned here that the direction of the LOW-level input and output currents shown in Fig. 5.3(b) is applicable to logic families with current-sinking action such as TTL.

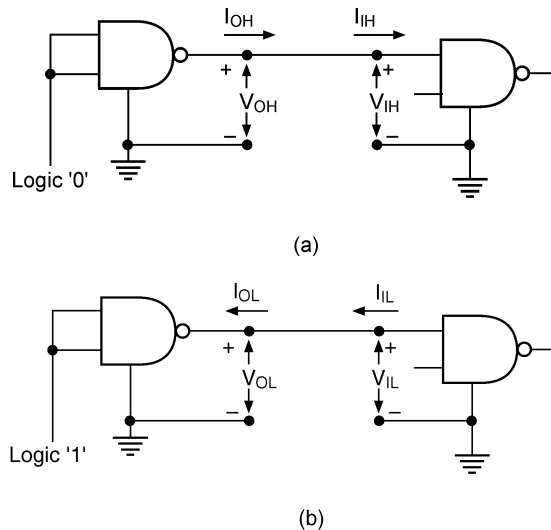


Figure 5.3 (a) HIGH-level current and voltage parameters and (b) LOW-level current and voltage parameters.

- **Supply current, I_{CC} .** The supply current when the output is HIGH, LOW and in the high-impedance state is respectively designated as I_{CCH} , I_{CCL} and I_{CCZ} .
- **Rise time, t_r .** This is the time that elapses between 10 and 90 % of the final signal level when the signal is making a transition from logic LOW to logic HIGH.
- **Fall time, t_f .** This is the time that elapses between 90 and 10 % of the signal level when it is making HIGH to LOW transition.
- **Propagation delay t_p .** The propagation delay is the time delay between the occurrence of change in the logical level at the input and before it is reflected at the output. It is the time delay between the specified voltage points on the input and output waveforms. Propagation delays are separately defined for LOW-to-HIGH and HIGH-to-LOW transitions at the output. In addition, we also define enable and disable time delays that occur during transition between the high-impedance state and defined logic LOW or HIGH states.
- **Propagation delay t_{pLH} .** This is the time delay between specified voltage points on the input and output waveforms with the output changing from LOW to HIGH.
- **Propagation delay t_{pHL} .** This is the time delay between specified voltage points on the input and output waveforms with the output changing from HIGH to LOW. Figure 5.4 shows the two types of propagation delay parameter.
- **Disable time from the HIGH state, t_{pHZ} .** Defined for a tristate device, this is the time delay between specified voltage points on the input and output waveforms with the tristate output changing from the logic HIGH level to the high-impedance state.
- **Disable time from the LOW state, t_{pLZ} .** Defined for a tristate device, this is the time delay between specified voltage points on the input and output waveforms with the tristate output changing from the logic LOW level to the high-impedance state.
- **Enable time from the HIGH state, t_{pZH} .** Defined for a tristate device, this is the time delay between specified voltage points on the input and output waveforms with the tristate output changing from the high-impedance state to the logic HIGH level.

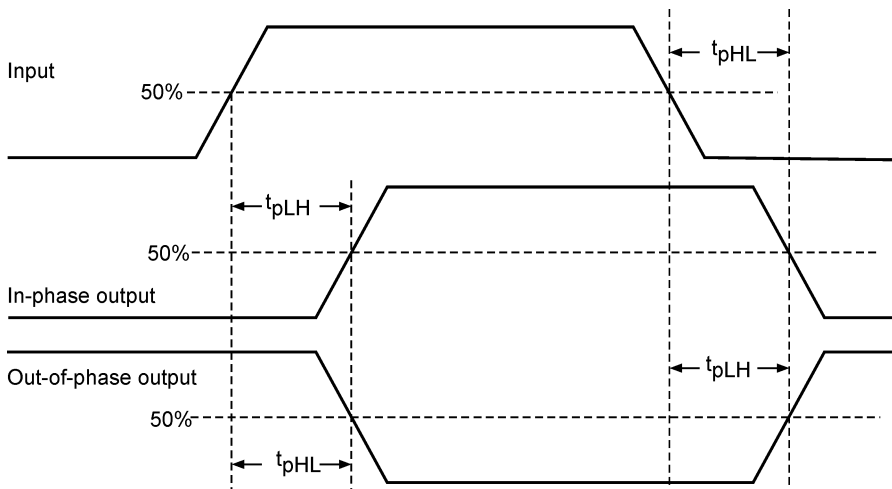


Figure 5.4 Propagation delay parameters.

- **Enable time from the LOW state, t_{pZL} .** Defined for a tristate device, this is the time delay between specified voltage points on the input and output waveforms with the tristate output changing from the high-impedance state to the logic LOW level.
- **Maximum clock frequency, f_{max} .** This is the maximum frequency at which the clock input of a flip-flop can be driven through its required sequence while maintaining stable transitions of logic level at the output in accordance with the input conditions and the product specification. It is also referred to as the maximum toggle rate for a flip-flop or counter device.
- **Power dissipation.** The power dissipation parameter for a logic family is specified in terms of power consumption per gate and is the product of supply voltage V_{CC} and supply current I_{CC} . The supply current is taken as the average of the HIGH-level supply current I_{CCH} and the LOW-level supply current I_{CCL} .
- **Speed–power product.** The speed of a logic circuit can be increased, that is, the propagation delay can be reduced, at the expense of power dissipation. We will recall that, when a bipolar transistor switches between cut-off and saturation, it dissipates the least power but has a large associated switching time delay. On the other hand, when the transistor is operated in the active region, power dissipation goes up while the switching time decreases drastically. It is always desirable to have in a logic family low values for both propagation delay and power dissipation parameters. A useful figure-of-merit used to evaluate different logic families is the speed–power product, expressed in picojoules, which is the product of the propagation delay (measured in nanoseconds) and the power dissipation per gate (measured in milliwatts).
- **Fan-out.** The fan-out is the number of inputs of a logic function that can be driven from a single output without causing any false output. It is a characteristic of the logic family to which the device belongs. It can be computed from I_{OH}/I_{IH} in the logic HIGH state and from I_{OL}/I_{IL} in the logic LOW state. If, in a certain case, the two values I_{OH}/I_{IH} and I_{OL}/I_{IL} are different, the fan-out is taken as the smaller of the two. This description of the fan-out is true for bipolar logic families like TTL and ECL. When determining the fan-out of CMOS logic devices, we should also take into consideration how much input load capacitance can be driven from the output without exceeding the acceptable value of propagation delay.
- **Noise margin.** This is a quantitative measure of noise immunity offered by the logic family. When the output of a logic device feeds the input of another device of the same family, a legal HIGH logic state at the output of the feeding device should be treated as a legal HIGH logic state by the input of the device being fed. Similarly, a legal LOW logic state of the feeding device should be treated as a legal LOW logic state by the device being fed. We have seen in earlier paragraphs while defining important characteristic parameters that legal HIGH and LOW voltage levels for a given logic family are different for outputs and inputs. Figure 5.5 shows the generalized case of legal HIGH and LOW voltage levels for output [Fig. 5.5(a)] and input [Fig. 5.5(b)]. As we can see from the two diagrams, there is a disallowed range of output voltage levels from $V_{OL(max.)}$ to $V_{OH(min.)}$ and an indeterminate range of input voltage levels from $V_{IL(max.)}$ to $V_{IH(min.)}$. Since $V_{IL(max.)}$ is greater than $V_{OL(max.)}$, the LOW output state can therefore tolerate a positive voltage spike equal to $V_{IL(max.)} - V_{OL(max.)}$ and still be a legal LOW input. Similarly, $V_{OH(min.)}$ is greater than $V_{IH(min.)}$, and the HIGH output state can tolerate a negative voltage spike equal to $V_{OH(min.)} - V_{IH(min.)}$ and still be a legal HIGH input. Here, $V_{IL(max.)} - V_{OL(max.)}$ and $V_{OH(min.)} - V_{IH(min.)}$ are respectively known as the LOW-level and HIGH-level noise margin.

Let us illustrate it further with the help of data for the standard TTL family. The minimum legal HIGH output voltage level in the case of the standard TTL is 2.4 V. Also, the minimum legal HIGH input voltage level for this family is 2 V. This implies that, when the output of one device feeds the input of another, there is an available margin of 0.4 V. That is, any negative voltage spikes of amplitude

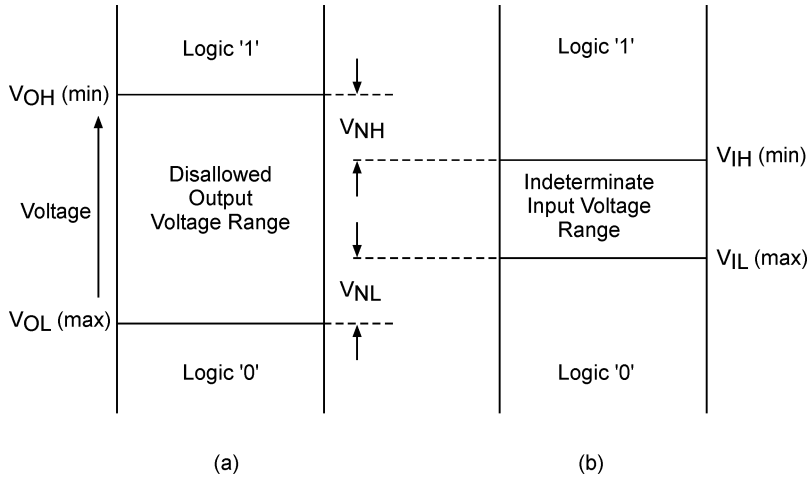


Figure 5.5 Noise margin.

less than or equal to 0.4 V on the signal line do not cause any spurious transitions. Similarly, when the output is in the logic LOW state, the maximum legal LOW output voltage level in the case of the standard TTL is 0.4 V. Also, the maximum legal LOW input voltage level for this family is 0.8 V. This implies that, when the output of one device feeds the input of another, there is again an available margin of 0.4 V. That is, any positive voltage spikes of amplitude less than or equal to 0.4 V on the signal line do not cause any spurious transitions. This leads to the standard TTL family offering a noise margin of 0.4 V. To generalize, the noise margin offered by a logic family, as outlined earlier, can be computed from the HIGH-state noise margin, $V_{NH} = V_{OH}(\text{min.}) - V_{IH}(\text{min.})$, and the LOW-state noise margin, $V_{NL} = V_{IL}(\text{max.}) - V_{OL}(\text{max.})$. If the two values are different, the noise margin is taken as the lower of the two.

Example 5.1

The data sheet of a quad two-input NAND gate specifies the following parameters: $I_{OH}(\text{max.}) = 0.4$ mA, $V_{OH}(\text{min.}) = 2.7$ V, $V_{IH}(\text{min.}) = 2$ V, $V_{IL}(\text{max.}) = 0.8$ V, $V_{OL}(\text{max.}) = 0.4$ V, $I_{OL}(\text{max.}) = 8$ mA, $I_{IL}(\text{max.}) = 0.4$ mA, $I_{IH}(\text{max.}) = 20$ μ A, $I_{CCH}(\text{max.}) = 1.6$ mA, $I_{CCL}(\text{max.}) = 4.4$ mA, $t_{pLH} = t_{pHL} = 15$ ns and a supply voltage range of 5 V. Determine (a) the average power dissipation of a single NAND gate, (b) the maximum average propagation delay of a single gate, (c) the HIGH-state noise margin and (d) the LOW-state noise margin

Solution

- (a) The average supply current $= (I_{CCH} + I_{CCL})/2 = (1.6 + 4.4)/2 = 3$ mA.
 The supply voltage $V_{CC} = 5$ V.
 Therefore, the power dissipation for all four gates in the IC $= 5 \times 3 = 15$ mW.
 The average power dissipation per gate $= 15/4 = 3.75$ mW.
- (b) The propagation delay $= 15$ ns.
- (c) The HIGH-state noise margin $= V_{OH}(\text{min.}) - V_{IH}(\text{min.}) = 2.7 - 2 = 0.7$ V.
- (d) The LOW-state noise margin $= V_{IL}(\text{max.}) - V_{OL}(\text{max.}) = 0.8 - 0.4 = 0.4$ V.

Example 5.2

Refer to example 5.1. How many NAND gate inputs can be driven from the output of a NAND gate of this type?

Solution

- This figure is given by the worst-case fan-out specification of the device.
- Now, the HIGH-state fan-out = $I_{OH}/I_{IH} = 400/20 = 20$.
- The LOW-state fan-out = $I_{OL}/I_{IL} = 8/0.4 = 20$.
- Therefore, the number of inputs that can be driven from a single output = 20.

Example 5.3

Determine the fan-out of IC 74LS04, given the following data: input loading factor (HIGH state) = 0.5 UL, input loading factor (LOW state) = 0.25 UL, output loading factor (HIGH state) = 10 UL, output loading factor (LOW state) = 5 UL, where UL is the unit load.

Solution

- The HIGH-state fan-out can be computed from: fan-out = output loading factor (HIGH)/input loading factor (HIGH) = $10 \text{ UL}/0.5 \text{ UL} = 20$.
- The LOW-state fan-out can be computed from: fan-out = output loading factor (LOW)/input loading factor (LOW) = $5 \text{ UL}/0.25 \text{ UL} = 20$.
- Since the fan-out in the two cases turns out to be the same, it follows that the fan-out = 20.

Example 5.4

A certain TTL gate has $I_{IH} = 20 \mu\text{A}$, $I_{IL} = 0.1 \text{ mA}$, $I_{OH} = 0.4 \text{ mA}$ and $I_{OL} = 4 \text{ mA}$. Determine the input and output loading in the HIGH and LOW states in terms of UL.

Solution

- 1 UL (LOW state) = 1.6 mA and 1 UL (HIGH state) = 40 μA .
- The input loading factor (HIGH state) = $20 \mu\text{A} = 20/40 = 0.5 \text{ UL}$.
- The input loading factor (LOW state) = $0.1 \text{ mA} = 0.1/1.6 = 1/16 \text{ UL}$.
- The output loading factor (HIGH state) = $0.4 \text{ mA} = 0.4/0.04 = 10 \text{ UL}$.
- The output loading factor (LOW state) = $4 \text{ mA} = 4/1.6 = 2.5 \text{ UL}$.

5.3 Transistor Transistor Logic (TTL)

TTL as outlined above stands for transistor transistor logic. It is a logic family implemented with bipolar process technology that combines or integrates NPN transistors, PN junction diodes and diffused resistors in a single monolithic structure to get the desired logic function. The NAND gate is the basic building block of this logic family. Different subfamilies in this logic family, as outlined earlier, include standard TTL, low-power TTL, high-power TTL, low-power Schottky TTL, Schottky TTL, advanced low-power Schottky TTL, advanced Schottky TTL and fast TTL. In the following paragraphs, we will briefly describe each of these subfamilies in terms of internal structure and characteristic parameters.

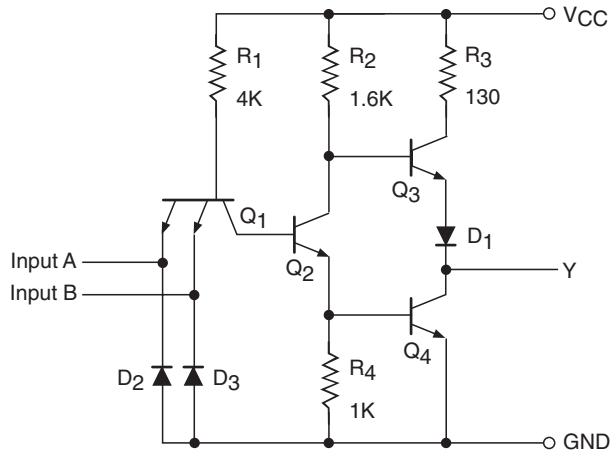


Figure 5.6 Standard TTL NAND gate.

5.3.1 Standard TTL

Figure 5.6 shows the internal schematic of a standard TTL NAND gate. It is one of the four circuits of 5400/7400, which is a quad two-input NAND gate. The circuit operates as follows. Transistor Q_1 is a two-emitter NPN transistor, which is equivalent to two NPN transistors with their base and emitter terminals tied together. The two emitters are the two inputs of the NAND gate. Diodes D_2 and D_3 are used to limit negative input voltages. We will now examine the behaviour of the circuit for various possible logic states at the two inputs.

5.3.1.1 Circuit Operation

When both the inputs are in the logic HIGH state as specified by the TTL family ($V_{IH} = 2\text{ V}$ minimum), the current flows through the base-collector PN junction diode of transistor Q_1 into the base of transistor Q_2 . Transistor Q_2 is turned ON to saturation, with the result that transistor Q_3 is switched OFF and transistor Q_4 is switched ON. This produces a logic LOW at the output, with V_{OL} being 0.4 V maximum when it is sinking a current of 16 mA from external loads represented by inputs of logic functions being driven by the output. The current-sinking action is shown in Fig. 5.7(a). Transistor Q_4 is also referred to as the current-sinking or pull-down transistor, for obvious reasons. Diode D_1 is used to prevent transistor Q_3 from conducting even a small amount of current when the output is LOW. When the output is LOW, Q_4 is in saturation and Q_3 will conduct slightly in the absence of D_1 . Also, the input current I_{IH} in the HIGH state is nothing but the reverse-biased junction diode leakage current and is typically 40 μA .

When either of the two inputs or both inputs are in the logic LOW state, the base-emitter region of Q_1 conducts current, driving Q_2 to cut-off in the process. When Q_2 is in the cut-off state, Q_3 is driven to conduction and Q_4 to cut-off. This produces a logic HIGH output with $V_{OH}(\text{min.}) = 2.4\text{ V}$ guaranteed for minimum supply voltage V_{CC} and a source current of 400 μA . The current-sourcing action is shown in Fig. 5.7(b). Transistor Q_3 is also referred to as the current-sourcing or pull-up transistor. Also, the LOW-level input current I_{IL} , given by $(V_{CC} - V_{BE1})/R_1$, is 1.6 mA (max.) for maximum V_{CC} .

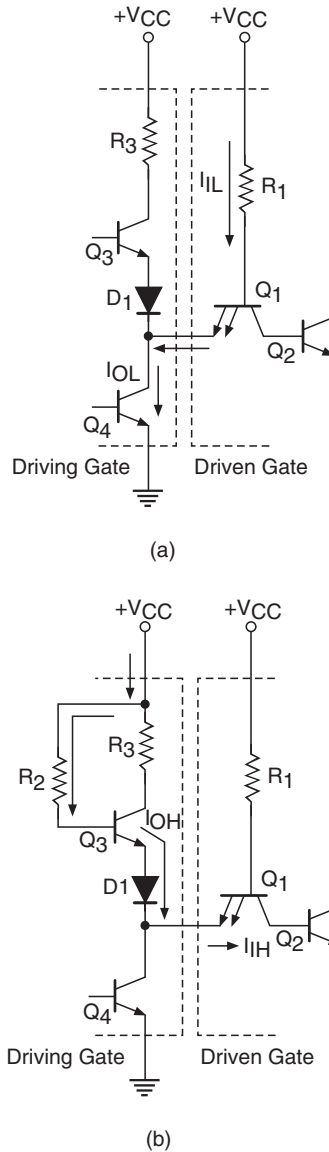


Figure 5.7 (a) Current sinking action and (b) current sourcing action.

5.3.1.2 Totem-Pole Output Stage

Transistors Q_3 and Q_4 constitute what is known as a totem-pole output arrangement. In such an arrangement, either Q_3 or Q_4 conducts at a time depending upon the logic status of the inputs. The totem-pole arrangement at the output has certain distinct advantages. The major advantage of using

a totem-pole connection is that it offers low-output impedance in both the HIGH and LOW output states. In the HIGH state, Q_3 acts as an emitter follower and has an output impedance of about $70\ \Omega$. In the LOW state, Q_4 is saturated and the output impedance is approximately $10\ \Omega$. Because of the low output impedance, any stray capacitance at the output can be charged or discharged very rapidly through this low impedance, thus allowing quick transitions at the output from one state to the other. Another advantage is that, when the output is in the logic LOW state, transistor Q_4 would need to conduct a fairly large current if its collector were tied to V_{CC} through R_3 only. A nonconducting Q_3 overcomes this problem. A disadvantage of the totem-pole output configuration results from the switch-off action of Q_4 being slower than the switch-on action of Q_3 . On account of this, there will be a small fraction of time, of the order of a few nanoseconds, when both the transistors are conducting, thus drawing heavy current from the supply.

5.3.1.3 Characteristic Features

To sum up, the characteristic parameters and features of the standard TTL family of devices include the following: $V_{IL} = 0.8\text{ V}$; $V_{IH} = 2\text{ V}$; $I_{IH} = 40\ \mu\text{A}$; $I_{IL} = 1.6\text{ mA}$; $V_{OH} = 2.4\text{ V}$; $V_{OL} = 0.4\text{ V}$; $I_{OH} = 400\ \mu\text{A}$; $I_{OL} = 16\text{ mA}$; $V_{CC} = 4.75\text{--}5.25\text{ V}$ (74-series) and $4.5\text{--}5.5\text{ V}$ (54-series); propagation delay (for a load resistance of $400\ \Omega$, a load capacitance of 15 pF and an ambient temperature of $25\text{ }^\circ\text{C}$) = 22 ns (max.) for LOW-to-HIGH transition at the output and 15 ns (max.) for HIGH-to-LOW output transition; worst-case noise margin = 0.4 V ; fan-out = 10; I_{CCH} (for all four gates) = 8 mA ; I_{CCL} (for all four gates) = 22 mA ; operating temperature range = $0\text{--}70\text{ }^\circ\text{C}$ (74-series) and $-55\text{ to }+125\text{ }^\circ\text{C}$ (54-series); speed-power product = 100 pJ ; maximum flip-flop toggle frequency = 35 MHz .

5.3.2 Other Logic Gates in Standard TTL

As outlined earlier, the NAND gate is the fundamental building block of the TTL family. In the following paragraphs we will look at the internal schematics of the other logic gates and find for ourselves their similarity to the schematic of the NAND gate discussed in detail in earlier paragraphs.

5.3.2.1 NOT Gate (or Inverter)

Figure 5.8 shows the internal schematic of a NOT gate (inverter) in the standard TTL family. The schematic shown is that of one of the six inverters in a hex inverter (type 7404/5404). The internal schematic is just the same as that of the NAND gate except that the input transistor is a normal single emitter NPN transistor instead of a multi-emitter one. The circuit is self-explanatory.

5.3.2.2 NOR Gate

Figure 5.9 shows the internal schematic of a NOR gate in the standard TTL family. The schematic shown is that of one of the four NOR gates in a quad two-input NOR gate (type 7402/5402). On the input side there are two separate transistors instead of the multi-emitter transistor of the NAND gate. The inputs are fed to the emitters of the two transistors, the collectors of which again feed the bases of the two transistors with their collector and emitter terminals tied together. The resistance values used are the same as those used in the case of the NAND gate. The output stage is also the same totem-pole output stage. The circuit is self-explanatory. The only input condition for which transistors Q_3 and Q_4

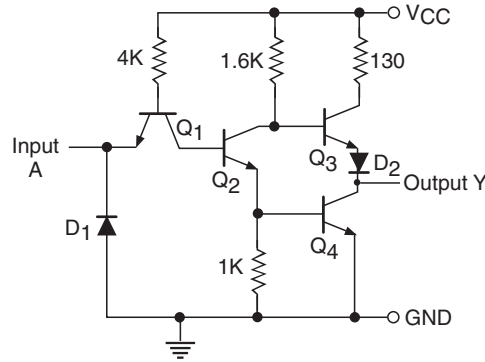


Figure 5.8 Inverter in the standard TTL.

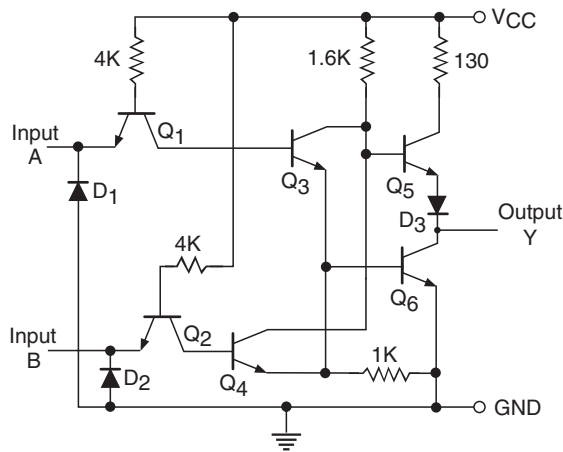


Figure 5.9 NOR gate in the standard TTL.

remain in cut-off, thus driving Q_6 to cut-off and Q_5 to conduction, is the one when both the inputs are in the logic LOW state. The output in such a case is logic HIGH. For all other input conditions, either Q_3 or Q_4 will conduct, driving Q_6 to saturation and Q_5 to cut-off, producing a logic LOW at the output.

5.3.2.3 AND Gate

Figure 5.10 shows the internal schematic of an AND gate in the standard TTL family. The schematic shown is that of one of the four AND gates in a quad two-input AND gate (type 7408/5408). In order to explain how this schematic arrangement behaves as an AND gate, we will begin by investigating the input condition that would lead to a HIGH output. A HIGH output implies Q_6 to be in cut-off and Q_5 to be in conduction. This can happen only when Q_4 is in cut-off. Transistor Q_4 can be in the cut-off

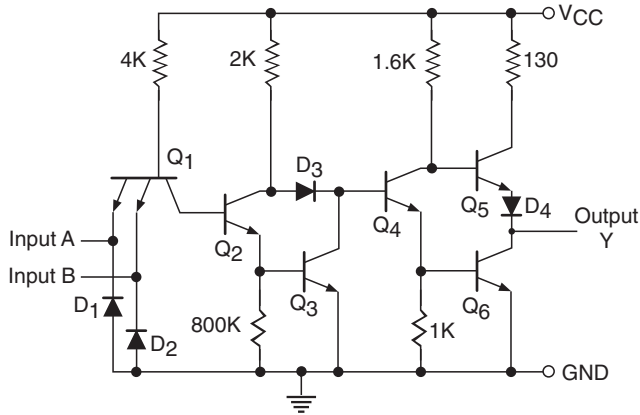


Figure 5.10 AND gate in standard TTL.

state only when both Q_2 and Q_3 are in conduction. This is possible only when both inputs are in the logic HIGH state. Let us now see what happens when either of the two inputs is driven to the LOW state. This drives Q_2 and Q_3 to the cut-off state, which forces Q_4 and subsequently Q_6 to saturation and Q_5 to cut-off.

5.3.2.4 OR Gate

Figure 5.11 shows the internal schematic of an OR gate in the standard TTL family. The schematic shown is that of one of the four OR gates in a quad two-input OR gate (type 7432/5432). We will begin by investigating the input condition that would lead to a LOW output. A LOW output demands a saturated Q_8 and a cut-off Q_7 . This in turn requires Q_6 to be in saturation and Q_5, Q_4 and Q_3 to

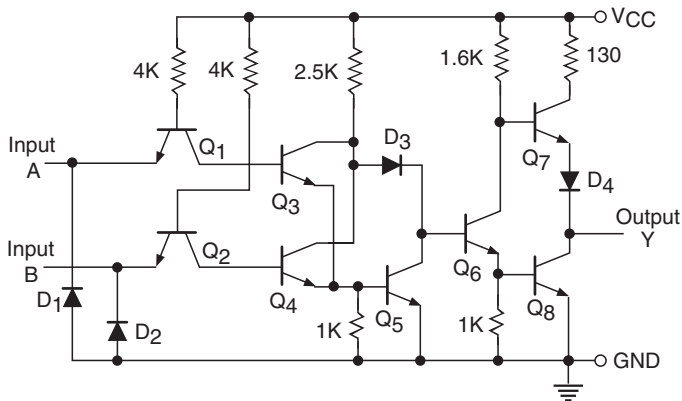


Figure 5.11 OR gate in the standard TTL.

be in cut-off. This is possible only when both Q_1 and Q_2 are in saturation. That is, both inputs are in the logic LOW state. This verifies one of the entries of the truth table of the OR gate. Let us now see what happens when either of the two inputs is driven to the HIGH state. This drives either of the two transistors Q_3 and Q_4 to saturation, which forces Q_5 to saturation and Q_6 to cut-off. This drives Q_7 to conduction and Q_8 to cut-off, producing a logic HIGH output.

5.3.2.5 EXCLUSIVE-OR Gate

Figure 5.12 shows the internal schematic of an EX-OR gate in the standard TTL family. The schematic shown is that of one of the four EX-OR gates in a quad two-input EX-OR gate (type 7486/5486). We will note the similarities between this circuit and that of an OR gate. The only new element is the interconnected pair of transistors Q_7 and Q_8 . We will see that, when both the inputs are either HIGH or LOW, both Q_7 and Q_8 remain in cut-off. In the case of inputs being in the logic HIGH state, the base and emitter terminals of both these transistors remain near the ground potential. In the case of inputs being in the LOW state, the base and emitter terminals of both these transistors remain near V_{CC} . The result is conducting Q_9 and Q_{11} and nonconducting Q_{10} , which leads to a LOW output. When either of the inputs is HIGH, either Q_7 or Q_8 conducts. Transistor Q_7 conducts when input B is HIGH, and transistor Q_8 conducts when input A is HIGH. Conducting Q_7 or Q_8 turns off Q_9 and Q_{11} and turns on Q_{10} , producing a HIGH output. This explains how this circuit behaves as an EX-OR gate.

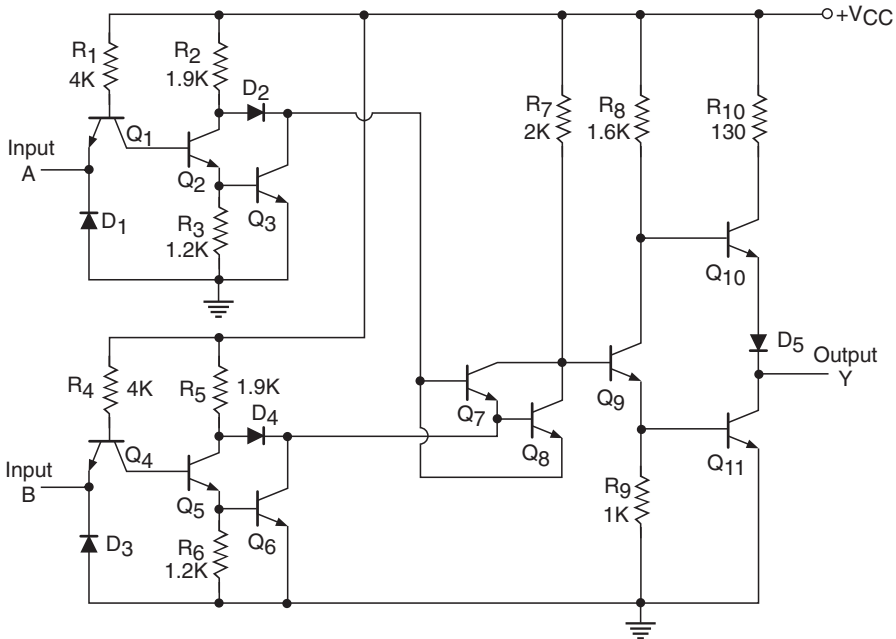


Figure 5.12 EX-OR gate in the standard TTL.

5.3.2.6 AND-OR-INVERT Gate

Figure 5.13 shows the internal schematic of a two-wide, two-input AND-OR-INVERT or AND-NOR gate. The schematic shown is that of one of the two gates in a dual two-wide, two-input AND-OR-INVERT gate (type 7450/5450). The two multi-emitter input transistors Q_1 and Q_2 provide ANDing of their respective inputs. Drive splitters comprising Q_3 , Q_4 , R_3 and R_4 provide the OR function. The output stage provides inversion. The number of emitters in each of the input transistors determines the number of literals in each of the minterms in the output sum-of-products Boolean expression. How wide the gate is going to be is decided by the number of input transistors, which also equals the number of drive splitter transistors.

5.3.2.7 Open Collector Gate

An open collector gate in TTL is one that is without a totem-pole output stage. The output stage in this case does not have the active pull-up transistor. An external pull-up resistor needs to be connected from the open collector terminal of the pull-down transistor to the V_{CC} terminal. The pull-up resistor is typically 10 k Ω . Figure 5.14 shows the internal schematic of a NAND gate with an open collector output. The schematic shown is that of one of the four gates of a quad two-input NAND (type 74/5401). The advantage of open collector outputs is that the outputs of different gates can be wired together, resulting in ANDing of their outputs. WIRE-AND operation was discussed in Chapter 4 on logic gates.

It may be mentioned here that the outputs of totem-pole TTL devices cannot be tied together. Although a common tied output may end up producing an ANDing of individual outputs, such a connection is impractical. This is illustrated in Fig. 5.15, where outputs of two totem-pole output TTL

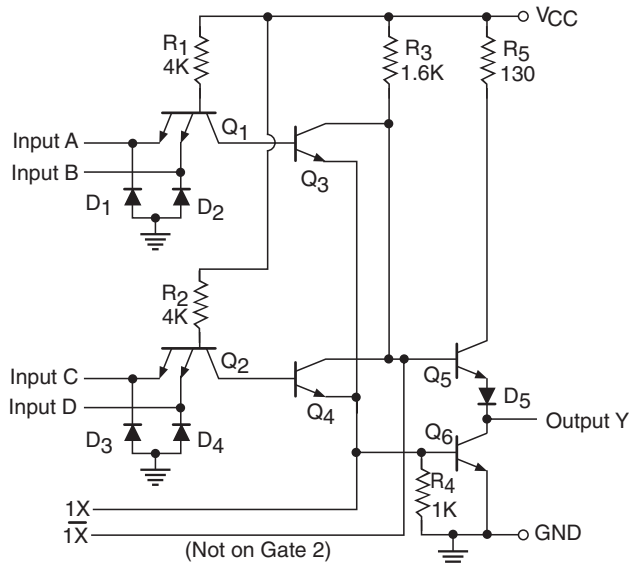


Figure 5.13 Two-input, two-wide AND-OR-INVERT gate.

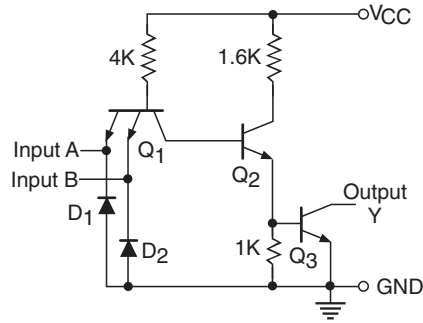


Figure 5.14 NAND gate with an open collector output.

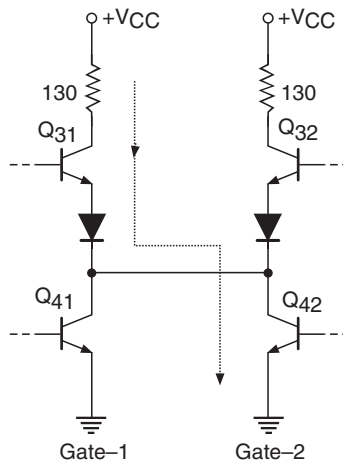


Figure 5.15 Totem-pole output gates tied at the output.

gates have been tied together. Let us assume that the output of one of the gates, say gate-2, is LOW, and the output of the other is HIGH. The result is that a relatively heavier current flows through Q_{31} and Q_{42} . This current, which is of the order of 50–60 mA, exceeds the $I_{OL(max)}$ rating of Q_{42} . This may eventually lead to both transistors getting damaged. Even if they survive, $V_{OL(max)}$ of Q_{42} is no longer guaranteed. In view of this, although totem-pole output TTL gates are not tied together, an accidental shorting of outputs is not ruled out. In such a case, both devices are likely to get damaged. In the case of open collector devices, deliberate or nondeliberate, shorting of outputs produces ANDing of outputs with no risk of either damage or compromised performance specifications.

5.3.2.8 Tristate Gate

Tristate gates were discussed in Chapter 4. A tristate gate has three output states, namely the logic LOW state, the logic HIGH state and the high-impedance state. An external enable input decides

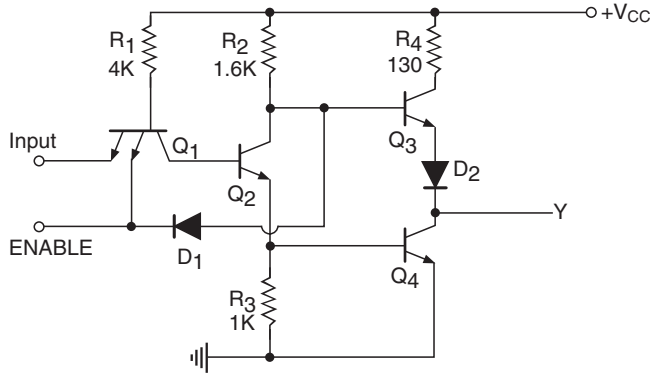


Figure 5.16 Tristate inverter in the TTL.

whether the logic gate works according to its truth table or is in the high-impedance state. Figure 5.16 shows the typical internal schematic of a tristate inverter with an active HIGH enable input. The circuit functions as follows. When the enable input is HIGH, it reverse-biases diode D_1 and also applies a logic HIGH on one of the emitters of the input transistor Q_1 . The circuit behaves like an inverter. When the enable input is LOW, diode D_1 becomes forward biased. A LOW enable input forces Q_2 and Q_4 to cut-off. Also, a forward-biased D_1 forces Q_3 to cut-off. With both output transistors in cut-off, the output essentially is an open circuit and thus presents high output impedance.

5.3.3 Low-Power TTL

The low-power TTL is a low-power variant of the standard TTL where lower power dissipation is achieved at the expense of reduced speed of operation. Figure 5.17 shows the internal schematic of a

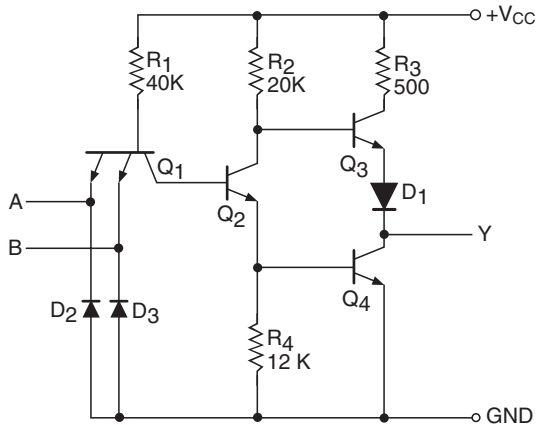


Figure 5.17 NAND gate in the low-power TTL.

low-power TTL NAND gate. The circuit shown is that of one of the four gates inside a quad two-input NAND (type 74L00 or 54L00). The circuit, as we can see, is the same as that of the standard TTL NAND gate except for an increased resistance value of the different resistors used in the circuit. Increased resistance values lead to lower power dissipation.

5.3.3.1 Characteristic Features

Characteristic features of this family are summarized as follows: $V_{IH} = 2\text{ V}$; $V_{IL} = 0.7\text{ V}$; $I_{IH} = 10\ \mu\text{A}$; $I_{IL} = 0.18\text{ mA}$; $V_{OH} = 2.4\text{ V}$; $V_{OL} = 0.4\text{ V}$; $I_{OH} = 200\ \mu\text{A}$; $I_{OL} = 3.6\text{ mA}$; $V_{CC} = 4.75\text{--}5.25\text{ V}$ (74-series) and $4.5\text{--}5.5\text{ V}$ (54-series); propagation delay (for a load resistance of $4000\ \Omega$, a load capacitance of 50 pF , $V_{CC} = 5\text{ V}$ and an ambient temperature of $25\text{ }^\circ\text{C}$) = 60 ns (max.) for both LOW-to-HIGH and HIGH-to-LOW output transitions; worst-case noise margin = 0.3 V ; fan-out = 20; I_{CCH} (for all four gates) = 0.8 mA ; I_{CCL} (for all four gates) = 2.04 mA ; operating temperature range = $0\text{--}70\text{ }^\circ\text{C}$ (74-series) and $-55\text{ to }+125\text{ }^\circ\text{C}$ (54-series); speed-power product = 33 pJ ; maximum flip-flop toggle frequency = 3 MHz .

5.3.4 High-Power TTL (74H/54H)

The high-power TTL is a high-power, high-speed variant of the standard TTL where improved speed (reduced propagation delay) is achieved at the expense of higher power dissipation. Figure 5.18 shows the internal schematic of a high-power TTL NAND gate. The circuit shown is that of one of the four gates inside a quad two-input NAND (type 74H00 or 54H00). The circuit, as we can see, is nearly the same as that of the standard TTL NAND gate except for the transistor Q_3 -diode D_1 combination in the totem-pole output stage having been replaced by a Darlington arrangement comprising Q_3 , Q_5 and R_5 . The Darlington arrangement does the same job as diode D_1 in the conventional totem-pole arrangement. It ensures that Q_5 does not conduct at all when the output is LOW. The decreased resistance values of different resistors used in the circuit lead to higher power dissipation.

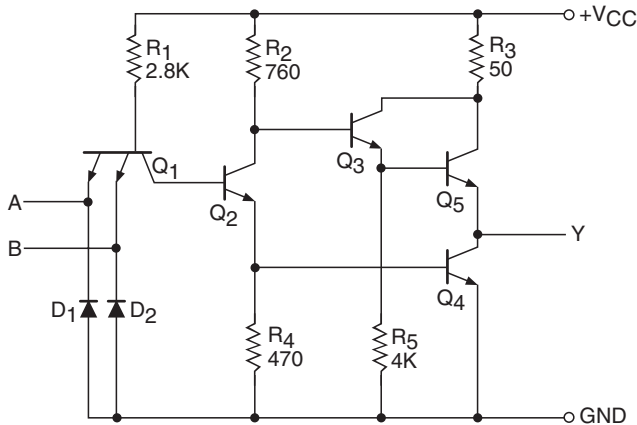


Figure 5.18 NAND gate in the high-power TTL.

5.3.4.1 Characteristic Features

Characteristic features of this family are summarized as follows: $V_{IH} = 2\text{ V}$; $V_{IL} = 0.8\text{ V}$; $I_{IH} = 50\text{ }\mu\text{A}$; $I_{IL} = 2\text{ mA}$; $V_{OH} = 2.4\text{ V}$; $V_{OL} = 0.4\text{ V}$; $I_{OH} = 500\text{ }\mu\text{A}$; $I_{OL} = 20\text{ mA}$; $V_{CC} = 4.75\text{--}5.25\text{ V}$ (74-series) and $4.5\text{--}5.5\text{ V}$ (54-series); propagation delay (for a load resistance of $280\text{ }\Omega$, a load capacitance of 25 pF , $V_{CC} = 5\text{ V}$ and an ambient temperature of $25\text{ }^\circ\text{C}$) = 10 ns (max.) for both LOW-to-HIGH and HIGH-to-LOW output transitions; worst-case noise margin = 0.4 V ; fan-out = 10; I_{CCH} (for all four gates) = 16.8 mA ; I_{CCL} (for all four gates) = 40 mA ; operating temperature range = $0\text{--}70\text{ }^\circ\text{C}$ (74-series) and $-55\text{ to }+125\text{ }^\circ\text{C}$ (54-series); speed-power product = 132 pJ ; maximum flip-flop frequency = 50 MHz .

5.3.5 Schottky TTL (74S/54S)

The Schottky TTL offers a speed that is about twice that offered by the high-power TTL for the same power consumption. Figure 5.19 shows the internal schematic of a Schottky TTL NAND gate. The circuit shown is that of one of the four gates inside a quad two-input NAND (type 74S00 or 54S00). The circuit, as we can see, is nearly the same as that of the high-power TTL NAND gate. The transistors used in the circuit are all Schottky transistors with the exception of Q_5 . A Schottky Q_5 would serve no purpose, with Q_4 being a Schottky transistor. A Schottky transistor is nothing but a conventional bipolar transistor with a Schottky diode connected between its base and collector terminals. The Schottky diode with its metal-semiconductor junction not only is faster but also offers a lower forward voltage drop of 0.4 V as against 0.7 V for a P-N junction diode for the same value of forward current. The presence of a Schottky diode does not allow the transistor to go to deep saturation. The moment the collector voltage of the transistor tends to go below about 0.3 V , the Schottky diode becomes forward biased and bypasses part of the base current through it. The collector voltage is thus not allowed to go to the saturation value of 0.1 V and gets clamped around 0.3 V . While the power consumption of a Schottky TTL gate is almost the same as that of a high-power TTL gate owing to nearly the same values of the resistors used in the circuit, the Schottky TTL offers a higher speed on account of the use of Schottky transistors.

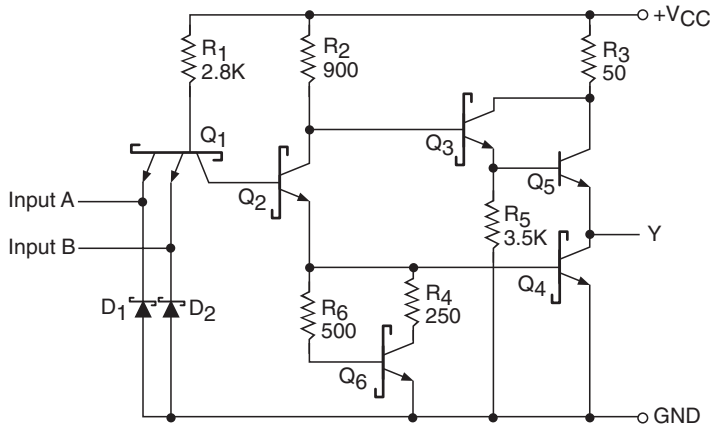


Figure 5.19 NAND gate in the Schottky TTL.

5.3.5.1 Characteristic Features

Characteristic features of this family are summarized as follows: $V_{IH} = 2\text{ V}$; $V_{IL} = 0.8\text{ V}$; $I_{IH} = 50\text{ }\mu\text{A}$; $I_{IL} = 2\text{ mA}$; $V_{OH} = 2.7\text{ V}$; $V_{OL} = 0.5\text{ V}$; $I_{OH} = 1\text{ mA}$; $I_{OL} = 20\text{ mA}$; $V_{CC} = 4.75\text{--}5.25\text{ V}$ (74-series) and $4.5\text{--}5.5\text{ V}$ (54-series); propagation delay (for a load resistance of $280\text{ }\Omega$, a load capacitance of 15 pF , $V_{CC} = 5\text{ V}$ and an ambient temperature of $25\text{ }^\circ\text{C}$) = 5 ns (max.) for LOW-to-HIGH and 4.5 ns (max.) for HIGH-to-LOW output transitions; worst-case noise margin = 0.3 V ; fan-out = 10; I_{CCH} (for all four gates) = 16 mA ; I_{CCL} (for all four gates) = 36 mA ; operating temperature range = $0\text{--}70\text{ }^\circ\text{C}$ (74-series) and $-55\text{ to }+125\text{ }^\circ\text{C}$ (54-series); speed-power product = 57 pJ ; maximum flip-flop toggle frequency = 125 MHz .

5.3.6 Low-Power Schottky TTL (74LS/54LS)

The low-power Schottky TTL is a low power consumption variant of the Schottky TTL. Figure 5.20 shows the internal schematic of a low-power Schottky TTL NAND gate. The circuit shown is that of one of the four gates inside a quad two-input NAND (type 74LS00 or 54LS00). We can notice the significantly increased value of resistors R_1 and R_2 used to achieve lower power consumption. Lower power consumption, of course, occurs at the expense of reduced speed or increased propagation delay. Resistors R_3 and R_5 , which primarily affect speed, have not been increased in the same proportion with respect to the corresponding values used in the Schottky TTL as resistors R_1 and R_2 . That is why, although the low-power Schottky TTL draws an average maximum supply current of 3 mA (for all four gates) as against 26 mA for the Schottky TTL, the propagation delay is 15 ns in LS-TTL as against 5 ns for S-TTL. Diodes D_3 and D_4 reduce the HIGH-to-LOW propagation delay. While D_3 speeds up the turn-off of Q_4 , D_4 sinks current from the load. Another noticeable difference in the internal schematics of the low-power Schottky TTL NAND and Schottky TTL NAND is the replacement of the

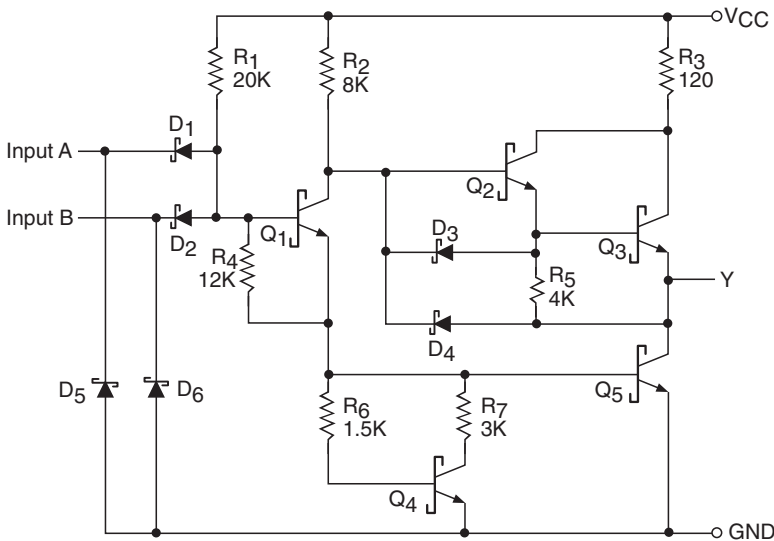


Figure 5.20 NAND gate in the low-power Schottky TTL.

multi-emitter input transistor of the Schottky TTL by diodes D_1 and D_2 and resistor R_1 . The junction diodes basically replace the two emitter-base junctions of the multi-emitter input transistor Q_1 of the Schottky TTL NAND (Fig. 5.19). The reason for doing so is that Schottky diodes can be made smaller than the transistor and therefore will have lower parasitic capacitances. Also, since Q_1 of LS-TTL (Fig. 5.20) cannot saturate, it is not necessary to remove its base charge with a bipolar junction transistor.

5.3.6.1 Characteristic Features

Characteristic features of this family are summarized as follows: $V_{IH} = 2\text{ V}$; $V_{IL} = 0.8\text{ V}$; $I_{IH} = 20\ \mu\text{A}$; $I_{IL} = 0.4\text{ mA}$; $V_{OH} = 2.7\text{ V}$; $V_{OL} = 0.5\text{ V}$; $I_{OH} = 0.4\text{ mA}$; $I_{OL} = 8\text{ mA}$; $V_{CC} = 4.75\text{--}5.25\text{ V}$ (74-series) and $4.5\text{--}5.5\text{ V}$ (54-series); propagation delay (for a load resistance of $280\ \Omega$, a load capacitance of 15 pF , $V_{CC} = 5\text{ V}$ and an ambient temperature of $25\text{ }^\circ\text{C}$) = 15 ns (max.) for both LOW-to-HIGH and HIGH-to-LOW output transitions; worst-case noise margin = 0.3 V ; fan-out = 20; I_{CCH} (for all four gates) = 1.6 mA ; I_{CCL} (for all four gates) = 4.4 mA ; operating temperature range = $0\text{--}70\text{ }^\circ\text{C}$ (74-series) and $-55\text{ to }+125\text{ }^\circ\text{C}$ (54-series); speed-power product = 18 pJ ; maximum flip-flop toggle frequency = 45 MHz .

5.3.7 Advanced Low-Power Schottky TTL (74ALS/54ALS)

The basic ideas behind the development of the advanced low-power Schottky TTL (ALS-TTL) and advanced Schottky TTL (AS-TTL) discussed in Section 5.3.8 were further to improve both speed and power consumption performance of the low-power Schottky TTL and Schottky TTL families respectively. In the TTL subfamilies discussed so far, we have seen that different subfamilies achieved improved speed at the expense of increased power consumption, or vice versa. For example, the low-power TTL offered lower power consumption over standard TTL at the cost of reduced speed. The high-power TTL, on the other hand, offered improved speed over the standard TTL at the expense of increased power consumption. ALS-TTL and AS-TTL incorporate certain new circuit design features and fabrication technologies to achieve improvement of both parameters. Both ALS-TTL and AS-TTL offer an improvement in speed-power product respectively over LS-TTL and S-TTL by a factor of 4. Salient features of ALS-TTL and AS-TTL include the following:

1. All saturating transistors are clamped by using Schottky diodes. This virtually eliminates the storage of excessive base charge, thus significantly reducing the turn-off time of the transistors. Elimination of transistor storage time also provides stable switching times over the entire operational temperature range.
2. Inputs and outputs are clamped by Schottky diodes to limit the negative-going excursions.
3. Both ALS-TTL and AS-TTL use ion implantation rather than a diffusion process, which allows the use of small geometries leading to smaller parasitic capacitances and hence reduced switching times.
4. Both ALS-TTL and AS-TTL use oxide isolation rather than junction isolation between transistors. This leads to reduced epitaxial layer-substrate capacitance, which further reduces the switching times.
5. Both ALS-TTL and AS-TTL offer improved input threshold voltage and reduced low-level input current.
6. Both ALS-TTL and AS-TTL feature active turn-off of the LOW-level output transistor, producing a better HIGH-level output voltage and thus a higher HIGH-level noise immunity.

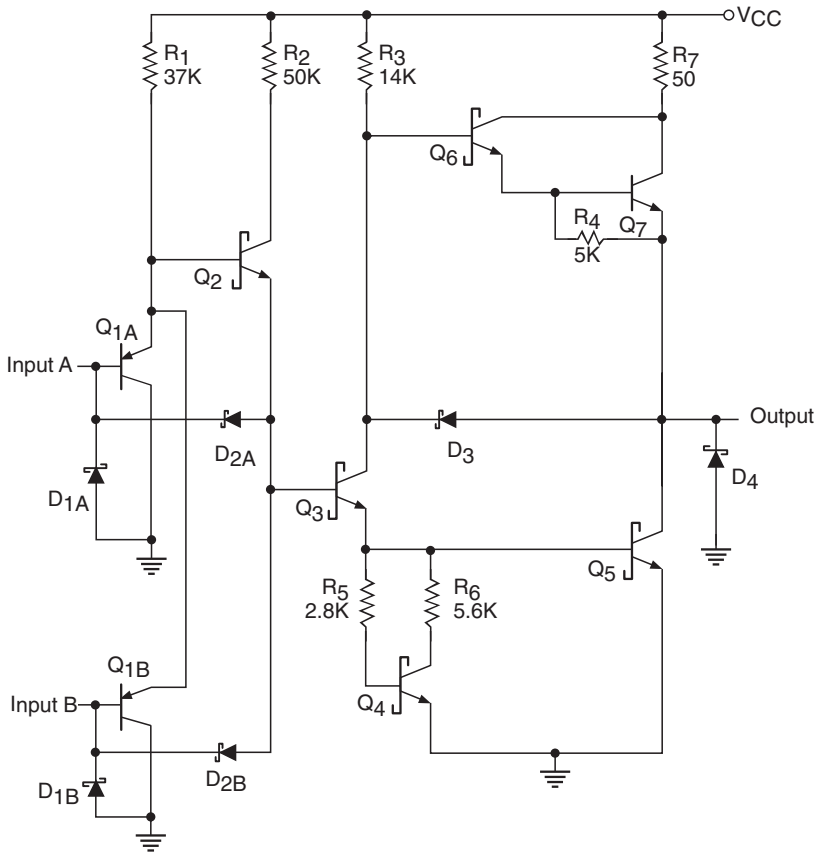


Figure 5.21 NAND gate in the ALS-TTL.

Figure 5.21 shows the internal schematic of an advanced low-power Schottky TTL NAND gate. The circuit shown is that of one of the four gates inside a quad two-input NAND (type 74ALS00 or 54ALS00). The multi-emitter input transistor is replaced by two PNP transistors Q_{1A} and Q_{1B} . Diodes D_{1A} and D_{1B} provide input clamping to negative excursions. Buffering offered by Q_{1A} or Q_{1B} and Q_2 reduces the LOW-level input current by a factor of $(1 + h_{FE} \text{ of } Q_{1A})$. HIGH-level output voltage is determined primarily by V_{CC} , transistors Q_6 and Q_7 and resistors R_4 and R_7 and is typically $(V_{CC} - 2)$ V. LOW-level output voltage is determined by the turn-on characteristics of Q_5 . Transistor Q_5 gets sufficient base drive through R_3 and a conducting Q_3 whose base terminal in turn is driven by a conducting Q_2 whenever either or both inputs are HIGH. Transistor Q_4 provides active turn-off for Q_5 .

5.3.7.1 Characteristic Features

Characteristic features of this family are summarized as follows: $V_{IH} = 2$ V; $V_{IL} = 0.8$ V; $I_{IH} = 20$ μ A; $I_{IL} = 0.1$ mA; $V_{OH} = (V_{CC} - 2)$ V; $V_{OL} = 0.5$ V; $I_{OH} = 0.4$ mA; $I_{OL} = 8$ mA (74ALS) and 4 mA (54ALS);

$V_{CC} = 4.5\text{--}5.5\text{ V}$; propagation delay (for a load resistance of $500\ \Omega$, a load capacitance of 50 pF , $V_{CC} = 4.5\text{--}5.5\text{ V}$ and an ambient temperature of minimum to maximum) = $11\text{ ns}/16\text{ ns}$ (max.) for LOW-to-HIGH and $8\text{ ns}/13\text{ ns}$ for HIGH-to-LOW output transitions (74ALS/54ALS); worst-case noise margin = 0.3 V ; fan-out = 20 ; I_{CCH} (for all four gates) = 0.85 mA ; I_{CCL} (for all four gates) = 3 mA ; operating temperature range = $0\text{--}70\text{ }^\circ\text{C}$ (74-series) and $-55\text{ to }+125\text{ }^\circ\text{C}$ (54-series); speed-power product = 4.8 pJ ; maximum flip-flop toggle frequency = 70 MHz .

5.3.8 Advanced Schottky TTL (74AS/54AS)

Figure 5.22 shows the internal schematic of an advanced Schottky TTL NAND gate. The circuit shown is that of one of the four gates inside a quad two-input NAND (type 74AS00 or 54AS00). Salient

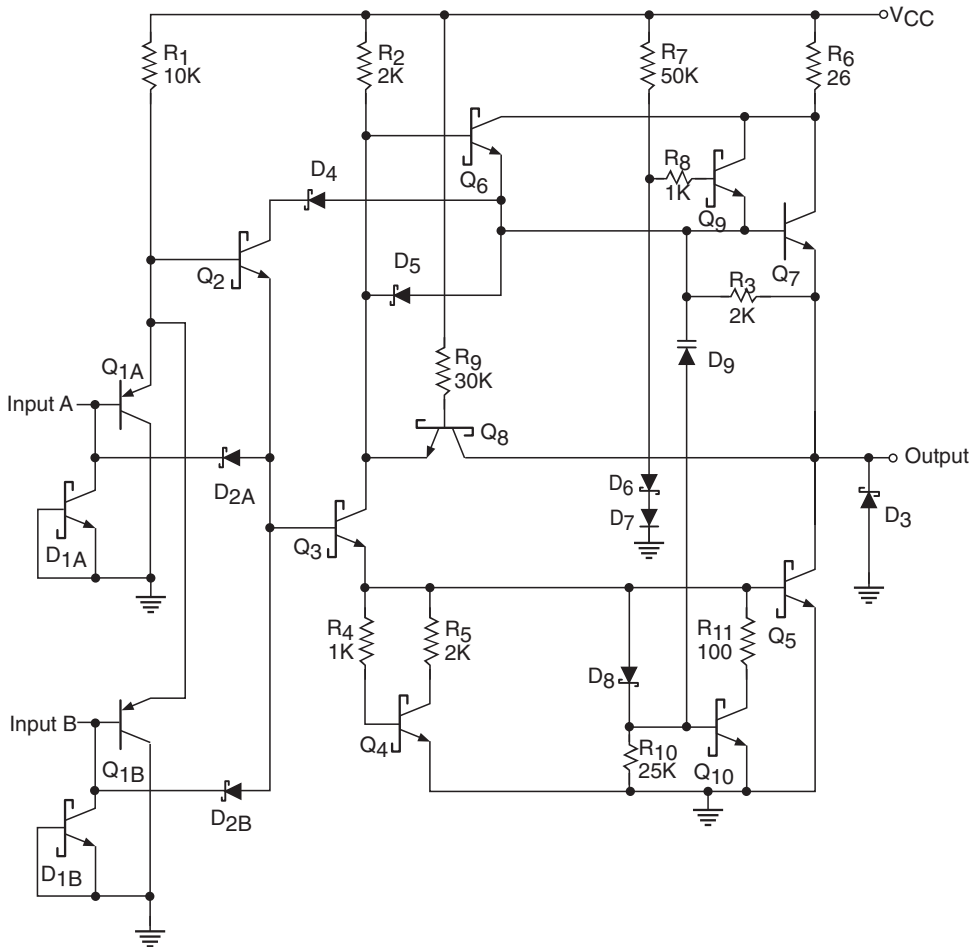


Figure 5.22 NAND gate in the AS-TTL.

features of ALS-TTL and AS-TTL have been discussed at length in the preceding paragraphs. As is obvious from the internal circuit schematic of the AS-TTL NAND gate, it has some additional circuits not found in ALS-TTL devices. These are added to enhance the throughput of AS-TTL family devices. Transistor Q_{10} provides a discharge path for the base-collector capacitance of Q_5 . In the absence of Q_{10} , a rising voltage across the output forces current into the base of Q_5 through its base-collector capacitance, thus causing it to turn on. Transistor Q_{10} turns on through D_9 , thus keeping transistor Q_5 in the cut-off state.

5.3.8.1 Characteristic Features

Characteristic features of this family are summarized as follows: $V_{IH} = 2\text{ V}$; $V_{IL} = 0.8\text{ V}$; $I_{IH} = 20\text{ }\mu\text{A}$; $I_{IL} = 0.5\text{ mA}$; $V_{OH} = (V_{CC} - 2)\text{ V}$; $V_{OL} = 0.5\text{ V}$; $I_{OH} = 2\text{ mA}$; $I_{OL} = 20\text{ mA}$; $V_{CC} = 4.5\text{--}5.5\text{ V}$; propagation delay (for a load resistance of $50\text{ }\Omega$, a load capacitance of 50 pF , $V_{CC} = 4.5\text{--}5.5\text{ V}$ and an ambient temperature of minimum to maximum) = $4.5\text{ ns}/5\text{ ns}$ (max.) for LOW-to-HIGH and $4\text{ ns}/5\text{ ns}$ (max.) for HIGH-to-LOW output transitions (74AS/54AS); worst-case noise margin = 0.3 V ; fan-out = 40; I_{CCH} (for all four gates) = 3.2 mA ; I_{CCL} (for all four gates) = 17.4 mA ; operating temperature range = $0\text{--}70\text{ }^\circ\text{C}$ (74-series) and $-55\text{ to }+125\text{ }^\circ\text{C}$ (54-series); speed-power product = 13.6 pJ ; maximum flip-flop toggle frequency = 200 MHz .

5.3.9 Fairchild Advanced Schottky TTL (74F/54F)

The Fairchild Advanced Schottky TTL family, commonly known as FAST logic, is similar to the AS-TTL family. Figure 5.23 shows the internal schematic of a Fairchild Advanced Schottky TTL

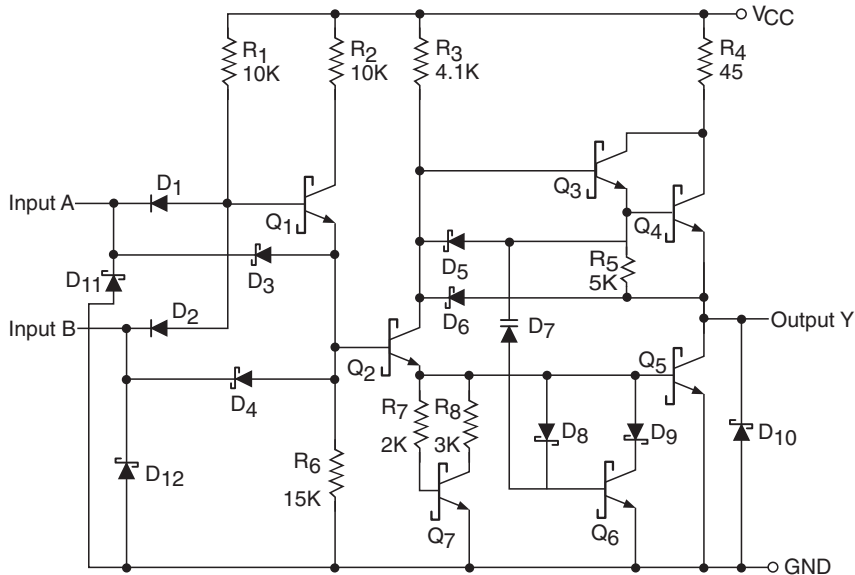


Figure 5.23 NAND gate in the FAST TTL.

NAND gate. The circuit shown is that of one of the four gates inside a quad two-input NAND (type 74F00 or 54F00). The DTL kind of input with emitter follower configuration of Q_1 provides a good base drive to Q_2 . The ‘Miller killer’ configuration comprising varactor diode D_7 , transistor Q_6 and associated components speeds up LOW-to-HIGH transition. During LOW-to-HIGH transition, voltage at the emitter terminal of Q_3 begins to rise while Q_5 is still conducting. Varactor diode D_7 conducts, thus supplying base current to Q_6 . A conducting Q_6 provides a discharge path for the charge stored in the base-collector capacitance of Q_5 , thus expediting its turn-off.

5.3.9.1 Characteristic Features

Characteristic features of this family are summarized as follows: $V_{IH} = 2\text{ V}$; $V_{IL} = 0.8\text{ V}$; $I_{IH} = 20\ \mu\text{A}$; $I_{IL} = 0.6\text{ mA}$; $V_{OH} = 2.7\text{ V}$; $V_{OL} = 0.5\text{ V}$; $I_{OH} = 1\text{ mA}$; $I_{OL} = 20\text{ mA}$; $V_{CC} = 4.75\text{--}5.25\text{ V}$ (74F) and $4.5\text{--}5.5\text{ V}$ (54F); propagation delay (a load resistance of $500\ \Omega$, a load capacitance of 50 pF and full operating voltage and temperature ranges) = $5.3\text{ ns}/7\text{ ns}$ (max.) for LOW-to-HIGH and $6\text{ ns}/6.5\text{ ns}$ (max.) for HIGH-to-LOW output transitions (74AS/54AS); worst-case noise margin = 0.3 V ; fan-out = 40; I_{CCH} (for all four gates) = 2.8 mA ; I_{CCL} (for all four gates) = 10.2 mA ; operating temperature range = $0\text{--}70\text{ }^\circ\text{C}$ (74F-series) and $-55\text{ to }+125\text{ }^\circ\text{C}$ (54F-series); speed-power product = 10 pJ ; maximum flip-flop toggle frequency = 125 MHz .

5.3.10 Floating and Unused Inputs

The floating input of TTL family devices behaves as if logic HIGH has been applied to the input. Such behaviour is explained from the input circuit of a TTL device. When the input is HIGH, the input emitter-base junction is reverse biased and the current that flows into the input is the reverse-biased diode leakage current. The input diode will be reverse biased even when the input terminal is left unconnected or floating, which implies that a floating input behaves as if there were logic HIGH applied to it.

As an initial thought, we may tend to believe that it should not make any difference if we leave the unused inputs of NAND and AND gates as floating, as logic HIGH like behaviour of the floating input makes no difference to the logical behaviour of the gate, as shown in Figs 5.24(a) and (b). In spite of this, it is strongly recommended that the unused inputs of AND and NAND gates be connected to a logic HIGH input [Fig. 5.24(c)] because floating input behaves as an antenna and may pick up stray noise and interference signals, thus causing the gate to function improperly. $1\text{ k}\Omega$ resistance is connected to protect the input from any current spikes caused by any spikes on the power supply line. More than one unused input (up to 50) can share the same $1\text{ k}\Omega$ resistance, if needed.

In the case of OR and NOR gates, unused inputs are connected to ground (logic LOW), as shown in Fig. 5.25(c), for obvious reasons. A floating input or an input tied to logic HIGH in this case produces a permanent logic HIGH (for an OR gate) and LOW (for a NOR gate) at the output as shown in Figs 5.25(a) and (b) respectively. An alternative solution is shown in Fig. 5.25(d), where the unused input has been tied to one of the used inputs. This solution works well for all gates, but one has to be conscious of the fact that the fan-out capability of the output driving the tied inputs is not exceeded.

If we recall the internal circuit schematics of AND and NAND gates, we will appreciate that, when more than one input is tied together, the input loading, that is, the current drawn by the tied inputs from the driving gate output, in the HIGH state is n times the loading of one input (Fig. 5.26); n is the number of inputs tied together. When the output is LOW, the input loading is the same as that of a single input. The reason for this is that, in the LOW input state, the current flowing out of the gate is determined by the resistance R_1 , as shown in Fig. 5.27. However, the same is not true in the case of

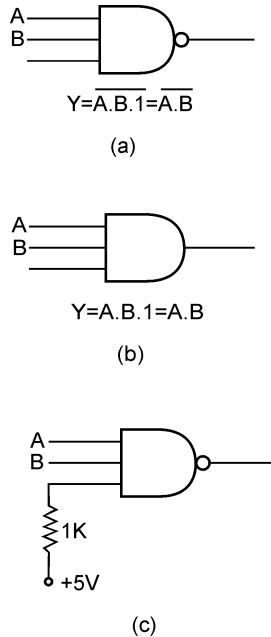


Figure 5.24 Handling unused inputs of AND and NAND gates.

OR and NOR gates, which do not use a multi-emitter input transistor and use separate input transistors instead, as shown in Fig. 5.28. In this case, the input loading is n times the loading of a single input for both HIGH and LOW states.

5.3.11 Current Transients and Power Supply Decoupling

TTL family devices are prone to occurrence of narrow-width current spikes on the power supply line. Current transients are produced when the totem-pole output stage of the device undergoes a transition from a logic LOW to a logic HIGH state. The problem becomes severe when in a digital circuit a large number of gates are likely to switch states at the same time. These current spikes produce voltage spikes due to any stray inductance present on the line. On account of the large rate of change in current in the current spike, even a small value of stray inductance produces voltage spikes large enough adversely to affect the circuit performance.

Figure 5.29 illustrates the phenomenon. When the output changes from LOW to HIGH, there is a small fraction of time when both the transistors are conducting because the pull-up transistor Q_3 has switched on and the pull-down transistor Q_4 has not yet come out of saturation. During this small fraction of time, there is an increase in current drawn from the supply; I_{CCL} experiences a positive spike before it settles down to a usually lower I_{CCH} . The presence of any stray capacitance C across the output owing to any stray wiring capacitance or capacitance loading of the circuit being fed also adds to the problem. The problem of voltage spikes on the power supply line is usually overcome by connecting small-value, low-inductance, high-frequency capacitors between V_{CC} terminal and ground. It is standard practice to use a 0.01 or 0.1 μF ceramic capacitor from V_{CC} to ground. This

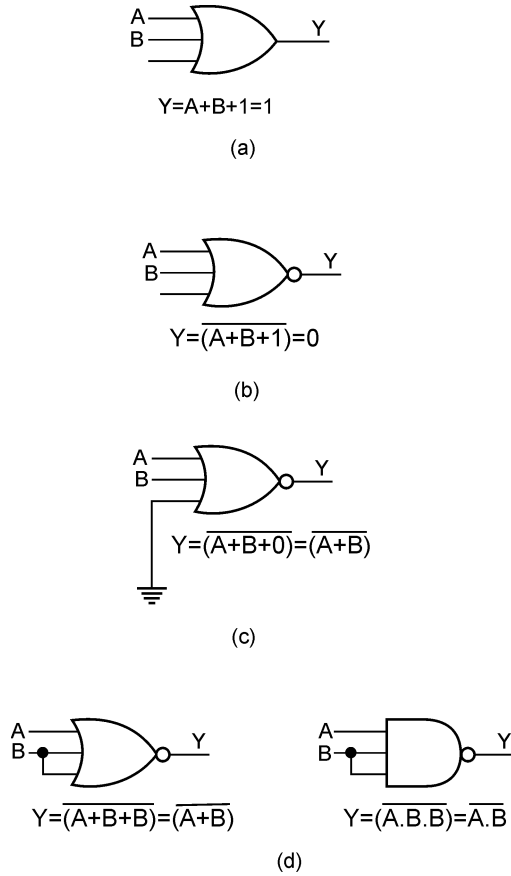


Figure 5.25 Handling unused inputs of OR and NOR gates.

capacitor is also known by the name of power supply decoupling capacitor, and it is recommended to use a separate capacitor for each IC. A decoupling capacitor is connected as close to the V_{CC} terminal as possible, and its leads are kept to a bare minimum to minimize lead inductance. In addition, a single relatively large-value capacitor in the range of 1–22 μF is also connected between V_{CC} and ground on each circuit card to take care of any low-frequency voltage fluctuations in the power supply line.

Example 5.5

Refer to Fig. 5.30. Determine the current being sourced by gate 1 when its output is HIGH and sunk by it when its output is LOW. All gates are from the standard TTL family, given that $I_{IH} = 40 \mu\text{A}$ and $I_{IL} = 1.6 \text{mA}$.

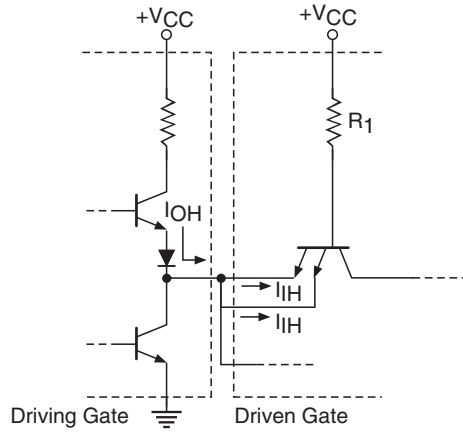


Figure 5.26 Input loading in the case of HIGH tied inputs of NAND and AND gates.

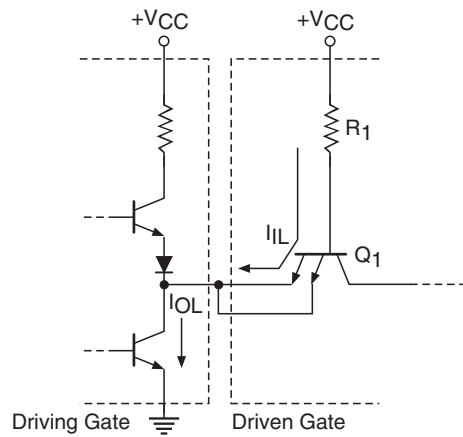


Figure 5.27 Input loading in the case of LOW tied inputs of NAND and AND gates.

Solution

- When the output is HIGH, the inputs of all gates draw current individually.
- Therefore, the input loading factor = equivalent of seven gate inputs = $7 \times 40 \mu\text{A} = 280 \mu\text{A}$.
- The current being sourced by the gate 1 output = $280 \mu\text{A}$.
- When the output is LOW, shorted inputs of AND and NAND gates offer a load equal to that of a single input owing to a multi-emitter transistor at the input of the gate. The inputs of OR and NOR gates draw current individually on account of the use of separate transistors at the input of the gate.
- Therefore, the input loading factor = equivalent of five gate inputs = $5 \times 1.6 = 8 \text{ mA}$.
- The current being sunk by the gate 1 output = 8 mA .

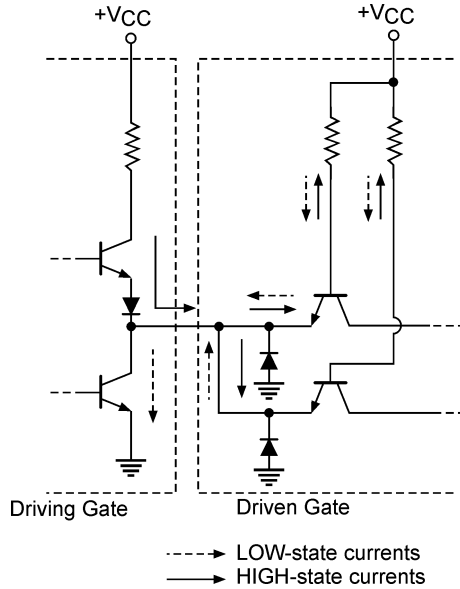


Figure 5.28 Input loading in the case of tied inputs of NOR and OR gates.

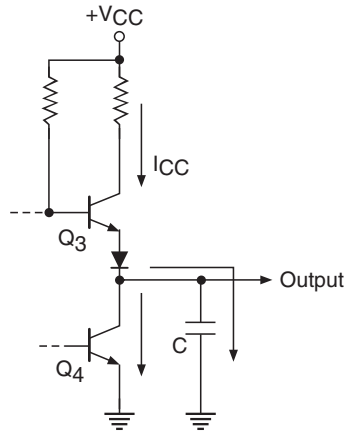


Figure 5.29 Current transients and power supply decoupling.

Example 5.6

Refer to the logic diagram of Fig. 5.31. Gate 1 and gate 4 belong to the standard TTL family, while gate 2 and gate 3 belong to the Schottky TTL family and the low-power Schottky TTL family respectively. Determine whether the fan-out capability of gate 1 is being exceeded. Relevant data for the three logic families are given in Table 5.1.

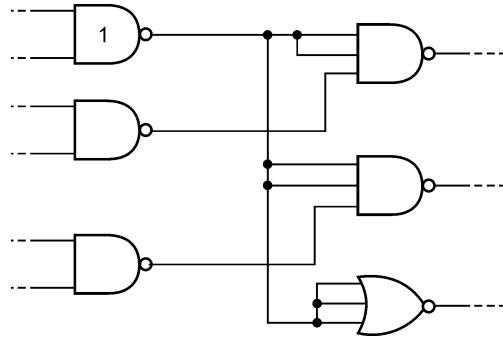


Figure 5.30 Example 5.5.

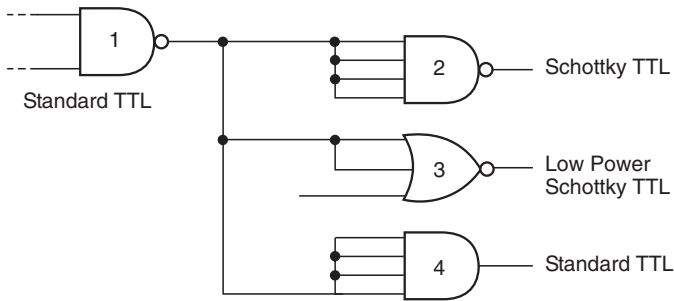


Figure 5.31 Example 5.6.

Table 5.1 Example 5.6

Logic family	$I_{IH}(\mu A)$	$I_{OH}(mA)$	$I_{IL}(mA)$	$I_{OL}(mA)$
Standard TTL	40	0.4	1.6	16
LS-TTL	20	0.4	0.4	8.0
S-TTL	50	1.0	2.0	20

Solution

- In the HIGH-state:

- the gate 1 output sourcing capability = $400 \mu A$;
- the gate 2 input requirement = $50 \times 4 = 200 \mu A$;
- the gate 3 input requirement = $20 \times 2 = 40 \mu A$;
- the gate 4 input requirement = $40 \times 4 = 160 \mu A$;
- the total input current requirement = $400 \mu A$;
- therefore, the fan-out is not exceeded in the HIGH state.

- In the LOW-state,
 - the gate 1 output sinking capability = 16 mA;
 - the gate 2 input sinking requirement = 2 mA;
 - the gate 3 input sinking requirement = $0.4 \times 2 = 0.8$ mA;
 - the gate 4 input sinking requirement = 1.6 mA;
 - the total input current requirement = 4.4 mA;
 - since the output of gate 1 has a current sinking capability of 16 mA, the fan-out capability is not exceeded in the LOW state either.

5.4 Emitter Coupled Logic (ECL)

The ECL family is the fastest logic family in the group of bipolar logic families. The characteristic features that give this logic family its high speed or short propagation delay are outlined as follows:

1. It is a nonsaturating logic. That is, the transistors in this logic are always operated in the active region of their output characteristics. They are never driven to either cut-off or saturation, which means that logic LOW and HIGH states correspond to different states of conduction of various bipolar transistors.
2. The logic swing, that is, the difference in the voltage levels corresponding to logic LOW and HIGH states, is kept small (typically 0.85 V), with the result that the output capacitance needs to be charged and discharged by a relatively much smaller voltage differential.
3. The circuit currents are relatively high and the output impedance is low, with the result that the output capacitance can be charged and discharged quickly.

5.4.1 Different Subfamilies

Different subfamilies of ECL logic include MECL-I, MECL-II, MECL-III, MECL 10K, MECL 10H and MECL 10E (ECLinPSTM and ECLinPS LiteTM).

5.4.1.1 MECL-I, MECL-II and MECL-III Series

MECL-I was the first monolithic emitter coupled logic family introduced by ON Semiconductor (formerly a division of Motorola SPS) in 1962. It was subsequently followed up by MECL-II in 1966. Both these logic families have become obsolete and have been replaced by MECL-III (also called the MC1600 series) introduced in 1968. Although, chronologically, MECL-III was introduced before the MECL-10K and MECL-10H families, it features higher speed than both of its successors. With a propagation delay of the order of 1 ns and a flip-flop toggle frequency of 500 MHz, MECL-III is used in high-performance, high-speed systems.

The basic characteristic parameters of MECL-III are as follows: gate propagation delay = 1 ns; output edge speed (indicative of the rise and fall time of output transition) = 1 ns; flip-flop toggle frequency = 500 MHz; power dissipation per gate = 50 mW; speed–power product = 60 pJ; input voltage = $0 - V_{EE}$ (V_{EE} is the negative supply voltage); negative power supply range (for $V_{CC} = 0$) = -5.1 V to -5.3 V; continuous output source current (max.) = 40 mA; surge output source current (max.) = 80 mA; operating temperature range = -30 °C to $+85$ °C.

5.4.1.2 MECL-10K Series

The MECL-10K family was introduced in 1971 to meet the requirements of more general-purpose high-speed applications. Another important feature of MECL-10K family devices is that they are compatible with MECL-III devices, which facilitates the use of devices of the two families in the same system. The increased propagation delay of 2 ns in the case of MECL-10K comes with the advantage of reduced power dissipation, which is less than half the power dissipation in MECL-III family devices.

The basic characteristic parameters of MECL-10K are as follows: gate propagation delay = 2 ns (10100-series) and 1.5 ns (10200-series); output edge speed = 3.5 ns (10100-series) and 2.5 ns (10200-series); flip-flop toggle frequency = 125 MHz (min.) in the 10100-series and 200 MHz (min.) in the 10200-series; power dissipation per gate = 25 mW; speed–power product = 50 pJ (10100-series) and 37 pJ (10200-series); input voltage = $0 - V_{EE}$ (V_{EE} is the negative supply voltage); negative power supply range (for $V_{CC} = 0$) = -4.68 to -5.72 V; continuous output source current (max.) = 50 mA; surge output source current (max.) = 100 mA; operating temperature range = -30 °C to $+85$ °C.

5.4.1.3 MECL-10H Series

The MECL-10H family, introduced in 1981, combines the high speed advantage of MECL-III with the lower power dissipation of MECL-10K. That is, it offers the speed of MECL-III with the power economy of MECL-10K. Backed by a propagation delay of 1 ns and a power dissipation of 25 mW per gate, MECL-10H offers one of the best speed–power product specifications in all available ECL subfamilies. Another important aspect of this family is that many of the MECL-10H devices are pin-out/functional replacements of MECL-10K series devices, which allows the users or the designers to enhance the performance of existing systems by increasing speed in critical timing areas.

The basic characteristic parameters of MECL-10H are as follows: gate propagation delay = 1 ns; output edge speed = 1 ns; flip-flop toggle frequency = 250 MHz (min.); power dissipation per gate = 25 mW; speed–power product = 25 pJ; input voltage = $0 - V_{EE}$ (V_{EE} is the negative supply voltage); negative power supply range (for $V_{CC} = 0$) = -4.94 to -5.46 V; continuous output source current (max.) = 50 mA; surge output source current (max.) = 100 mA; operating temperature range = 0 °C to $+75$ °C.

5.4.1.4 MECL-10E Series (ECLinPS™ and ECLinPSLite™)

The ECLinPS™ family, introduced in 1987, has a propagation delay of the order of 0.5 ns. ECLinPSLite™ is a recent addition to the ECL family. It offers a propagation delay of the order of 0.2 ns. The ECLPro™ family of devices is a rapidly growing line of high-performance ECL logic, offering a significant speed upgrade compared with the ECLinPSLite™ devices.

5.4.2 Logic Gate Implementation in ECL

OR/NOR is the fundamental logic gate of the ECL family. Figure 5.32 shows a typical internal schematic of an OR/NOR gate in the 10K-series MECL family. The circuit in essence comprises a differential amplifier input circuit with one side of the differential pair having multiple transistors depending upon the number of inputs to the gate, a voltage- and temperature-compensated bias network and emitter follower outputs. The internal schematic of the 10H-series gate is similar, except that the bias network is replaced with a voltage regulator circuit and the source resistor R_{EE} of the differential amplifier is replaced with a constant current source. Typical values of power supply voltages are

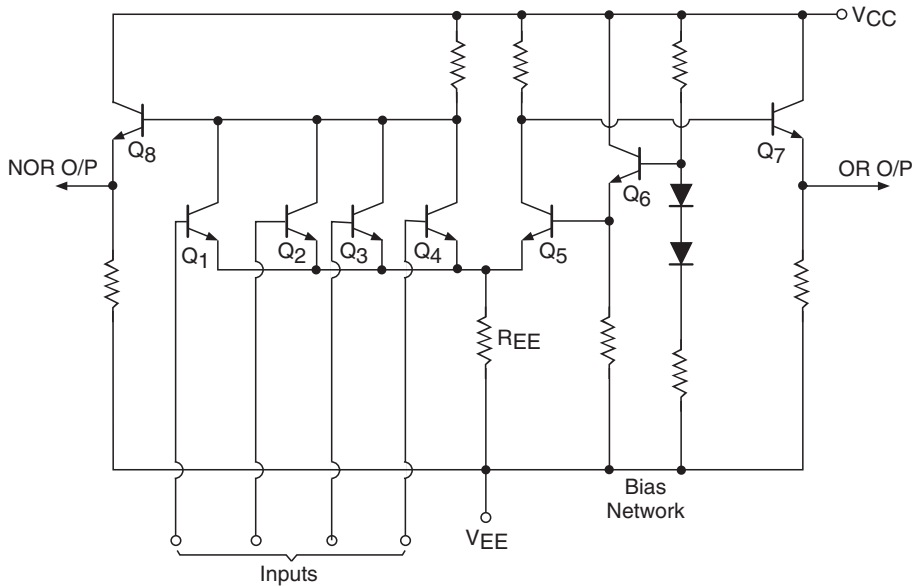


Figure 5.32 OR/NOR in ECL.

$V_{CC} = 0$ and $V_{EE} = -5.2$ V. The nominal logic levels are logic LOW = logic '0' = -1.75 V and logic HIGH = logic '1' = -0.9 V, assuming a positive logic system. The circuit functions as follows.

The bias network configured around transistor Q_6 produces a voltage of typically -1.29 V at its emitter terminal. This leads to a voltage of -2.09 V at the junction of all emitter terminals of various transistors in the differential amplifier, assuming 0.8 V to be the required forward-biased P-N junction voltage. Now, let us assume that all inputs are in a logic '0' state, that is, the voltage at the base terminals of various input transistors is -1.75 V. This means that the transistors Q_1 , Q_2 , Q_3 and Q_4 will remain in cut-off as their base-emitter junctions are not forward biased by the required voltage. This leads us to say that transistor Q_7 is conducting, producing a logic '0' output, and transistor Q_8 is in cut-off, producing a logic '1' output.

In the next step, let us see what happens if any one or all of the inputs are driven to logic '1' status, that is, a nominal voltage of -0.9 V is applied to the inputs. The base-emitter voltage differential of transistors Q_1 – Q_4 exceeds the required forward-biasing threshold, with the result that these transistors start conducting. This leads to a rise in voltage at the common-emitter terminal, which now becomes approximately -1.7 V as the common-emitter terminal is now 0.8 V more negative than the base-terminal voltage. With rise in the common-emitter terminal voltage, the base-emitter differential voltage of Q_5 becomes 0.31 V, driving Q_5 to cut-off. The Q_7 and Q_8 emitter terminals respectively go to logic '1' and logic '0'.

This explains how this basic schematic functions as an OR/NOR gate. We will note that the differential action of the switching transistors (where one section is ON while the other is OFF) leads to simultaneous availability of complementary signals at the output. Figure 5.33 shows the circuit symbol and switching characteristics of this basic ECL gate. It may be mentioned here that positive ECL (called PECL) devices operating at $+5$ V and ground are also available. When used in PECL mode, ECL devices must have their input/output DC parameters adjusted for proper operation. PECL DC parameters can be computed by adding ECL levels to the new V_{CC} .

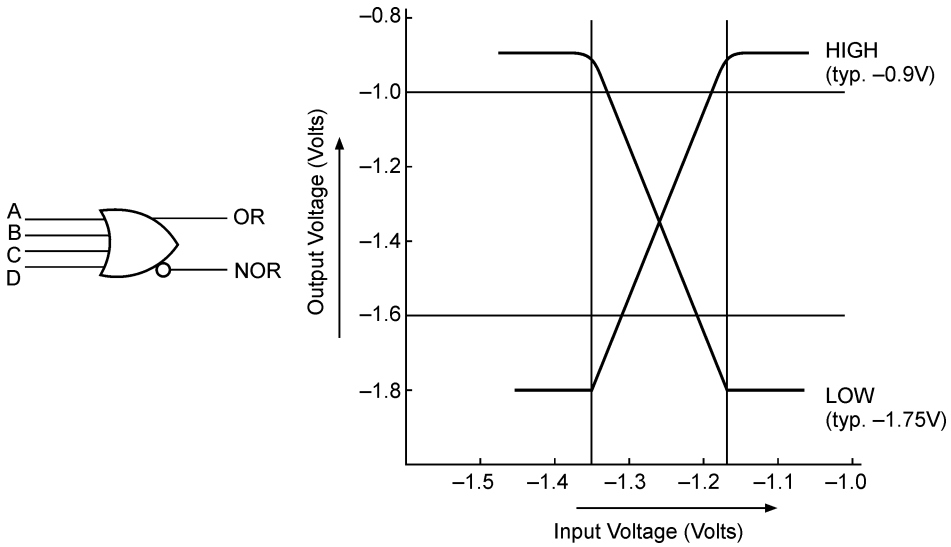


Figure 5.33 ECL input/output characteristics.

We will also note that voltage changes in ECL are small, largely governed by V_{BE} of the various conducting transistors. In fact, the magnitude of the currents flowing through various conducting transistors is of greater relevance to the operation of the ECL circuits. It is for this reason that emitter coupled logic is also sometimes called *current mode logic* (CML).

5.4.3 Salient Features of ECL

There are many features possessed by MECL family devices other than their high speed characteristics that make them attractive for many high-performance applications. The major ones are as follows:

1. ECL family devices produce the true and complementary output of the intended function simultaneously at the outputs without the use of any external inverters. This in turn reduces package count, reduces power requirements and also minimizes problems arising out of time delays that would be caused by external inverters.
2. The ECL gate structure inherently has high input impedance and low output impedance, which is very conducive to achieving large fan-out and drive capability.
3. ECL devices with open emitter outputs allow them to have transmission line drive capability. The outputs match any line impedance. Also, the absence of any pull-down resistors saves power.
4. ECL devices produce a near-constant current drain on the power supply, which simplifies power supply design.
5. On account of the differential amplifier design, ECL devices offer a wide performance flexibility, which allows ECL circuits to be used both as linear and as digital circuits.
6. Termination of unused inputs is easy. Resistors of approximately $50\text{ k}\Omega$ allow unused inputs to remain unconnected.

5.5 CMOS Logic Family

The CMOS (Complementary Metal Oxide Semiconductor) logic family uses both N-type and P-type MOSFETs (enhancement MOSFETs, to be more precise) to realize different logic functions. The two types of MOSFET are designed to have matching characteristics. That is, they exhibit identical characteristics in switch-OFF and switch-ON conditions. The main advantage of the CMOS logic family over bipolar logic families discussed so far lies in its extremely low power dissipation, which is near-zero in static conditions. In fact, CMOS devices draw power only when they are switching. This allows integration of a much larger number of CMOS gates on a chip than would have been possible with bipolar or NMOS (to be discussed later) technology. CMOS technology today is the dominant semiconductor technology used for making microprocessors, memory devices and application-specific integrated circuits (ASICs). The CMOS logic family, like TTL, has a large number of subfamilies. The prominent members of CMOS logic were listed in an earlier part of the chapter. The basic difference between different CMOS logic subfamilies such as 4000A, 4000B, 4000UB, 74C, 74HC, 74HCT, 74AC and 74ACT is in the fabrication process used and not in the design of the circuits employed to implement the intended logic function. We will firstly look at the circuit implementation of various logic functions in CMOS and then follow this up with a brief description of different subfamilies of CMOS logic.

5.5.1 Circuit Implementation of Logic Functions

In the following paragraphs, we will briefly describe the internal schematics of basic logic functions when implemented in CMOS logic. These include inverter, NAND, NOR, AND, OR, EX-OR, EX-NOR and AND-OR-INVERT functions.

5.5.1.1 CMOS Inverter

The inverter is the most fundamental building block of CMOS logic. It consists of a pair of N-channel and P-channel MOSFETs connected in cascade configuration as shown in Fig. 5.34. The circuit

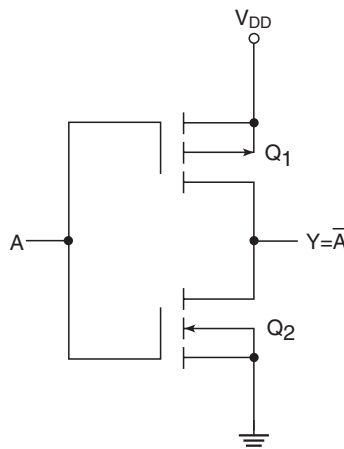


Figure 5.34 CMOS inverter.

functions as follows. When the input is in the HIGH state (logic '1'), P-channel MOSFET Q_1 is in the cut-off state while the N-channel MOSFET Q_2 is conducting. The conducting MOSFET provides a path from ground to output and the output is LOW (logic '0'). When the input is in the LOW state (logic '0'), Q_1 is in conduction while Q_2 is in cut-off. The conducting P-channel device provides a path for V_{DD} to appear at the output, so that the output is in HIGH or logic '1' state. A floating input could lead to conduction of both MOSFETs and a short-circuit condition. It should therefore be avoided. It is also evident from Fig. 5.34 that there is no conduction path between V_{DD} and ground in either of the input conditions, that is, when input is in logic '1' and '0' states. That is why there is practically zero power dissipation in static conditions. There is only dynamic power dissipation, which occurs during switching operations as the MOSFET gate capacitance is charged and discharged. The power dissipated is directly proportional to the switching frequency.

5.5.1.2 NAND Gate

Figure 5.35 shows the basic circuit implementation of a two-input NAND. As shown in the figure, two P-channel MOSFETs (Q_1 and Q_2) are connected in parallel between V_{DD} and the output terminal, and two N-channel MOSFETs (Q_3 and Q_4) are connected in series between ground and output terminal. The circuit operates as follows. For the output to be in a logic '0' state, it is essential that both the series-connected N-channel devices conduct and both the parallel-connected P-channel devices remain in the cut-off state. This is possible only when both the inputs are in a logic '1' state. This verifies one of the entries of the NAND gate truth table. When both the inputs are in a logic '0' state, both the N-channel devices are nonconducting and both the P-channel devices are conducting, which produces a logic '1' at the output. This verifies another entry of the NAND truth table. For the remaining two input combinations, either of the two N-channel devices will be nonconducting and either of the two parallel-connected P-channel devices will be conducting. We have either Q_3 OFF and Q_2 ON or Q_4 OFF and Q_1 ON. The output in both cases is a logic '1', which verifies the remaining entries of the truth table.

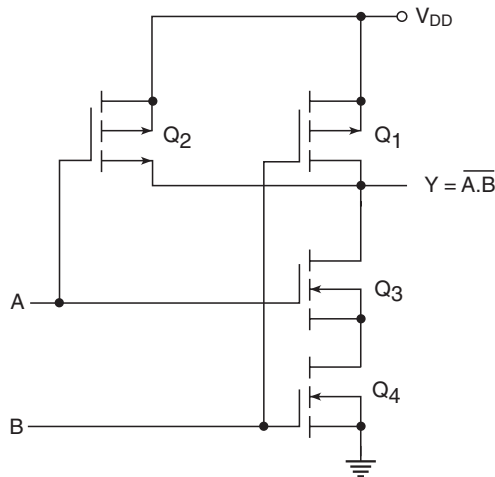


Figure 5.35 CMOS NAND.

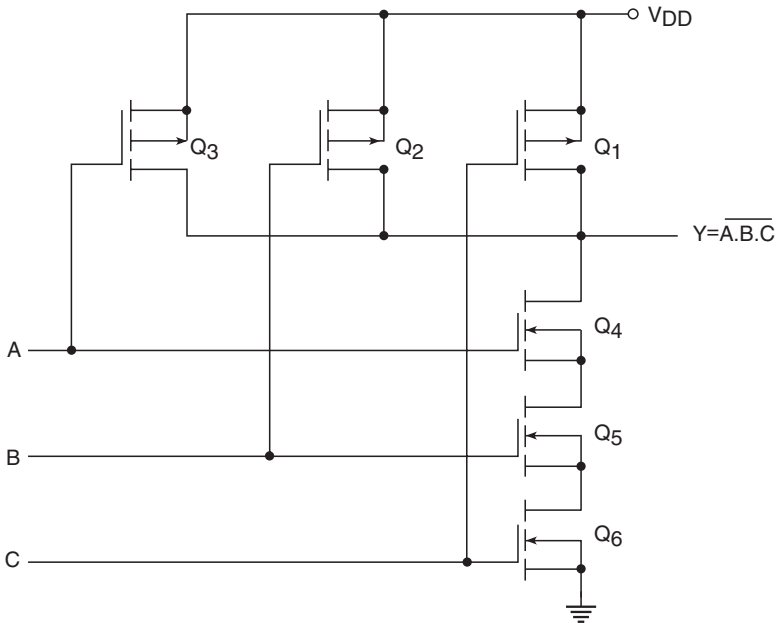


Figure 5.36 Three-input NAND in CMOS.

From the circuit schematic of Fig. 5.35 we can visualize that under no possible input combination of logic states is there a direct conduction path between V_{DD} and ground. This further confirms that there is near-zero power dissipation in CMOS gates under static conditions. Figure 5.36 shows how the circuit of Fig. 5.35 can be extended to build a three-input NAND gate. Operation of this circuit can be explained on similar lines. It may be mentioned here that series connection of MOSFETs adds to the propagation delay, which is greater in the case of P-channel devices than it is in the case of N-channel devices. As a result, the concept of extending the number of inputs as shown in Fig. 5.36 is usually limited to four inputs in the case of NAND and to three inputs in the case of NOR. The number is one less in the case of NOR because it uses series-connected P-channel devices. NAND and NOR gates with larger inputs are realized as a combination of simpler gates.

5.5.1.3 NOR Gate

Figure 5.37 shows the basic circuit implementation of a two-input NOR. As shown in the figure, two P-channel MOSFETs (Q_1 and Q_2) are connected in series between V_{DD} and the output terminal, and two N-channel MOSFETs (Q_3 and Q_4) are connected in parallel between ground and output terminal. The circuit operates as follows. For the output to be in a logic '1' state, it is essential that both the series-connected P-channel devices conduct and both the parallel-connected N-channel devices remain in the cut-off state. This is possible only when both the inputs are in a logic '0' state. This verifies one of the entries of the NOR gate truth table. When both the inputs are in a logic '1' state, both the N-channel devices are conducting and both the P-channel devices are nonconducting, which produces a logic '0' at the output. This verifies another entry of the NOR truth table. For the remaining two

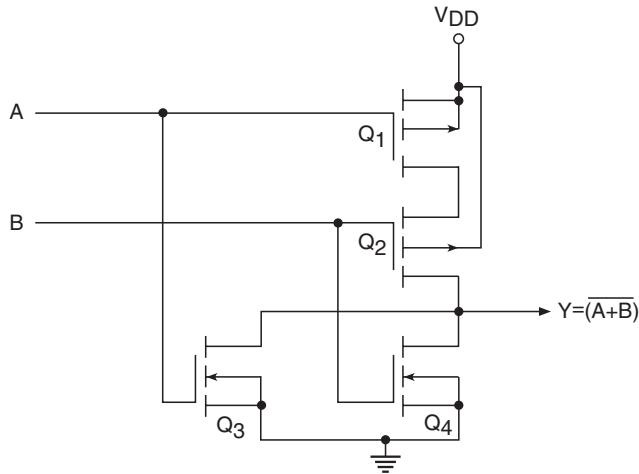


Figure 5.37 Two-input NOR in CMOS.

input combinations, either of the two parallel N-channel devices will be conducting and either of the two series-connected P-channel devices will be nonconducting. We have either Q_1 OFF and Q_3 ON or Q_2 OFF and Q_4 ON. The output in both cases is logic '0', which verifies the remaining entries of the truth table.

Figure 5.38 shows how the circuit of Fig. 5.37 can be extended to build a three-input NOR gate. The operation of this circuit can be explained on similar lines. As already explained, NOR gates with more than three inputs are usually realized as a combination of simpler gates.

5.5.1.4 AND Gate

An AND gate is nothing but a NAND gate followed by an inverter. Figure 5.39 shows the internal schematic of a two-input AND in CMOS. A buffered AND gate is fabricated by using a NOR gate schematic with inverters at both of its inputs and its output feeding two series-connected inverters.

5.5.1.5 OR Gate

An OR gate is nothing but a NOR gate followed by an inverter. Figure 5.40 shows the internal schematic of a two-input OR in CMOS. A buffered OR gate is fabricated by using a NAND gate schematic with inverters at both of its inputs and its output feeding two series-connected inverters.

5.5.1.6 EXCLUSIVE-OR Gate

An EXCLUSIVE-OR gate is implemented using the logic diagram of Fig. 5.41(a). As is evident from the figure, the output of this logic arrangement can be expressed by

$$\overline{(\overline{A+B}) + A.B} = \overline{(\overline{A.B} + A.B)} = \text{EX - OR function} \quad (5.1)$$

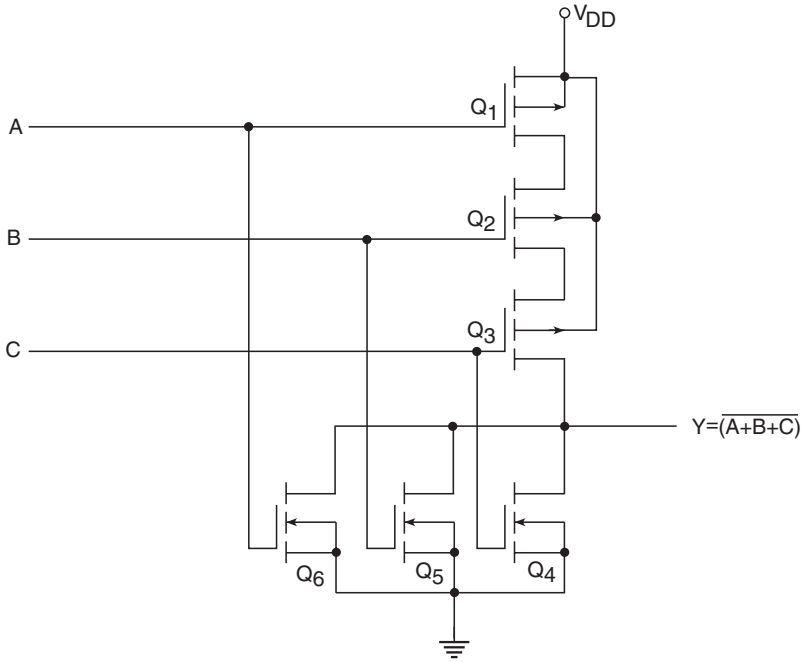


Figure 5.38 Three-input NOR.

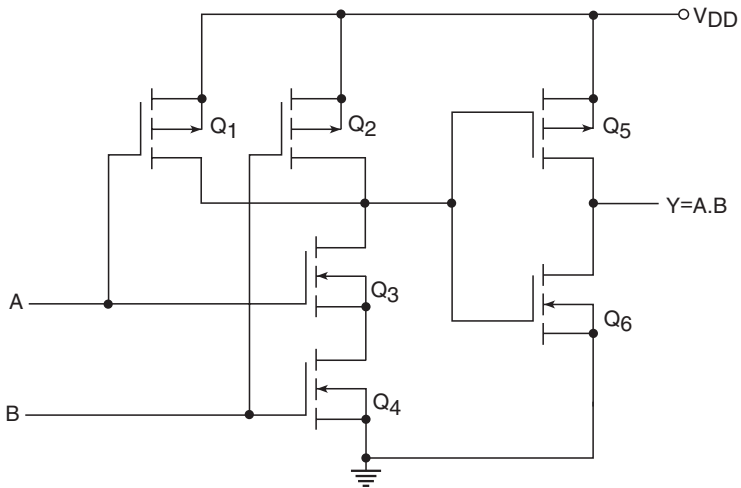


Figure 5.39 Two-input AND in CMOS.

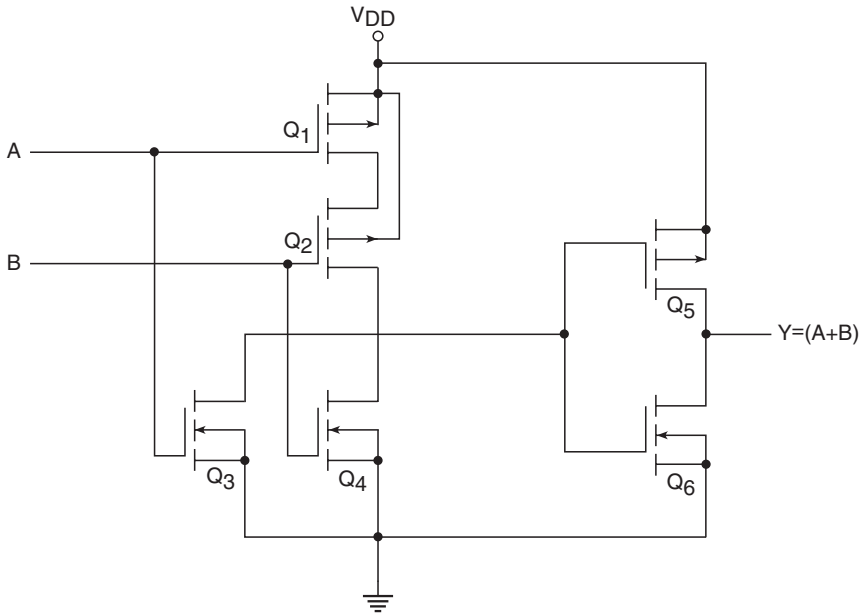


Figure 5.40 Two-input OR in CMOS.

Figure 5.41(b) shows the internal schematic of a two-input EX-OR gate. MOSFETs Q_1 – Q_4 constitute the NOR gate. MOSFETS Q_5 and Q_6 simulate ANDing of A and B , and MOSFET Q_7 provides ORing of the NOR output with ANDed output. Since MOSFETS Q_8 – Q_{10} make up the complement of the arrangement of MOSFETS Q_5 – Q_7 , the final output is inverted. Thus, the schematic of Fig. 5.41(b) implements the logic arrangement of Fig. 5.41(a) and hence a two-input EX-OR gate.

5.5.1.7 EXCLUSIVE-NOR Gate

An EXCLUSIVE-NOR gate is implemented using the logic diagram of Fig. 5.42(a). As is evident from the figure, the output of this logic arrangement can be expressed by

$$\overline{[(A \cdot B) \cdot (A + B)]} = \overline{[(\overline{A + B}) \cdot (A + B)]} = \text{EX - NOR function} \quad (5.2)$$

Figure 5.42(b) shows the internal schematic of a two-input EX-NOR gate. MOSFETs Q_1 – Q_4 constitute the NAND gate. MOSFETS Q_5 and Q_6 simulate ORing of A and B , and MOSFET Q_7 provides ANDing of the NAND output with Ored output. Since MOSFETS Q_8 – Q_{10} make up the complement of the arrangement of MOSFETS Q_5 – Q_7 , the final output is inverted. Thus, the schematic of Fig. 5.42(b) implements the logic arrangement of Fig. 5.42(a) and hence a two-input EX-NOR gate.

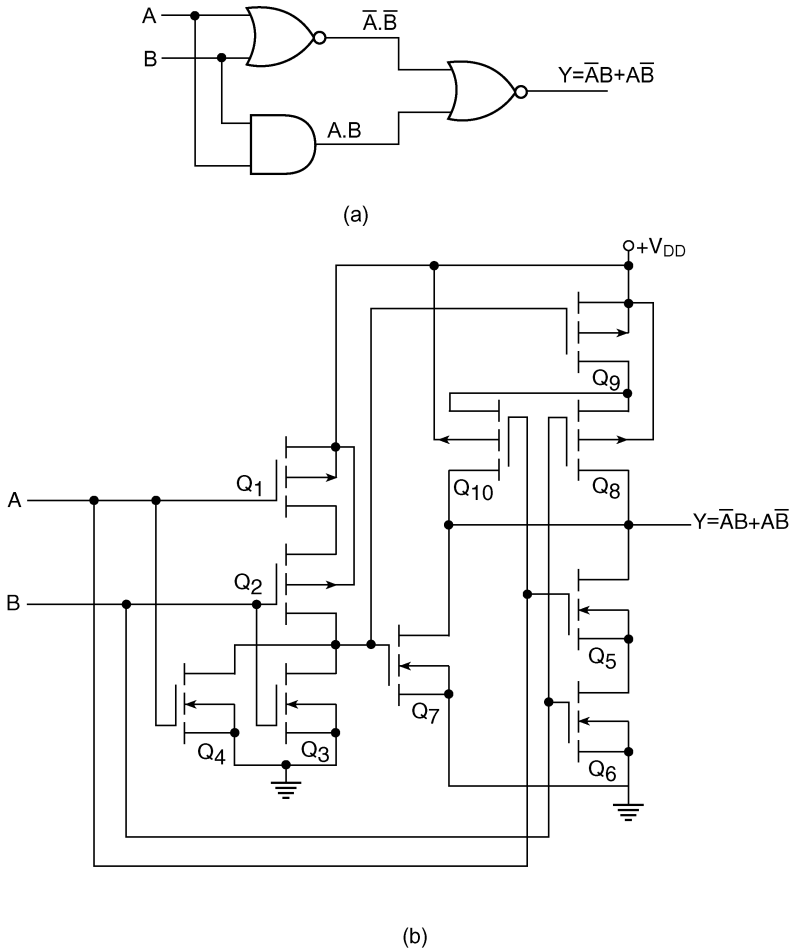


Figure 5.41 Two-input EX-OR in CMOS.

5.5.1.8 AND-OR-INVERT and OR-AND-INVERT Gates

Figure 5.43 shows the internal schematic of a typical two-wide, two-input AND-OR-INVERT gate. The output of this gate can be logically expressed by the Boolean equation

$$Y = \overline{(A.B + C.D)} \tag{5.3}$$

From the above expression, we can say that the output should be in a logic ‘0’ state for the following input conditions:

1. When either $A.B = \text{logic '1'}$ or $C.D = \text{logic '1'}$
2. When both $A.B$ and $C.D$ equal logic ‘1’.

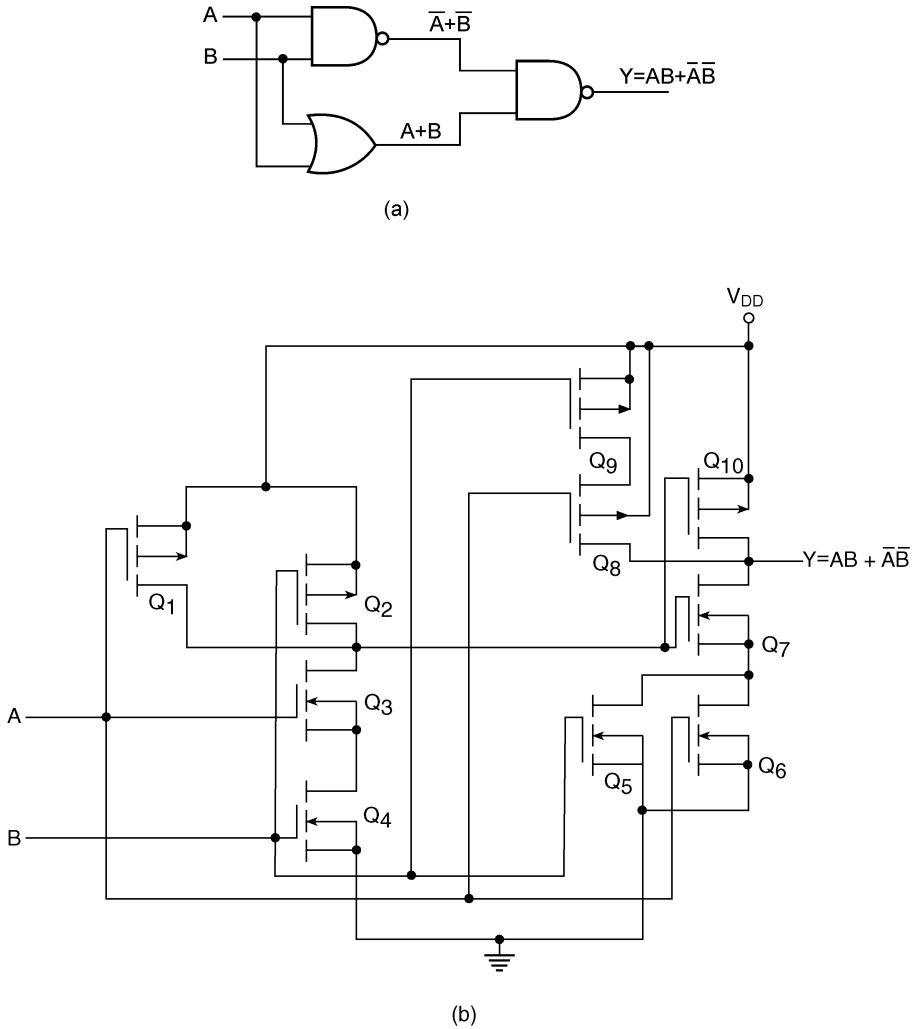


Figure 5.42 Two-input EX-NOR in CMOS.

For both these conditions there is a conduction path available from ground to output, which verifies that the circuit satisfies the logic expression. Also, according to the logic expression for the AND-OR-INVERT gate, the output should be in a logic '1' state when both $A.B$ and $C.D$ equal logic '0'. This implies that:

1. Either A or B or both are in a logic '0' state.
2. Either C or D or both are in a logic '0' state.

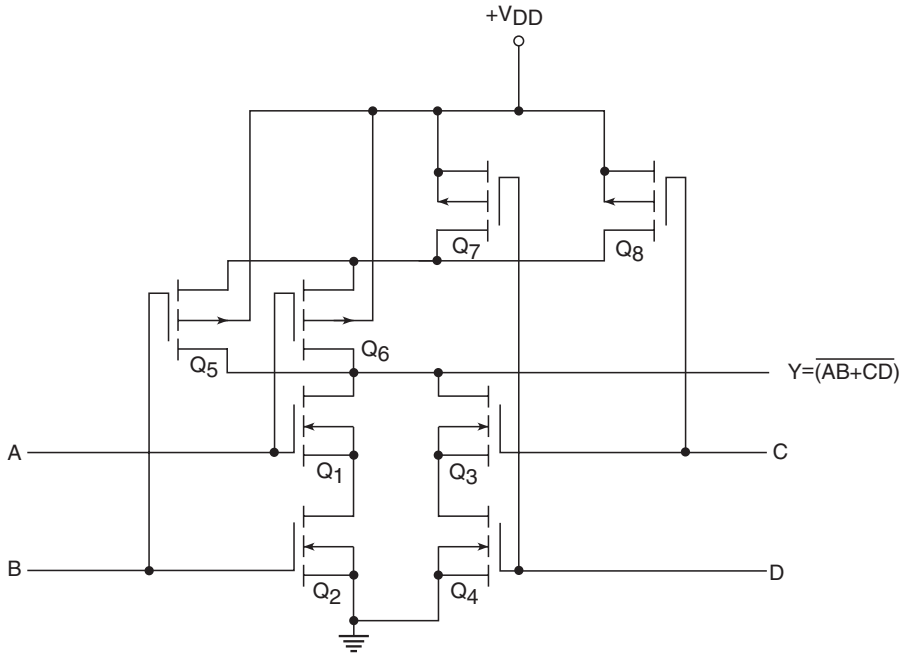


Figure 5.43 Two-wide, two-input AND-OR-INVERT gate in CMOS.

If these conditions are applied to the circuit of Fig. 5.43, we find that the ground will remain disconnected from the output and also that there is always a path from V_{DD} to output. This leads to a logic '1' at the output. Thus, we have proved that the given circuit implements the intended logic expression for the AND-OR-INVERT gate.

The OR-AND-INVERT gate can also be implemented in the same way. Figure 5.44 shows a typical internal schematic of a two-wide, two-input OR-AND-INVERT gate. The output of this gate can be expressed by the Boolean equation

$$Y = \overline{(A + B).(C + D)} \tag{5.4}$$

It is very simple to draw the internal schematic of an AND-OR-INVERT or OR-AND-INVERT gate. The circuit has two parts, that is, the N-channel MOSFET part of the circuit and the P-channel part of the circuit. Let us see, for instance, how Boolean equation (5.4) relates to the circuit of Fig. 5.44. The fact that we need $(A \text{ OR } B) \text{ AND } (C \text{ OR } D)$ explains why the N-channel MOSFETs representing A and B inputs are in parallel and also why the N-channel MOSFETs representing C and D are also in parallel. The two parallel arrangements are then connected in series to achieve an ANDing operation. The complementary P-channel MOSFET section achieves inversion. Note that the P-channel section is the complement of the N-channel section with N-channel MOSFETs replaced by P-channel MOSFETs and parallel connection replaced by series connection, and vice versa. The operation of an AND-OR-INVERT gate can be explained on similar lines to the case of an OR-AND-INVERT gate. Expansion of both AND-OR-INVERT and OR-AND-INVERT gates should be obvious, ensuring that we do not have more than three devices in series.

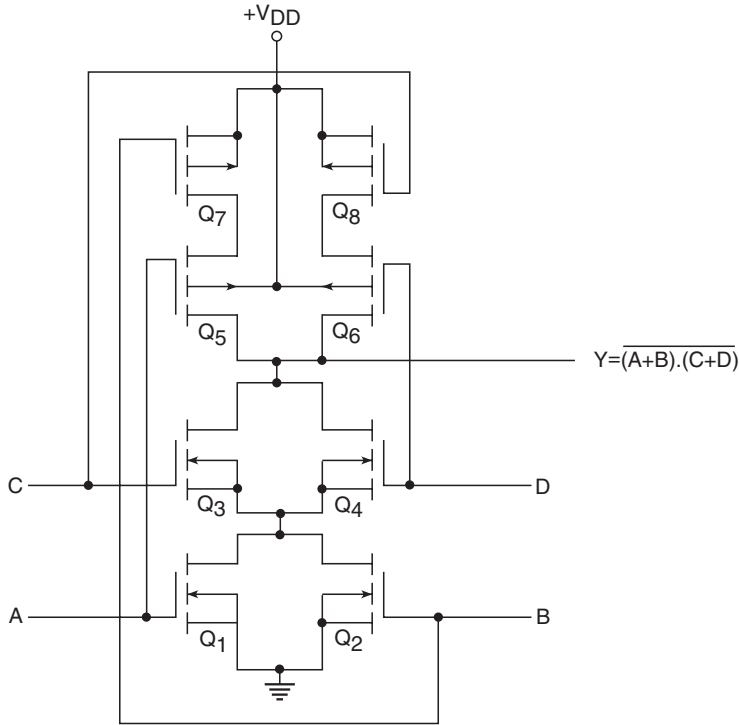


Figure 5.44 Two-wide, two-input OR-AND-INVERT gate.

5.5.1.9 Transmission Gate

The transmission gate, also called the *bilateral switch*, is exclusive to CMOS logic and does not have a counterpart in the TTL and ECL families. It is essentially a single-pole, single-throw (SPST) switch. The opening and closing operations can be controlled by externally applied logic levels. Figure 5.45(a) shows the circuit symbol. If a logic '0' at the control input corresponds to an open switch, then a logic '1' corresponds to a closed switch, and vice versa. The internal schematic of a transmission gate is nothing but a parallel connection of an N-channel MOSFET and a P-channel MOSFET with the control input applied to the gates, as shown in Fig. 5.45(b). Control inputs to the gate terminals of two MOSFETs are the complement of each other. This is ensured by an inbuilt inverter.

When the control input is HIGH (logic '1'), both devices are conducting and the switch is closed. When the control input is LOW (logic '0'), both devices are open and therefore the switch is open. It may be mentioned here that there is no discrimination between input and output terminals. Either of the two can be treated as the input terminal for the purpose of applying input. This is made possible by the symmetry of the two MOSFETs.

It may also be mentioned here that the ON-resistance of a conducting MOSFET depends upon drain and source voltages. In the case of an N-channel MOSFET, if the source voltage is close to V_{DD} , there is an increase in ON-resistance, leading to an increased voltage drop across the switch. A similar phenomenon is observed when the source voltage of a P-channel MOSFET is close to

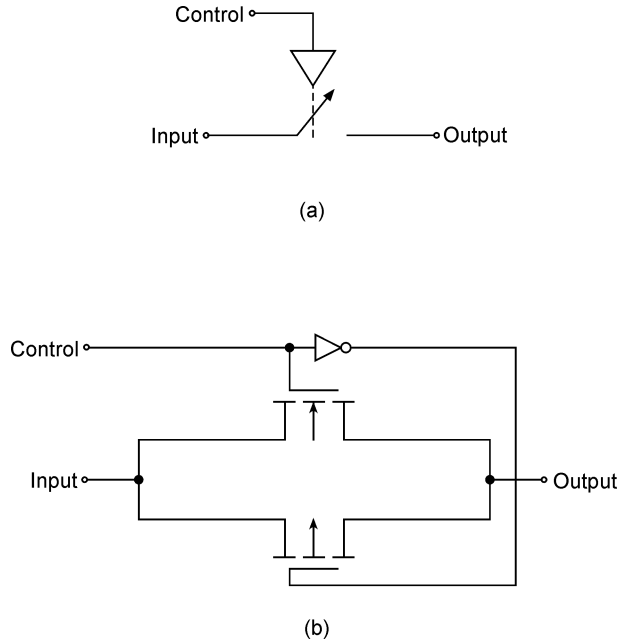


Figure 5.45 Transmission gate.

ground. Such behaviour causes no problem in static CMOS logic gates, where source terminals of all N-channel MOSFETs are connected to ground and source terminals of all P-channel MOSFETs are connected to V_{DD} . This would cause a problem if a single N-channel or P-channel device were used as a switch. Such a problem is overcome with the use of parallel connection of N-channel and P-channel devices. Transmission gate devices are available in 4000-series as well as 74HC series of CMOS logic.

5.5.1.10 CMOS with Open Drain Outputs

The outputs of conventional CMOS gates should never be shorted together, as illustrated by the case of two inverters shorted at the output terminals (Fig. 5.46). If the input conditions are such that the output of one inverter is HIGH and that of the other is LOW, the output circuit is then like a voltage divider network with two identical resistors equal to the ON-resistance of a conducting MOSFET. The output is then approximately equal to $V_{DD}/2$, which lies in the indeterminate range and is therefore unacceptable. Also, an arrangement like this draws excessive current and could lead to device damage.

This problem does not exist in CMOS gates with open drain outputs. Such a device is the counterpart to gates with open collector outputs in the TTL family. The output stage of a CMOS gate with an open drain output is a single N-channel MOSFET with an open drain terminal, and there is no P-channel MOSFET. The open drain terminal needs to be connected to V_{DD} through an external pull-up resistor. Figure 5.47 shows the internal schematic of a CMOS inverter with an open drain output. The pull-up resistor shown in the circuit is external to the device.

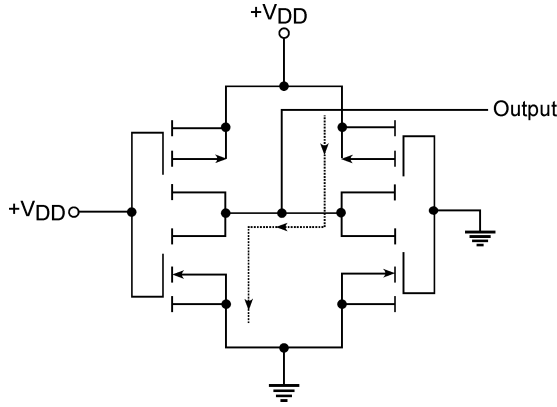


Figure 5.46 CMOS inverters with shorted outputs.

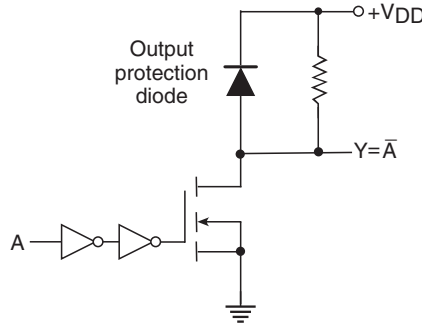


Figure 5.47 CMOS inverter with an open drain output.

5.5.1.11 CMOS with Tristate Outputs

Like tristate TTL, CMOS devices are also available with tristate outputs. The operation of tristate CMOS devices is similar to that of tristate TTL. That is, when the device is enabled it performs its intended logic function, and when it is disabled its output goes to a high-impedance state. In the high-impedance state, both N-channel and P-channel MOSFETs are driven to an OFF-state. Figure 5.48 shows the internal schematic of a tristate buffer with active LOW ENABLE input. The circuit shown is that of one of the buffers in CMOS hex buffer type CD4503B. The outputs of tristate CMOS devices can be connected together in a bus arrangement, like tristate TTL devices with the same condition that only one device is enabled at a time.

5.5.1.12 Floating or Unused Inputs

Unused inputs of CMOS devices should never be left floating or unconnected. A floating input is highly susceptible to picking up noise and accumulating static charge. This can often lead to simultaneous

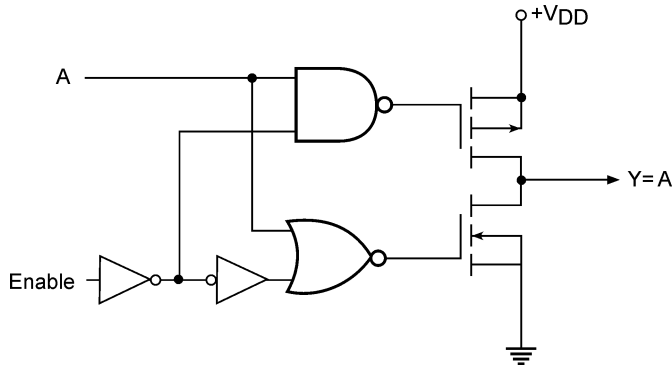


Figure 5.48 Tristate buffer in CMOS.

conduction of P-channel and N-channel devices on the chip, which causes increased power dissipation and overheating. Unused inputs of CMOS gates should either be connected to ground or V_{DD} or shorted to another input. The same is applicable to the inputs of all those gates that are not in use. For example, we may be using only two of the four gates available on an IC having four gates. The inputs of the remaining two gates should be tied to either ground or V_{DD} .

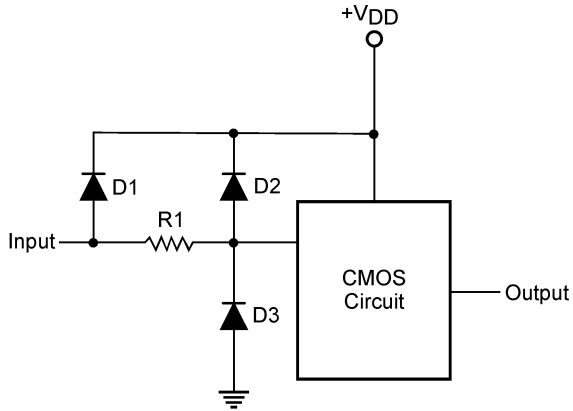
5.5.1.13 Input Protection

Owing to the high input impedance of CMOS devices, they are highly susceptible to static charge build-up. As a result of this, voltage developed across the input terminals could become sufficiently high to cause dielectric breakdown of the gate oxide layer. In order to protect the devices from this static charge build-up and its damaging consequences, the inputs of CMOS devices are protected by using a suitable resistor–diode network, as shown in Fig. 5.49(a). The protection circuit shown is typically used in metal-gate MOSFETs such as those used in 4000-series CMOS devices. Diode D_2 limits the positive voltage surges to $V_{DD} + 0.7$ V, while diode D_3 clamps the negative voltage surges to -0.7 V. Resistor R_1 limits the static discharge current amplitude and thus prevents any damagingly large voltage from being directly applied to the input terminals. Diode D_1 does not contribute to input protection. It is a distributed P–N junction present owing to the diffusion process used for fabrication of resistor R_1 . The protection diodes remain reverse biased for the normal input voltage range of 0 to V_{DD} , and therefore do not affect normal operation.

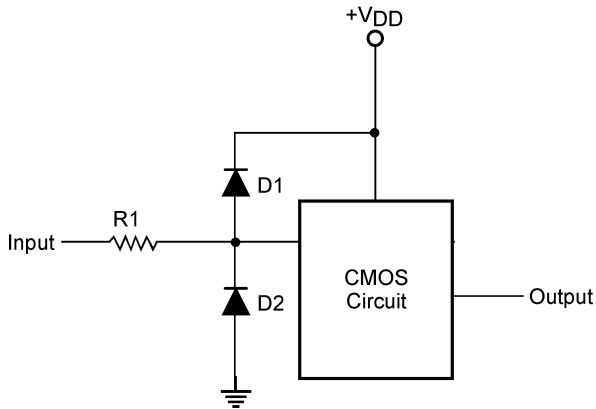
Figure 5.49(b) shows a typical input protection circuit used for silicon-gate MOSFETs used in 74C, 74HC, etc., series CMOS devices. A distributed P–N junction is absent owing to R_1 being a polysilicon resistor. Diodes D_1 and D_2 do the same job as diodes D_2 and D_3 in the case of metal-gate devices. Diode D_2 is usually fabricated in the form of a bipolar transistor with its collector and base terminals shorted.

5.5.1.14 Latch-up Condition

This is an undesired condition that can occur in CMOS devices owing to the existence of parasitic bipolar transistors (NPN and PNP) embedded in the substrate. While N-channel MOSFETs lead to the



(a)



(b)

Figure 5.49 (a) Input protection circuit-metal-gate devices and (b) input protection circuit-silicon-gate devices.

presence of NPN transistors, P-channel MOSFETs are responsible for the existence of PNP transistors. If we look into the arrangement of different semiconductor regions in the most basic CMOS building block, that is, the inverter, we will find that these parasitic NPN and PNP transistors find themselves interconnected in a back-to-back arrangement, with the collector of one transistor connected to the base of the other, and vice versa. Two such pairs of transistors connected in series exist between V_{DD} and ground in the case of an inverter, as shown in Fig. 5.50. If for some reason these parasitic elements are triggered into conduction, on account of inherent positive feedback they get into a latch-up condition and remain in conduction permanently. This can lead to the flow of large current and subsequently to destruction of the device. A latch-up condition can be triggered by high voltage spikes and ringing

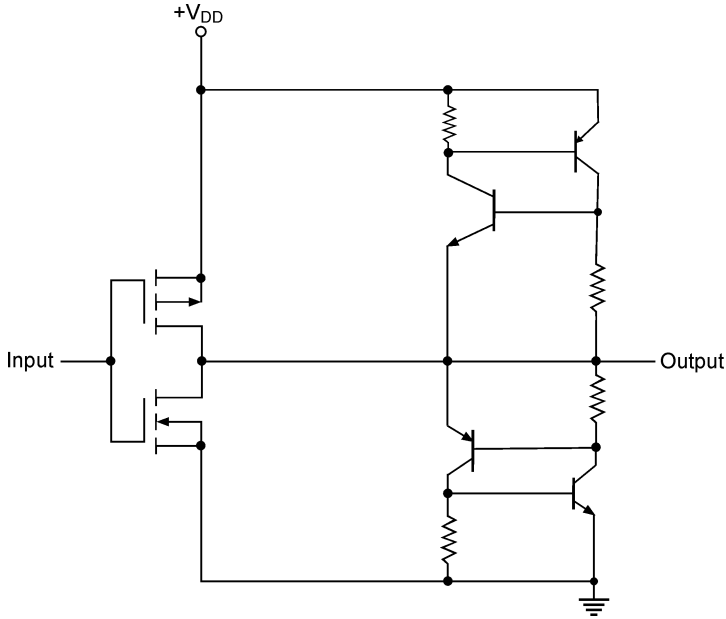


Figure 5.50 CMOS inverter with parasitic elements.

present at the device inputs and outputs. The device can also be prone to latch-up if its maximum ratings are exceeded. Modern CMOS devices use improved fabrication techniques so as to minimize factors that can cause this undesired effect. The use of external clamping diodes at inputs and outputs, proper termination of unused inputs and regulated power supply with a current-limiting feature also helps in minimizing the chances of occurrence of the latch-up condition and in minimizing its effects if it occurs.

5.5.2 CMOS Subfamilies

In the following paragraphs, we will briefly describe various subfamilies of CMOS logic, including subfamilies of the 4000 series and those of TTL pin-compatible 74C series.

5.5.2.1 4000-series

The 4000A-series CMOS ICs, introduced by RCA, were the first to arrive on the scene from the CMOS logic family. The 4000A CMOS subfamily is obsolete now and has been replaced by 4000B and 4000UB subfamilies. We will therefore not discuss it in detail. The 4000B series is a high-voltage version of the 4000A series, and also all the outputs in this series are buffered. The 4000UB series is also a high-voltage version of the 4000A series, but here the outputs are not buffered. A buffered CMOS device is one that has constant output impedance irrespective of the logic status of the inputs. If we recall the internal schematics of the basic CMOS logic gates described in the previous pages, we will see that, with the exception of the inverter, the output impedance of other gates depends upon the

logic status of the inputs. This variation in output impedance occurs owing to the varying combination of MOSFETs that conduct for a given input combination. All buffered devices are designated by the suffix 'B' and referred to as the 4000B series. The 4000-series devices that meet 4000B series specifications except for the V_{IL} and V_{IH} specifications and that the outputs are not buffered are called unbuffered devices and are said to belong to the 4000UB series.

Figures 5.51 and 5.52 show a comparison between the internal schematics of a buffered two-input NOR (Fig. 5.51) and an unbuffered two-input NOR (Fig. 5.52). A buffered gate has been implemented by using inverters at the inputs to a two-input NAND whose output feeds another inverter. This is the typical arrangement followed by various manufacturers, as the inverters at the input enhance noise immunity. Another possible arrangement would be a two-input NOR whose output feeds two series-connected inverters.

Variation in the output impedance of unbuffered gates is larger for gates with a larger number of inputs. For example, unbuffered gates have an output impedance of 200–400 Ω in the case of two-input gates, 133–400 Ω for three-input gates and 100–400 Ω for gates with four inputs. Buffered gates have an output impedance of 400 Ω . Since they have the same maximum output impedance, their minimum I_{OL} and I_{OH} specifications are the same.

Characteristic features of 4000B and 4000UB CMOS devices are as follows: V_{IH} (buffered devices) = 3.5 V (for $V_{DD} = 5$ V), 7.0 V (for $V_{DD} = 10$ V) and 11.0 V (for $V_{DD} = 15$ V); V_{IH} (unbuffered devices) = 4.0 V (for $V_{DD} = 5$ V), 8.0 V (for $V_{DD} = 10$ V) and 12.5 V (for $V_{DD} = 15$ V); $I_{IH} = 1.0 \mu\text{A}$; $I_{IL} = 1.0 \mu\text{A}$; $I_{OH} = 0.2$ mA (for $V_{DD} = 5$ V), 0.5 mA (for $V_{DD} = 10$ V) and 1.4 mA (for $V_{DD} = 15$ V); $I_{OL} = 0.52$ mA (for $V_{DD} = 5$ V), 1.3 mA (for $V_{DD} = 10$ V) and 3.6 mA (for $V_{DD} = 15$ V); V_{IL} (buffered devices) = 1.5 V (for $V_{DD} = 5$ V), 3.0 V (for $V_{DD} = 10$ V) and 4.0 V (for $V_{DD} = 15$ V); V_{IL} (unbuffered devices) = 1.0 V (for $V_{DD} = 5$ V), 2.0 V (for $V_{DD} = 10$ V) and 2.5 V (for $V_{DD} = 15$ V); $V_{OH} = 4.95$ V

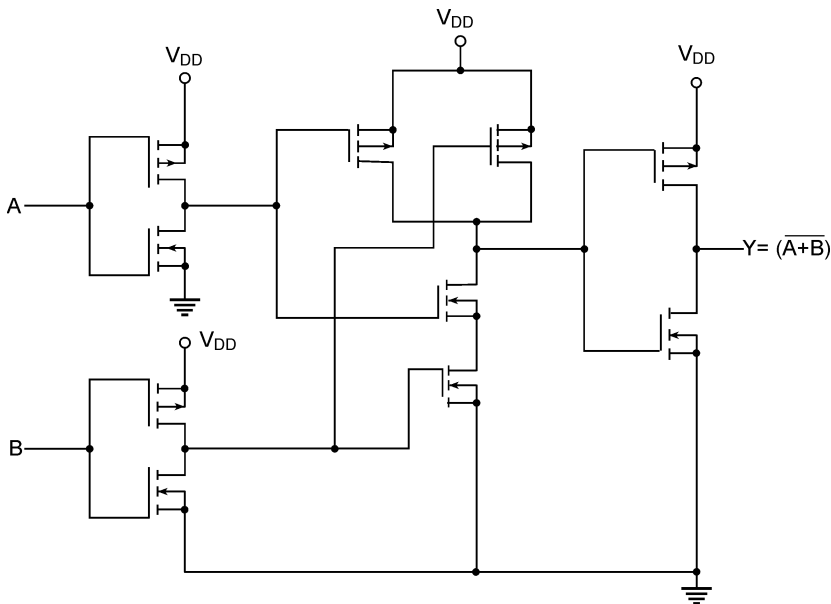


Figure 5.51 Buffered two-input NOR.

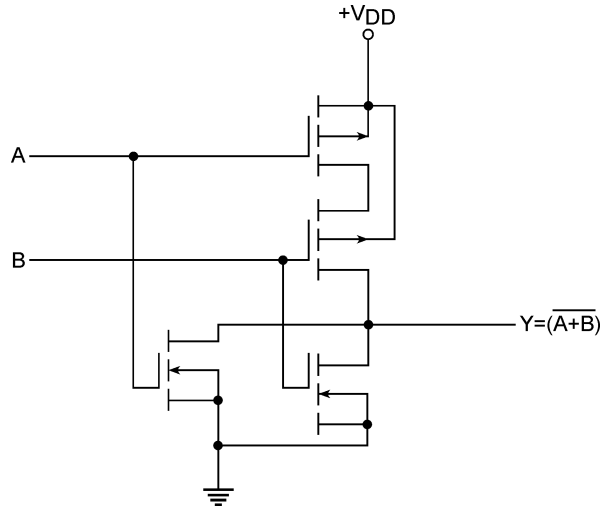


Figure 5.52 Unbuffered two-input NOR.

(for $V_{DD} = 5\text{ V}$), 9.95 V (for $V_{DD} = 10\text{ V}$) and 14.95 V (for $V_{DD} = 15\text{ V}$); $V_{OL} = 0.05\text{ V}$; $V_{DD} = 3\text{--}15\text{ V}$; propagation delay (buffered devices) = 150 ns (for $V_{DD} = 5\text{ V}$), 65 ns (for $V_{DD} = 10\text{ V}$) and 50 ns (for $V_{DD} = 15\text{ V}$); propagation delay (unbuffered devices) = 60 ns (for $V_{DD} = 5\text{ V}$), 30 ns (for $V_{DD} = 10\text{ V}$) and 25 ns (for $V_{DD} = 15\text{ V}$); noise margin (buffered devices) = 1.0 V (for $V_{DD} = 5\text{ V}$), 2.0 V (for $V_{DD} = 10\text{ V}$) and 2.5 V (for $V_{DD} = 15\text{ V}$); noise margin (unbuffered devices) = 0.5 V (for $V_{DD} = 5\text{ V}$), 1.0 V (for $V_{DD} = 10\text{ V}$) and 1.5 V (for $V_{DD} = 15\text{ V}$); output transition time (for $V_{DD} = 5\text{ V}$ and $C_L = 50\text{ pF}$) = 100 ns (buffered devices) and 50–100 ns (for unbuffered devices); power dissipation per gate (for $f = 100\text{ kHz}$) = 0.1 mW; speed–power product (for $f = 100\text{ kHz}$) = 5 pJ; maximum flip-flop toggle rate = 12 MHz.

5.5.2.2 74C Series

The 74C CMOS subfamily offers pin-to-pin replacement of the 74-series TTL logic functions. For instance, if 7400 is a quad two-input NAND in standard TTL, then 74C00 is a quad two-input NAND with the same pin connections in CMOS. The characteristic parameters of the 74C series CMOS are more or less the same as those of 4000-series devices.

5.5.2.3 74HC/HCT Series

The 74HC/HCT series is the high-speed CMOS version of the 74C series logic functions. This is achieved using silicon-gate CMOS technology rather than the metal-gate CMOS technology used in earlier 4000-series CMOS subfamilies. The 74HCT series is only a process variation of the 74HC series. The 74HC/HCT series devices have an order of magnitude higher switching speed and also a much higher output drive capability than the 74C series devices. This series also offers pin-to-pin replacement of 74-series TTL logic functions. In addition, the 74HCT series devices have TTL-compatible inputs.

5.5.2.4 74AC/ACT Series

The 74AC series is presently the fastest CMOS logic family. This logic family has the best combination of high speed, low power consumption and high output drive capability. Again, 74ACT is only a process variation of 74AC. In addition, 74ACT series devices have TTL-compatible inputs.

The characteristic parameters of the 74C/74HC/74HCT/74AC/74ACT series CMOS are summarized as follows (for $V_{DD} = 5\text{ V}$): V_{IH} (min.) = 3.5 V (74C), 3.5 V (74HC and 74AC) and 2.0 V (74HCT and 74ACT); V_{OH} (min.) = 4.5 V (74C) and 4.9 V (74HC, 74HCT, 74AC and 74ACT); V_{IL} (max.) = 1.5 V (74C), 1.0 V (74HC), 0.8 V (74HCT), 1.5 V (74AC) and 0.8 V (74ACT); V_{OL} (max.) = 0.5 V (74C) and 0.1 V (74HC, 74HCT, 74AC and 74ACT); I_{IH} (max.) = 1 μA ; I_{IL} (max.) = 1 μA ; I_{OH} (max.) = 0.4 mA (74C), 4.0 mA (74HC and 74HCT) and 24 mA (74AC and 74ACT); I_{OL} (max.) = 0.4 mA (74C), 4.0 mA (74HC and 74HCT) and 24 mA (74AC and 74ACT); V_{NH} = 1.4 V (74C, 74HC and 74AC) and 2.9 V (74HCT and 74ACT); V_{NL} = 1.4 V (74C), 0.9 V (74HC), 0.7 V (74HCT and 74ACT) and 1.4 V (74AC); propagation delay = 50 ns (74C), 8 ns (74HC and 74HCT) and 4.7 ns (74AC and 74ACT); power dissipation per gate (for $f = 100\text{ kHz}$) = 0.1 mW (74C), 0.17 mW (74HC and 74HCT) and 0.08 mW (74AC and 74ACT); speed–power product (for $f = 100\text{ kHz}$) = 5 pJ (74C), 1.4 pJ (74HC and 74HCT) and 0.37 pJ (74AC and 74ACT); maximum flip-flop toggle rate = 12 MHz (74C), 40 MHz (74HC and 74HCT) and 100 MHz (74AC and 74ACT).

Example 5.7

Draw the internal schematic of: (a) a two-wide, four-input AND-OR-INVERT logic function in CMOS and (b) a two-wide, four-input OR-AND-INVERT logic function in CMOS.

Solution

(a) Let us assume that A, B, C, D, E, F, G and H are the logic variables. The output Y of this logic function can then be expressed by the equation

$$Y = \overline{A.B.C.D + E.F.G.H} \quad (5.5)$$

Following the principles explained earlier in the text, the internal schematic is shown in Fig. 5.53(a). Series connection of N-channel MOSFETs on the left simulates ANDing of A, B, C and D , whereas series connection of N-channel MOSFETs on the right simulates ANDing of E, F, G and H . Parallel connection of two branches produces ORing of the ANDed outputs. Since the P-channel MOSFET arrangement is the complement of the N-channel MOSFET arrangement, the final output is what is given by Equation (5.5).

(b) The output Y of this logic function can be expressed by the equation

$$Y = \overline{(A + B + C + D).(E + F + G + H)} \quad (5.6)$$

Figure 5.53(b) shows the internal schematic, which can be explained on similar lines.

Example 5.8

Determine the logic function performed by the CMOS digital circuit of Fig. 5.54.

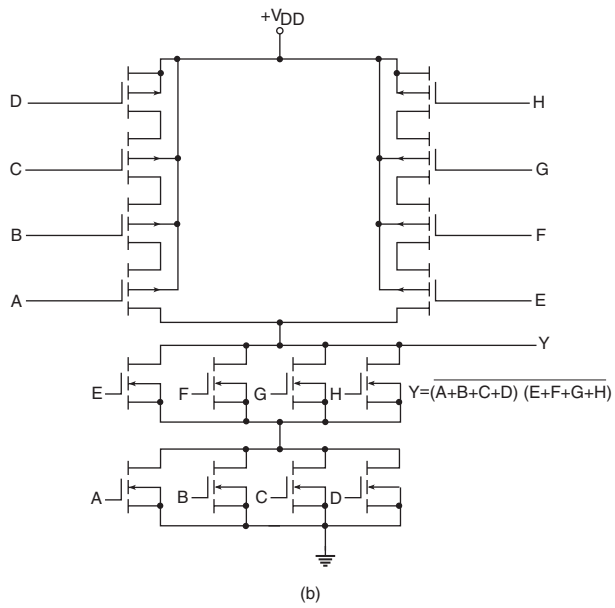
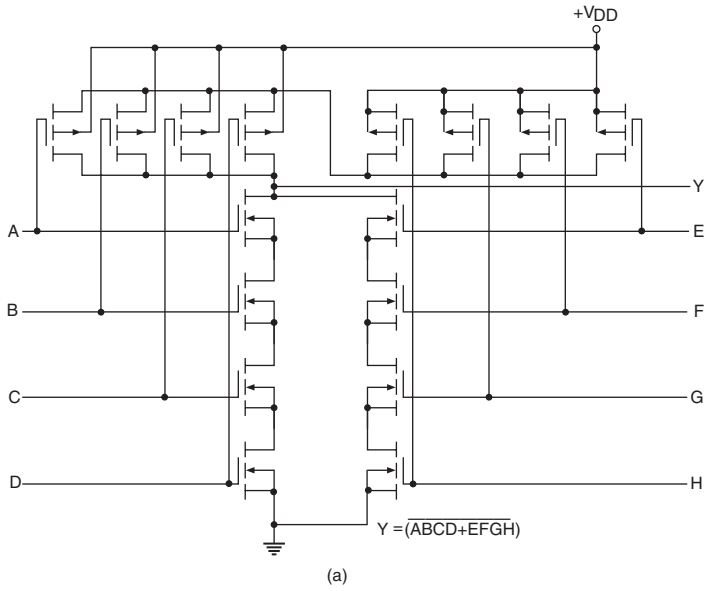


Figure 5.53 Example 5.7.

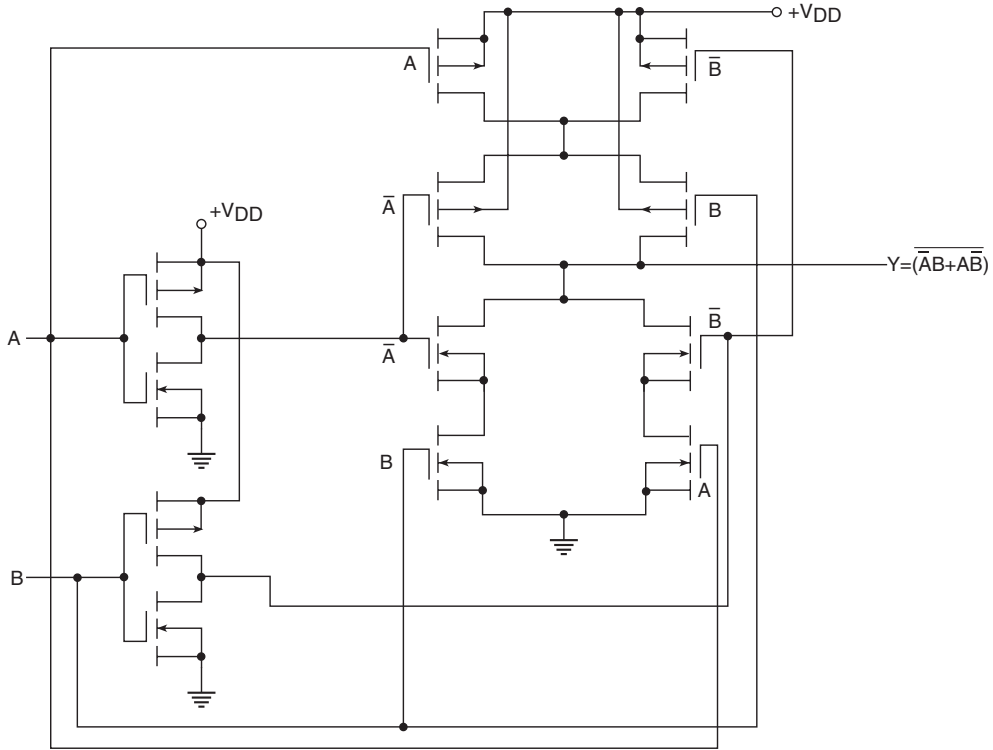


Figure 5.54 Example 5.8.

Solution

The given circuit can be divided into two stages. The first stage comprises two inverters that produce \bar{A} and \bar{B} . The second stage is a two-wide, two-input AND-OR-INVERT circuit. Inputs to the first AND are \bar{A} and B , and inputs to the second AND are A and \bar{B} . The final output is therefore given by $Y = (\bar{A}B + A\bar{B})$, which is an EX-NOR function.

5.6 BiCMOS Logic

The BiCMOS logic family integrates bipolar and CMOS devices on a single chip with the objective of deriving the advantages individually present in bipolar and CMOS logic families. While bipolar logic families such as TTL and ECL have the advantages of faster switching speed and larger output drive current capability, CMOS logic scores over bipolar counterparts when it comes to lower power dissipation, higher noise margin and larger packing density. BiCMOS logic attempts to get the best of both worlds. Two major categories of BiCMOS logic devices have emerged over the years since its introduction in 1985. In one type of device, moderate-speed bipolar circuits are combined with high-performance CMOS circuits. Here, CMOS circuitry continues to provide low power dissipation and larger packing density. Selective use of bipolar circuits gives improved performance. In the other

category, the bipolar component is optimized to produce high-performance circuitry. In the following paragraphs, we will briefly describe the basic BiCMOS inverter and NAND circuits.

5.6.1 BiCMOS Inverter

Figure 5.55 shows the internal schematic of a basic BiCMOS inverter. When the input is LOW, N-channel MOSFETs Q_2 and Q_3 are OFF. P-channel MOSFET Q_1 and N-channel MOSFET Q_4 are ON. This leads transistors Q_5 and Q_6 to be in the ON and OFF states respectively. Transistor Q_6 is OFF because it does not get the required forward-biased base-emitter voltage owing to a conducting Q_4 . Conducting Q_5 drives the output to a HIGH state, sourcing a large drive current to the load. The HIGH-state output voltage is given by the equation

$$V_{OH} = V_{DD} - V_{BE}(Q_5) \tag{5.7}$$

When the input is driven to a HIGH state, Q_2 and Q_3 turn ON. Initially, Q_4 is also ON and the output discharges through Q_3 and Q_4 . When Q_4 turns OFF owing to its gate-source voltage falling below the required threshold voltage, the output continues to discharge until the output voltage equals the forward-biased base-emitter voltage drop of Q_6 in the active region. The LOW-state output voltage is given by the equation

$$V_{OL} = V_{BE}(Q_6 \text{ in active mode}) = 0.7V \tag{5.8}$$

5.6.2 BiCMOS NAND

Figure 5.56 shows the internal schematic of a two-input NAND in BiCMOS logic. The operation of this circuit can be explained on similar lines to the case of an inverter. Note that MOSFETs Q_1 – Q_4

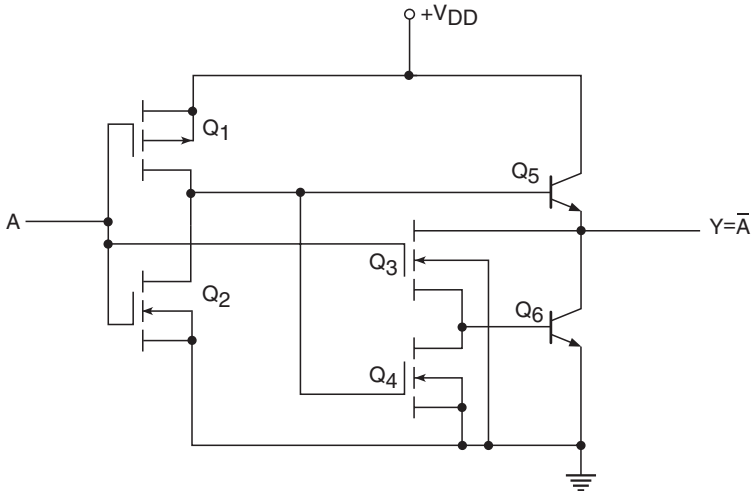


Figure 5.55 BiCMOS inverter.

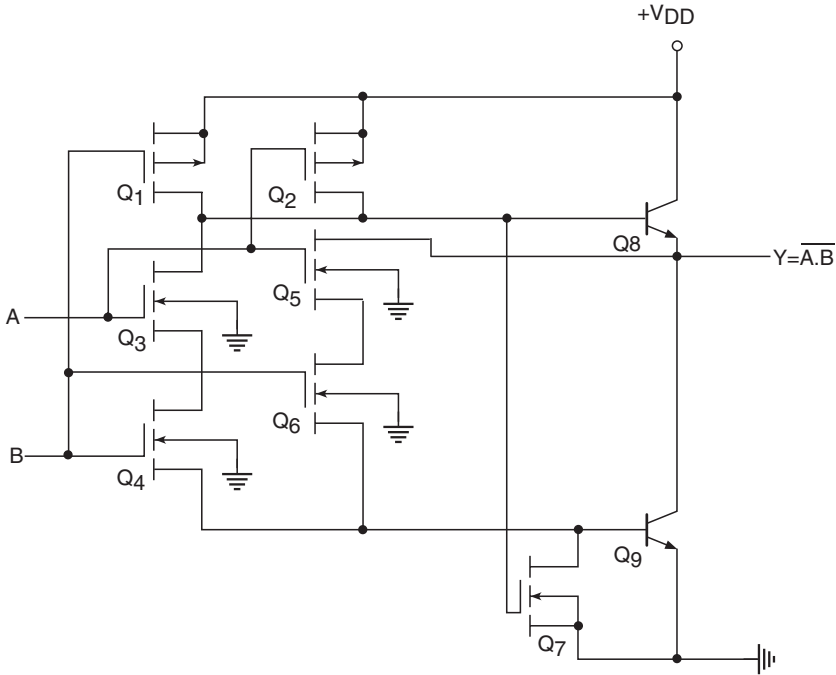


Figure 5.56 BiCMOS two-input NAND.

constitute a two-input NAND in CMOS. Also note the similarity of this circuit to the one shown in Fig. 5.55. The CMOS inverter stage of Fig. 5.55 is replaced by CMOS NAND in Fig. 5.56. N-channel MOSFET Q_3 in Fig. 5.55 is replaced by a series connection of N-channel MOSFETs Q_5 and Q_6 to accommodate the two inputs. The HIGH-state and LOW-state output voltage levels of this circuit are given by the equations

$$V_{OH} = (V_{DD} - 0.7) \quad (5.9)$$

$$V_{OL} = 0.7 \quad (5.10)$$

5.7 NMOS and PMOS Logic

Logic families discussed so far are the ones that are commonly used for implementing discrete logic functions such as logic gates, flip-flops, counters, multiplexers, demultiplexers, etc., in relatively less complex digital ICs belonging to the small-scale integration (SSI) and medium-scale integration (MSI) level of inner circuit complexities. The TTL, the CMOS and the ECL logic families are not suitable for implementing digital ICs that have a large-scale integration (LSI) level of inner circuit complexity and above. The competitors for LSI-class digital ICs are the PMOS, the NMOS and the integrated injection logic (I^2L). The first two are briefly discussed in this section, and the third is discussed in Section 5.8.

5.7.1 PMOS Logic

The PMOS logic family uses P-channel MOSFETS. Figure 5.57(a) shows an inverter circuit using PMOS logic. MOSFET Q_1 acts as an active load for the MOSFET switch Q_2 . For the circuit shown, GND and $-V_{DD}$ respectively represent a logic '1' and a logic '0' for a positive logic system. When the input is grounded (i.e. logic '1'), Q_2 remains in cut-off and $-V_{DD}$ appears at the output through

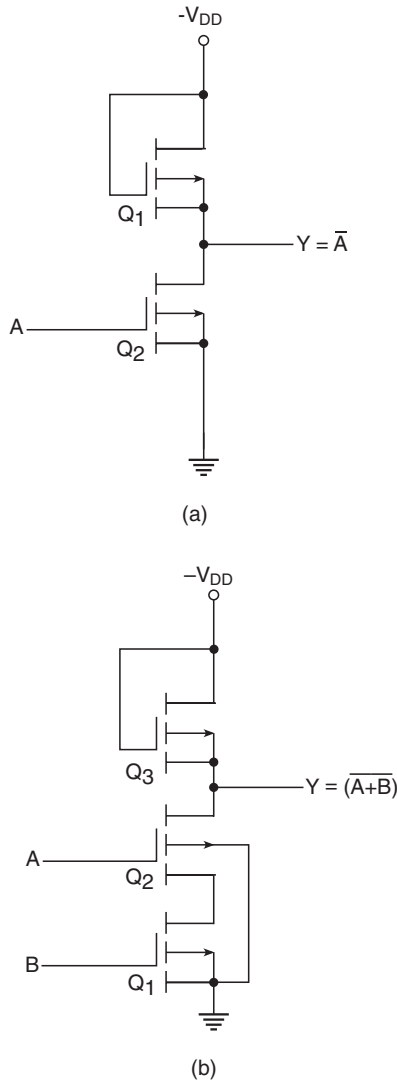


Figure 5.57 (a) PMOS logic inverter and (b) PMOS logic two-input NOR.

the conducting Q_1 . When the input is at $-V_{DD}$ or near $-V_{DD}$, Q_2 conducts and the output goes to near-zero potential (i.e. logic '1').

Figure 5.57(b) shows a PMOS logic based two-input NOR gate. In the logic arrangement of Fig. 5.57(b), the output goes to logic '1' state (i.e. ground potential) only when both Q_1 and Q_2 are conducting. This is possible only when both the inputs are in logic '0' state. For all other possible input combinations, the output is in logic '0' state, because, with either Q_1 or Q_2 nonconducting, the output is nearly $-V_{DD}$ through the conducting Q_3 . The circuit of Fig. 5.57(b) thus behaves like a two-input NOR gate in positive logic. It may be mentioned here that the MOSFET being used as load [Q_1 in Fig. 5.57(a) and Q_3 in Fig. 5.57(b)] is designed so as to have an ON-resistance that is much greater than the total ON-resistance of the MOSFETs being used as switches [Q_2 in Fig. 5.57(a) and Q_1 and Q_2 in Fig. 5.57(b)].

5.7.2 NMOS Logic

The NMOS logic family uses N-channel MOSFETs. N-channel MOS devices require a smaller chip area per transistor compared with P-channel devices, with the result that NMOS logic offers a higher density. Also, owing to the greater mobility of the charge carriers in N-channel devices, the NMOS logic family offers higher speed too. It is for this reason that most of the MOS memory devices and microprocessors employ NMOS logic or some variation of it such as VMOS, DMOS and HMOS. VMOS, DMOS and HMOS are only structural variations of NMOS, aimed at further reducing the propagation delay. Figures 5.58(a), (b) and (c) respectively show an inverter, a two-input NOR and a two-input NAND using NMOS logic. The logic circuits are self-explanatory.

5.8 Integrated Injection Logic (I²L) Family

Integrated injection logic (I²L), also known as current injection logic, is well suited to implementing LSI and VLSI digital functions and is a close competitor to the NMOS logic family. Figure 5.59 shows the basic I²L family building block, which is a multicollector bipolar transistor with a current source driving its base. Transistors Q_3 and Q_4 constitute current sources. The magnitude of current depends upon externally connected R and applied $+V$. This current is also known as the injection current, which gives it its name of injection logic. If input A is HIGH, the injection current through Q_3 flows through the base-emitter junction of Q_1 . Transistor Q_1 saturates and its collector drops to a low voltage, typically 50–100 mV. When A is LOW, the injection current is swept away from the base-emitter junction of Q_1 . Transistor Q_1 becomes open and the injection current through Q_4 saturates Q_2 , with the result that the Q_1 collector potential equals the base-emitter saturation voltage of Q_2 , typically 0.7 V.

The speed of I²L family devices is a function of the injection current I and improves with increase in current, as a higher current allows a faster charging of capacitive loads present at bases of transistors. The programmable injection current feature is made use of in the I²L family of digital ICs to choose the desired speed depending upon intended application. The logic '0' level is $V_{CE}(\text{sat.})$ of the driving transistor (Q_1 in the present case), and the logic '1' level is $V_{BE}(\text{sat.})$ of the driven transistor (Q_2 in the present case). Typically, the logic '0' and logic '1' levels are 0.1 and 0.7 V respectively. The speed–power product of the I²L family is typically under 1 pJ.

Multiple collectors of different transistors can be connected together to form wired logic. Figure 5.60 shows one such arrangement, depicting the generation of OR and NOR outputs of two logic variables A and B .

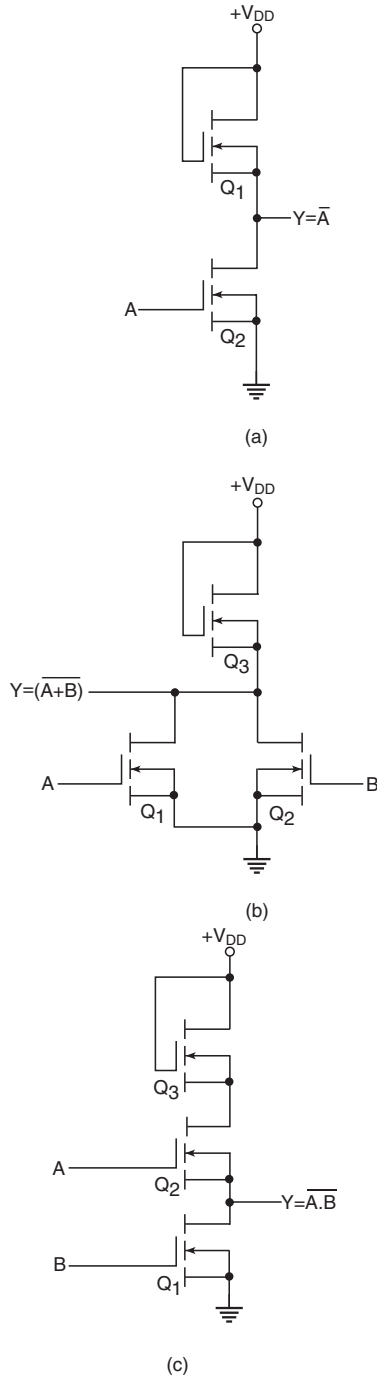


Figure 5.58 (a) NMOS logic circuit inverter, (b) NMOS logic two-input NOR and (c) NMOS logic two-input NAND.

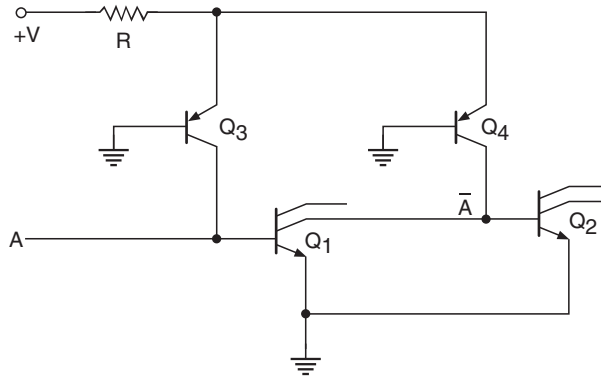


Figure 5.59 Integrated injection logic (I^2L).

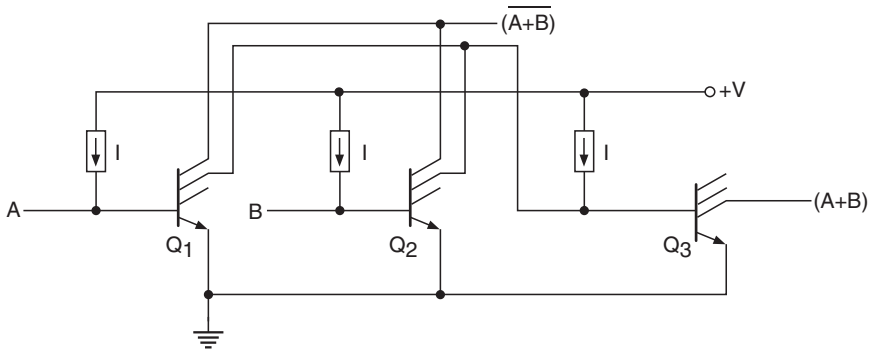


Figure 5.60 Wired logic in I^2L .

5.9 Comparison of Different Logic Families

Table 5.2 gives a comparison of various performance characteristics of important logic families for quick reference. The data given in the case of CMOS families are for $V_{DD} = 5\text{ V}$. In the case of ECL families, the data are for $V_{EE} = -5.2\text{ V}$. The values of various parameters given in the table should be used only for rough comparison. It is recommended that designers refer to the relevant data books for detailed information on these parameters along with the conditions under which those values are valid.

5.10 Guidelines to Using TTL Devices

The following guidelines should be adhered to while using TTL family devices:

1. Replacing a TTL IC of one TTL subfamily with another belonging to another subfamily (the type numbers remaining the same) should not be done blindly. The designer should ensure that

Table 5.2 Comparison of various performance characteristics of important logic families.

Logic family		Supply voltage (V)	Typical propagation delay (ns)	Worst-case noise margin (V)	Speed–power product (pJ)	Maximum flip-flop toggle frequency (MHz)
TTL	Standard	4.5 to 5.5	17	0.4	100	35
	L	4.5 to 5.5	60	0.3	33	3
	H	4.5 to 5.5	10	0.4	132	50
	S	4.5 to 5.5	5	0.3	57	125
	LS	4.5 to 5.5	15	0.3	18	45
	ALS	4.5 to 5.5	10	0.3	4.8	70
	AS	4.5 to 5.5	4.5	0.3	13.6	200
	F	4.5 to 5.5	6	0.3	10	125
CMOS	4000	3 to 15	150	1.0	5	12
	74C	3 to 13	50	1.4	5	12
	74HC	2 to –6	8	0.9	1.4	40
	74HCT	4.5 to 5.5	8	1.4	1.4	40
	74AC	2 to 6	4.7	0.7	0.37	100
	74ACT	4.5 to 5.5	4.7	0.72.9	0.37	100
ECL	MECL III	–5.1 to –5.3	1	0.2	60	500
	MECL 10K	–4.68 to –5.72	2.5	0.2	50	200
	MECL 10H	–4.94 to –5.46	1	0.15	25	250
	ECLINPS™	–4.2 to –5.5	0.5	0.15	10	1000
	ECLINPS	–4.2 to –5.5	0.2	0.15	10	2800
	LITE™					

the replacement device is compatible with the existing circuit with respect to parameters such as output drive capability, input loading, speed and so on. As an illustration, let us assume that we are using 74S00 (quad two-input NAND), the output of which drives 20 different NAND inputs implemented using 74S00, as shown in Fig. 5.61. This circuit works well as the Schottky TTL family has a fan-out of 20 with an output HIGH drive capability of 1 mA and an input HIGH current requirement of 50 μ A. If we try replacing the 74S00 driver with a 74LS00 driver, the circuit fails to work as 74LS00 NAND has an output HIGH drive capability of 0.4 mA only. It cannot feed 20 NAND input loads implemented using 74S00. By doing so, we will be exceeding the HIGH-state fan-out capability of the device. Also, 74LS00 has an output current-sinking specification of 8 mA, whereas the input current-sinking requirement of 74S00 is 2 mA. This implies that 74LS00 could reliably feed only four inputs of 74S00 in the LOW state. By feeding as many as 20 inputs, we will be exceeding the LOW-state fan-out capability of 74LS00 by a large margin.

2. None of the inputs and outputs of TTL ICs should be driven by more than 0.5 V below ground reference.
3. Proper grounding techniques should be used while designing the PCB layout. If the grounding is improper, the ground loop currents give rise to voltage drops, with the result that different ICs will not be at the same reference. This effectively reduces the noise immunity.

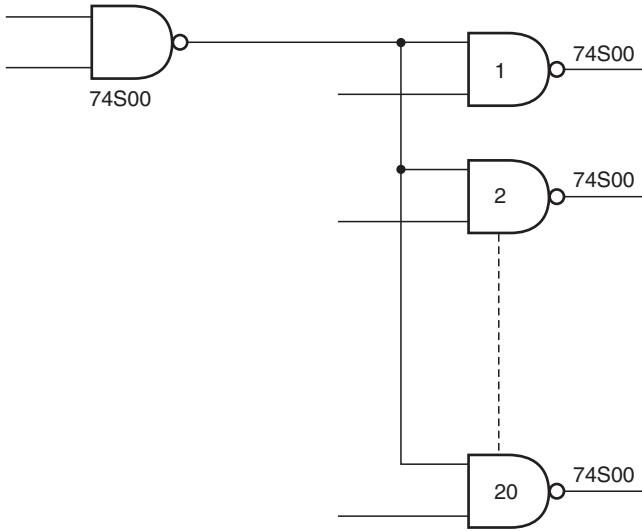


Figure 5.61 Output of one TTL subfamily driving another.

4. The power supply rail must always be properly decoupled with appropriate capacitors so that there is no drop in V_{CC} rail as the inputs and outputs make logic transitions. Usually, two capacitors are used at the V_{CC} point of each IC. A $0.1\ \mu\text{F}$ ceramic disc should be used to take care of high-frequency noise, while typically a $10\text{--}20\ \mu\text{F}$ electrolytic is good enough to eliminate any low-frequency variations resulting from variations in I_{CC} current drawn from V_{CC} , depending upon logic states of inputs and outputs. To be effective, the decoupling capacitors should be wired as close as feasible to the V_{CC} pin of the IC.
5. The unused inputs should not be left floating. All unused inputs should be tied to logic HIGH in the case of AND and NAND gates, and to ground in the case of OR and NOR gates. An alternative is to connect the unused input to one of the used inputs.
6. While using open collector devices, resistive pull-up should be used. The value of pull-up resistance should be determined from the following equations:

$$R_X = [V_{CC}(\text{max.}) - V_{OL}] / [I_{OL} - N_2(\text{LOW}) \times 1.6] \quad (5.11)$$

$$R_X(\text{max.}) = [V_{CC}(\text{min.}) - V_{OH}] / [N_1 \times I_{OH} + N_2(\text{HIGH}) \times 40] \quad (5.12)$$

where R_X is the external pull-up resistor; $R_X(\text{max.})$ is the maximum value of the external pull-up resistor; N_1 is the number of WIRED-OR outputs; N_2 is the number of unit input loads being driven; I_{OH} is the output HIGH leakage current (in mA); I_{OL} is the LOW-level output current of the driving element (in mA); V_{OL} is the LOW-level output voltage; and V_{OH} is the HIGH-level output voltage. One TTL unit load in the HIGH state = 40 mA, and one TTL unit load in the LOW-state = 1.6 mA.

5.11 Guidelines to Handling and Using CMOS Devices

The following guidelines should be adhered to while using CMOS family devices:

1. Proper handling of CMOS ICs before they are used and also after they have been mounted on the PC boards is very important as these ICs are highly prone to damage by electrostatic discharge. Although all CMOS ICs have inbuilt protection networks to guard them against electrostatic discharge, precautions should be taken to avoid such an eventuality. While handling unmounted chips, potential differences should be avoided. It is good practice to cover the chips with a conductive foil. Once the chips have been mounted on the PC board, it is good practice again to put conductive clips or conductive tape on the PC board terminals. Remember that PC board is nothing but an extension of the leads of the ICs mounted on it unless it is integrated with the overall system and proper voltages are present.
2. All unused inputs must always be connected to either V_{SS} or V_{DD} depending upon the logic involved. A floating input can result in a faulty logic operation. In the case of high-current device types such as buffers, it can also lead to the maximum power dissipation of the chip being exceeded, thus causing device damage. A resistor (typically 220 k Ω to 1 M Ω) should preferably be connected between input and the V_{SS} or V_{DD} if there is a possibility of device terminals becoming temporarily unconnected or open.
3. The recommended operating supply voltage ranges are 3–12 V for A-series (3–15 V being the maximum rating) and 3–15 V for B-series and UB-series (3–18 V being the maximum). For CMOS IC application circuits that are operated in a linear mode over a portion of the voltage range, such as RC or crystal oscillators, a minimum V_{DD} of 4 V is recommended.
4. Input signals should be maintained within the power supply voltage range $V_{SS} < V_i < V_{DD}$ ($-0.5 \text{ V} < V_i < V_{DD} + 0.5 \text{ V}$ being the absolute maximum). If the input signal exceeds the recommended input signal range, the input current should be limited to $\pm 100 \text{ mA}$.
5. CMOS ICs like active pull-up TTL ICs cannot be connected in WIRE-OR configuration. Paralleling of inputs and outputs of gates is also recommended for ICs in the same package only.
6. The majority of CMOS clocked devices have maximum rise and fall time ratings of normally 5–15 μs . The device may not function properly with larger rise and fall times. The restriction, however, does not apply to those CMOS ICs that have inbuilt Schmitt trigger shaping in the clock circuit.

5.12 Interfacing with Different Logic Families

CMOS and TTL are the two most widely used logic families. Although ICs belonging to the same logic family have no special interface requirements, that is, the output of one can directly feed the input of the other, the same is not true if we have to interconnect digital ICs belonging to different logic families. Incompatibility of ICs belonging to different families mainly arises from different voltage levels and current requirements associated with LOW and HIGH logic states at the inputs and outputs. In this section, we will discuss simple interface techniques that can be used for CMOS-to-TTL and TTL-to-CMOS interconnections. Interface guidelines for CMOS–ECL, ECL–CMOS, TTL–ECL and ECL–TTL are also given.

5.12.1 CMOS-to-TTL Interface

The first possible type of CMOS-to-TTL interface is the one where both ICs are operated from a common supply. We have read in earlier sections that the TTL family has a recommended supply

voltage of 5 V, whereas the CMOS family devices can operate over a wide supply voltage range of 3–18 V. In the present case, both ICs would operate from 5 V. As far as the voltage levels in the two logic states are concerned, the two have become compatible. The CMOS output has a $V_{OH}(\text{min.})$ of 4.95 V (for $V_{CC} = 5$ V) and a $V_{OL}(\text{max.})$ of 0.05 V, which is compatible with $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ requirements of approximately 2 and 0.8 V respectively for TTL family devices. In fact, in a CMOS-to-TTL interface, with the two devices operating on the same V_{CC} , voltage level compatibility is always there. It is the current level compatibility that needs attention. That is, in the LOW state, the output current-sinking capability of the CMOS IC in question must at least equal the input current-sinking requirement of the TTL IC being driven. Similarly, in the HIGH state, the HIGH output current drive capability of the CMOS IC must equal or exceed the HIGH-level input current requirement of TTL IC. For a proper interface, both the above conditions must be met. As a rule of thumb, a CMOS IC belonging to the 4000B family (the most widely used CMOS family) can feed one LS TTL or two low-power TTL unit loads. When a CMOS IC needs to drive a standard TTL or a Schottky TTL device, a CMOS buffer (4049B or 4050B) is used. 4049B and 4050B are hex buffers of inverting and noninverting types respectively, with each buffer capable of driving two standard TTL loads. Figure 5.62(a) shows a CMOS-to-TTL interface with both devices operating from 5 V supply and the CMOS IC driving a low-power TTL or a low-power Schottky TTL device. Figure 5.62(b) shows a CMOS-to-TTL interface where the TTL device in use is either a standard TTL or a Schottky TTL. The CMOS-to-TTL interface when the two are operating on different power supply voltages can be achieved in several ways. One such scheme is shown in Fig. 5.62(c). In this case, there is both a voltage level as well as a current level compatibility problem.

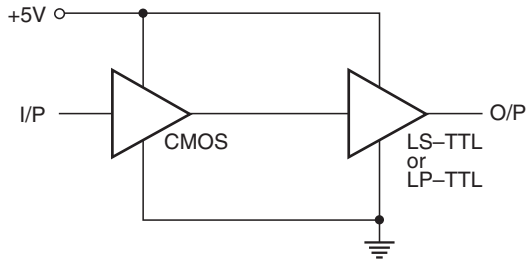
5.12.2 TTL-to-CMOS Interface

In the TTL-to-CMOS interface, current compatibility is always there. The voltage level compatibility in the two states is a problem. $V_{OH}(\text{min.})$ of TTL devices is too low as regards the $V_{IH}(\text{min.})$ requirement of CMOS devices. When the two devices are operating on the same power supply voltage, that is, 5 V, a pull-up resistor of 10 k Ω achieves compatibility [Fig. 5.63(a)]. The pull-up resistor causes the TTL output to rise to about 5 V when HIGH. When the two are operating on different power supplies, one of the simplest interface techniques is to use a transistor (as a switch) in-between the two, as shown in Fig. 5.63(b). Another technique is to use an open collector type TTL buffer [Fig. 5.63(c)].

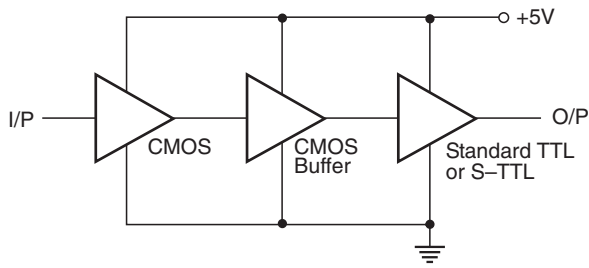
5.12.3 TTL-to-ECL and ECL-to-TTL Interfaces

TTL-to-ECL and ECL-to-TTL interface connections are not as straightforward as TTL-to-CMOS and CMOS-to-TTL connections owing to widely different power supply requirements for the two types and also because ECL devices have differential inputs and differential outputs. Nevertheless, special chips are available that can take care of all these aspects. These are known as level translators. MC10124 is one such quad TTL-to-ECL level translator. That is, there are four independent single-input and complementary-output translators inside the chip. Figure 5.64(a) shows a TTL-to-ECL interface using MC10124.

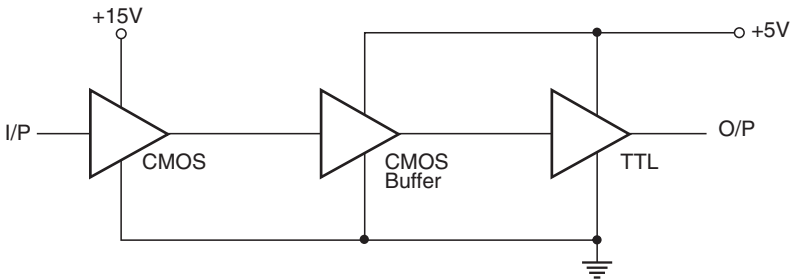
MC10125 is a level translator for ECL-to-TTL interfaces; it has differential inputs and a single-ended output. Figure 5.64(b) shows a typical interface schematic using MC10125. Note that in the interface schematics of Figs 5.64(a) and (b), only one of the available four translators has been used.



(a)

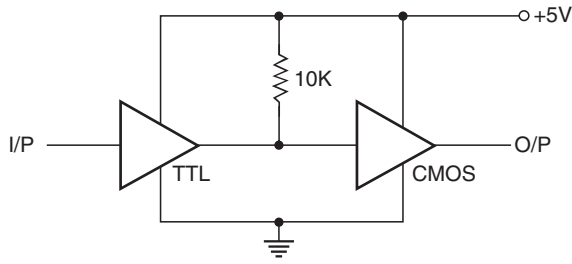


(b)

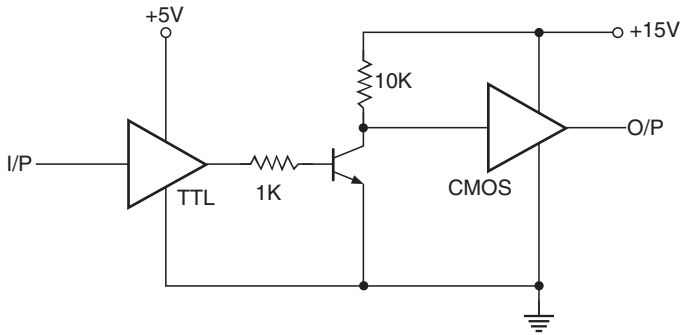


(c)

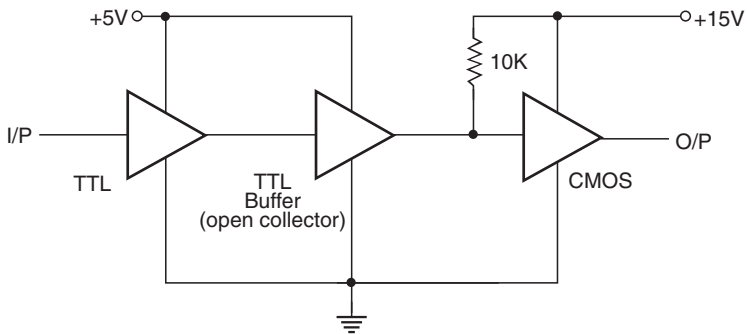
Figure 5.62 CMOS-to-TTL interface.



(a)



(b)



(c)

Figure 5.63 TTL-to-CMOS interface.

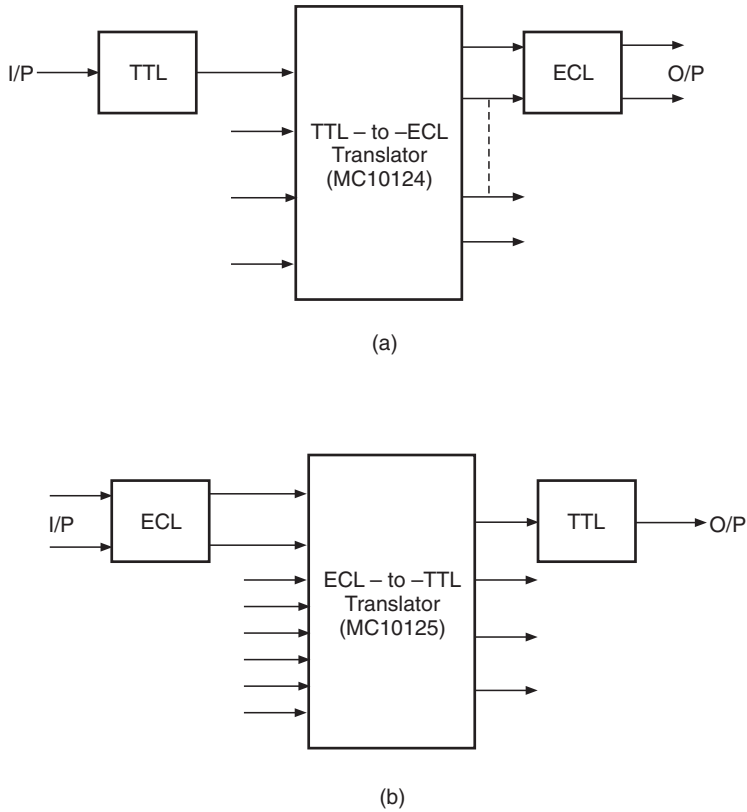


Figure 5.64 TTL-to-ECL and ECL-to-TTL interfaces.

5.12.4 CMOS-to-ECL and ECL-to-CMOS Interfaces

CMOS-to-ECL and ECL-to-CMOS interfaces are similar to the TTL-to-ECL and ECL-to-TTL interfaces described. Again, dedicated level translators are available. MC10352, for instance, is a quad CMOS-to-ECL level translator chip. A CMOS-to-ECL interface is also possible by having firstly a CMOS-to-TTL interface followed by a TTL-to-ECL interface using MC10124 or a similar chip. Figure 5.65(a) shows the arrangement. Similarly, an ECL-to-CMOS interface is possible by having an ECL-to-TTL interface using MC10125 or a similar chip followed by a TTL-to-CMOS interface. Figure 5.65(b) shows a typical interface schematic.

5.13 Classification of Digital ICs

We are all familiar with terms like SSI, MSI, LSI, VLSI and ULSI being used with reference to digital integrated circuits. These terms refer to groups in which digital ICs are divided on the basis of the complexity of the circuitry integrated on the chip. It is common practice to consider the complexity of

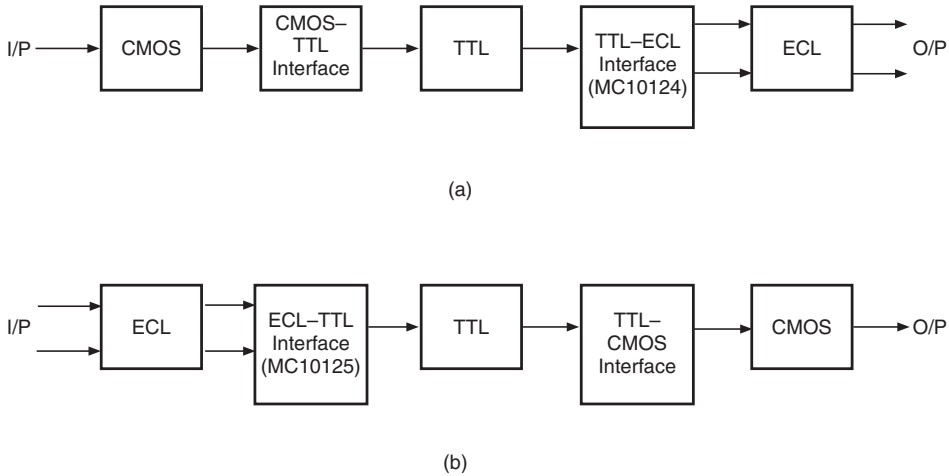


Figure 5.65 CMOS-to-ECL and ECL-to-CMOS interfaces.

a logic gate as a reference for defining the complexities of the other digital IC functions. A broadly accepted definition of different groups of ICs mentioned above is as follows.

A small-scale integration (SSI) chip is one that contains circuitry equivalent in complexity to less than or equal to 10 logic gates. This category of digital ICs includes basic logic gates and flip-flops. A medium-scale integration (MSI) chip is one that contains circuitry equivalent in complexity to 10–100 gates. This category of digital ICs includes multiplexers, demultiplexers, counters, registers, small memories, arithmetic circuits and others. A large-scale integration (LSI) chip is one that contains circuitry equivalent in complexity to 100–10 000 gates. A very-large-scale integration (VLSI) chip contains circuitry equivalent in complexity to 10 000–100 000 gates. Large-sized memories and microprocessors come in the category of LSI and VLSI chips. An ultralarge-scale integration (ULSI) chip contains circuitry equivalent in complexity to more than 100 000 gates. Very large memories, larger microprocessors and larger single-chip computers come into this category.

5.14 Application-Relevant Information

Table 5.3 lists the commonly used type numbers of level translator ICs, along with the functional description. The pin connection diagrams and functional tables for TTL-to-ECL level translator IC type MC10124 and ECL-to-TTL level translator IC type MC10125 are given in the companion website.

Table 5.3 Functional index of level translators

Type number	Function
10124	Quad TTL-to-ECL translator
10125	Quad ECL-to-TTL translator
10177	Triple ECL-to-CMOS translator
10352	Quad CMOS-to-ECL translator