

## Design and Implementation of VGA Controller Using FPGA

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### Abstract

As a standard display interface, VGA (Video Graphics Array) has been widely used. This paper presents the design and implementation of VGA controller. Hardware architecture is implemented on an Altera EPIC6Q240C8 FPGA (Field Programmable Gate Array) chip. The paper has given its top layer module design and the timing function simulation. Detailed information is focused on the system architecture, hardware design and software programming. This controller is developed using only VHDL (hardware description language) based in the IEEE standards, to ensure the portability with any manufacturer. The system can display various color strip, Chinese characters and image. The results show that this proposed algorithm gives good performance with short processing time, low resource utilization, small power consumption and memory usage. Because the data can be sent directly to monitors, the design can speed up data processing, improve system reliability in real time and save hardware resource.

**Keywords:** VGA Controller, FPGA, VHDL

### 1. Introduction

At present, the research and development of applied digital systems for specific tasks are increasing, such as video conference systems, face recognition systems [1], surveillance and remote vehicle guidance systems, etc. Among them, VGA (Video Graphic Array) is the most popular display interface. A VGA Controller is a hardware exclusive system that works with high frequency signals and which it was initially implemented on PCB (Printed Circuit Board) [2]. But such solutions are often quite oversized and high power dissipation. Digital Signal Processors (DSP) [3], or Graphics Processing Units (GPU) are often used too [4]. DSP is very simple to program, and often result in systems that consume less power than FPGA, but have lesser capabilities in terms of parallelism [5]. On the other hand, GPU provides a very flexible environment for parallelism, but consume a lot of power. With the development of electronic and semiconductor technology, FPGA (Field Programmable Gates Array) provides an impacted size and low power consumption solution. FPGA also has other advantages over these platforms, these advantages are: high clock frequency, high operations per second, code portability, code libraries reusability, low cost, parallel processing, capability of interacting with high or low interfaces, security and Intellectual Property (IP) retention [6]. Only the emerging of FPGA technology made VGA controller design accessible and suitable for study, experimentation and research. There is much work carried out in the field of image processing based on FPGA, where image processing based algorithms have been widely implemented [7-12].

In this paper, the Altera's FPGA (EPIC6Q240C8) is used as the core of the hardware circuit. We take the top-down programming methodology and adopt the integration tools (Quartus version 6.1 of Altera) [13]. After giving every module compile, function simulation, layout and timing simulation, each module can be downloaded into FPGA. This method can greatly reduce the size of the circuit board and enhance the reliability of system and design flexibility. As a result, it can greatly reduce the system cost.

The remainder of this paper is organized as follows. Section 2 introduces architecture of the VGA controller system, which includes the detailed design of hardware and software. The experimental results and analysis of the design are presented in Section 3 and some final conclusions and areas of future work are given in section 4.

## 2. System architecture

The VGA controller is a larger digital system which utilizes top-down programming methodology according to hierarchy and functional separation [14]. Each functional module should be compiled and simulated, so the top-layer simulation of the VGA graphics controller can be passed without a hitch. The architecture of the VGA controller system is shown in Figure 1. It consists of the following modules: Timing Control module; VGA Display controller; 4-Of-1 MUX(multiplexor) module; LPM\_ROM module. LPM\_ROM module is generated by using Quartus II Mega Wizard. Memory Initialization File(mif) is ROM initialization data file format. There are three blocks in VGA Display controller including Color Strip Display module, Chinese Character Display module and Image Display module, which will be illuminated in detail in following subsections. In Figure 1, clk0 is the main clock signal coming from a 50MHz clock from the developing board GW48-PK3, clk2 comes from 4Hz clock signal, Reset is connected to high or low level. An ordinary VGA monitor contains 5 signals: R, G and B: tri-chromatic signal. HS: horizontal synchronization signal. VS: vertical synchronization signal [15]. All signals must meet requirements of the VGA monitor, and then the FPGA reads and display the image into a CRT (Cathode Ray Tube) and LCD (Liquid Crystal Display) monitor. It can display horizontal color strip, vertical color strip, checkerboard, Chinese characters, images and other effects according to Mode Selection value.

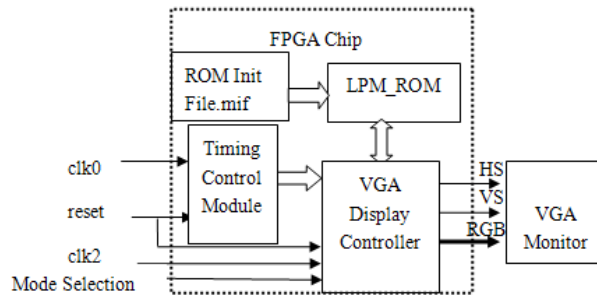


Figure 1. Architecture of the system

### 2.1. Hardware design

FPGA EPIC6Q240C8 produced by Altera is selected. It is the core hardware of system, which is responsible for the VGA Display and storage. EPIC6Q240C8 is a chip of 240 pins, among all the pins, 185 pins can be used as I/O pin at most, some of them can only act as input pin, some can be used as I/O port [16]and JTAG configuration switched by special software. It has two PLL (Phase Locked Loop) of 8ns and 6030 LE, each LE includes a LUT, a trigger and related relevant logic. Look-up table (LUT) is a RAM unit in fact.

In order to make the system run normally, there are other peripherals, for example, FPGA'S configuration chip, a 50MHz active crystal, one reset key switch, some data I/O buffers, JTAG debugging, power supplies, etc.

### 2.2. Software design

This VGA controller is developed using only VHDL (hardware description language) based in the IEEE standards, to ensure the portability with any manufacturer. The main modules include Timing Control module, VGA Display controller, LPM\_ROM module. There are three blocks in VGA Display controller unit including Color Strip Display module, Chinese Character Display module and Image Display module. All modules are mutually independent, because working mode of FPGA is parallel. The following subsections delineate each of these blocks in details.

### 2.2.1 Timing control module

The Timing control module is a key part of the display controller and VGA timing generator documents, includes line synchronization signal (HS) and field synchronization signal (VS), these signals must be in strict accordance with the VGA timing standard. The standard VGA tableau size is 640 \* 480, about 60 frames per second and the pixel clock is up to 25.175MHz [17]. Timing control is designed according to timing parameters and the external clock frequency (in figure 2 that is clk0). Pixel CLK (25MHz) defines the needed time to display the pixel information. The controller decodes the output of the vector-x counter module to generate the HS signal time. This counter may be used to locate the pixel of a given row. The output for the module vector-y Counter that increases the HS pulse may be used to generate the VS output time. The module called Frequency Divisor generates a frequency of 25MHz to work with a 640x640 resolution. If the clk0 has the exact frequency needed (that is 25MHz), the Frequency Divider module can be omitted. The architecture of the timing control module is shown in Figure 2.

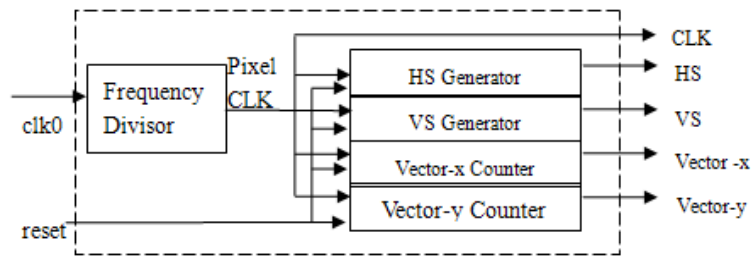


Figure 2. Architecture of timing module

In order to observe that whether the design meets the requirements, simulation test for timing module is carried out. Furthermore, we can find problems and deficiencies at the early stage of design, reduce the risk of direct hardware testing and improve the quality of design. Reset port is effective when its signal is in "low" level, vertical blanking interval acts as two horizontal scanning intervals and it is consistent with the intended design, as shown in Figure 3. The line synchronization signal (HS) and field synchronization signal are able to basically meet the requirements of the VGA display.

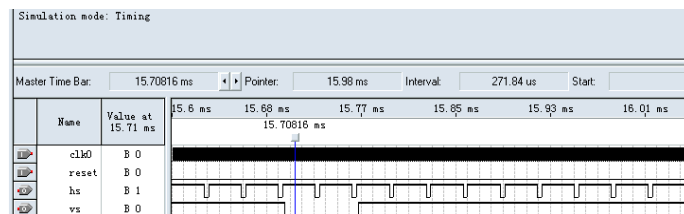


Figure 3. Results of timing simulation

### 2.2.2 LPM\_ROM module

There are two LPM\_ROM modules in this design which is Chinese characters ROM modular and Image LPM\_ROM modular

#### (1) Chinese characters ROM modular

Chinese character extraction process (16 × 16 lattice) is used during the process of the design. Open the software, input the word that you want to extract in the text box, such as "财", then click on the "seizure" with left mouse button, hexadecimal data will be shown in the lower right corner as shown in Figure 4. Then hexadecimal data should be converted to binary data, finally fill all these data in the "VGA\_ROM\_zhecai yuan.mif" file in the appropriate location.

The function of Chinese Character display module is to generate coordinates of the location of Chinese character on the display. Change of address pointer of ROM will change Chinese characters location [18]. Figure 4 indicates pixel frame and character mapping.

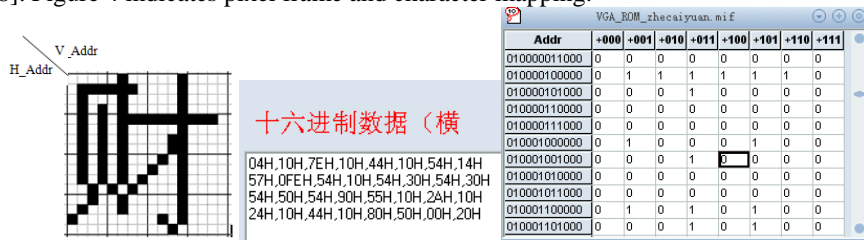


Figure 4. Pixel Frame and Character Mapping

The block LPM\_ROM memory address is a one-dimensional continuous, its storage range is 0 to 4096, 12 for the data bits, however, each Chinese character to be displayed is lattice of 16 × 16. In order to resolve this problem, one dimension address is mapped to a two-dimensional. The contents of the address can be obtained through visiting block LPM\_ROM, which produces a color signal. Therefore, the key problem to be solved is how to obtain the address of current content in LPM\_ROM block according to values of vector-y counter and vector-x counter. Of course, the number of extracted address bits will affect the display of horizontal and vertical storage location of the Chinese characters. By adopting such addressing mode, we easily solve inconsistency between LPM\_ROM addressing and character lattice addressing [19] and we save storage capacity of characters obviously.

We design Two Chinese characters LPM\_ROM modules, which are the zhecai yuan\_rom module and xiaoxun\_rom module. Zhecai yuan\_rom stores the name of our school-浙财院, xiaoxun\_rom stores our school motto -进德修业, 与时偕行. English characters and any other symbols can be displayed by adopting above principle.

(2) Image LPM\_ROM modular

The functions of Pic2Mif software are as follows: (1) Black and white picture is converted to a monochrome mif file, color picture is converted to a three-color mif file. (2) A binary file is converted to mif file using bitwise operators. We use this software to convert black and white school badge into monochrome mif file. The effect of the preview map is shown in Figure 5.



Figure 5. Pic2Mif Preview Map of school badge

The size of school badge (Xiaohui\_hei.Bmp) is 256×249, and the total bits are 63744 bits,  $215=32768 < 63744 < 216=65536$ . Therefore, 16 bit address signal is used as the block LPM\_ROM address. The entire image is fixed on the rows of the screen 128 to 384, columns 192 to 448. Therefore, it should be minus the starting row and column number so as to determine accessing to read from the address from zero.

2.2.3. VGA Display controller design

Display module is an important part of the entire display controller, which includes Color Strip display module, Chinese character display module, Image display module and 4 of 1 Mux (multiplexor) module. The architecture of Display module is shown in Figure 6. Display module outputs horizontal synchronizing signal, vertical synchronizing signal and r, g, b tri-chromatic signal,

these output signals are directly connected to the VGA interface. When the scanning signal reaches the range of the display picture, it is time to determine storage content value according to the vector-x counter and the vector-y counter, meanwhile tri-chromatic signal value can be read out from the corresponding position in the storage. Tri-chromatic signal ought to be sent to the monitor after selecting by the 4 of 1 multiplexor.

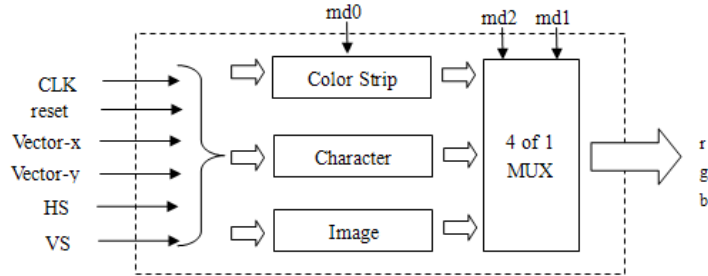


Figure 6. Architecture of the VGA display controller module

(1) Color stripe Display module

The main function of the module is to allocate the width and the color of color stripe [20]. Divide the screen into eight equal portions according to the horizontal and vertical direction and give each portion the same RGB value. Display the corresponding color in the corresponding position to obtain the desired strip signal. Checkerboard signal is XOR of the horizontal color bar and the vertical color bar.

(2) Character Display Module

The module is to locate Chinese characters display coordinate position and determine the storage content value according to the address of vector-x counter and vector-y counter. We can also control the corresponding color of character by changing color signal code.

(3) Image Module

The module is to realize the image display and control color variations, as well as the movement direction of the image.

(4)4-Of-1 MUX (multiplexor)

The function of module is to select one channel data as output from the multi-channel data. It can display horizontal color strip, vertical color strip, checkerboard, Chinese characters and images.

### 2.2.4. Top-layer diagram

The Top-layer Diagram is shown in Figure 7. Timing control module (VGASIG) generates 25MHz clock signal CLK, the horizontal and vertical sync signals. Mycolor module generates color strip. Myhanzi module generates Chinese character. Myxiaohui2 generates image. Mux4 to 1 generates mode selection signal, "00" for color strip display, "01"for the Chinese characters, "11" for the image. Mode md0 is to choose the vertical color strip, horizontal color strip and checkerboard mode. The final output signals are r, g, b, horizontal and vertical sync signals which are all connected to the VGA monitor. Reset is active when it is in low level.

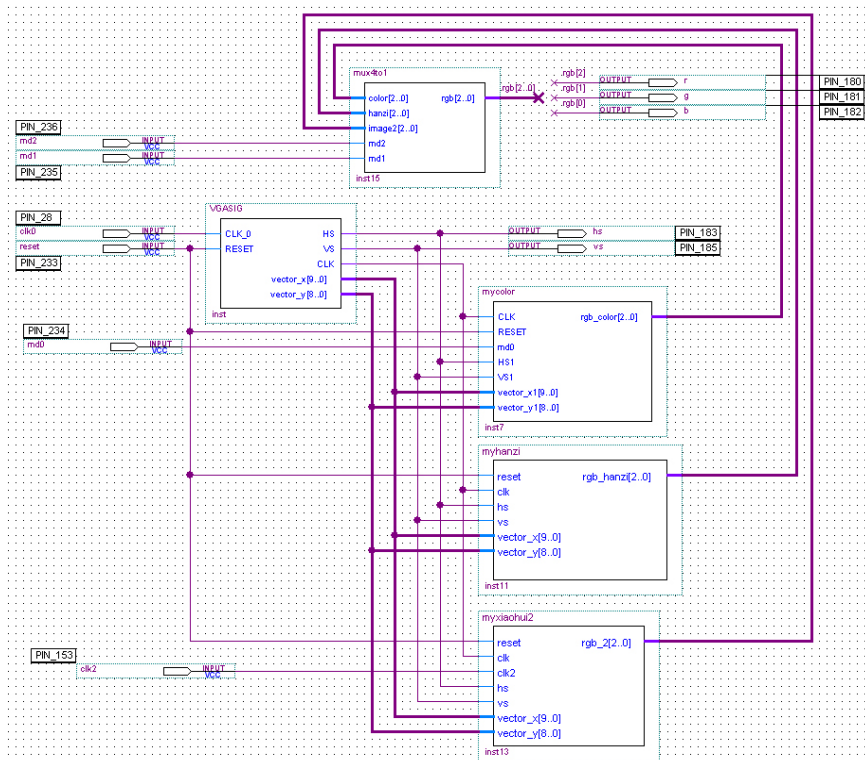


Figure 7. Top-layer Diagram

### 3. Experimental results and discussion

In order to be able to see the results obtained from the proposed algorithms on an FPGA, a standard VGA monitor may be chosen. The monitor used is a VGA port CRT. However, the system can be connected to any VGA port LCD (Liquid Crystal Display) or CRT (Cathode Ray Tube) monitor. Connect USB-Blaster between PC and experiment box, turn on power supply and select Programmer in Tools menu. Moreover, we should connect clock0 to 50MHz clock signal, clock2 to the 4Hz clock signal. If the above steps have been finished, download the top layer file into the target device (EPIC6Q240C8). After downloading successfully, choose working mode of electric circuit and control the corresponding mode selection button and observe how the monitor changes its display.

The system can generate three kinds of color strip: horizontal color strip, vertical color strip and checkerboard. The effect is shown in Figure 8.

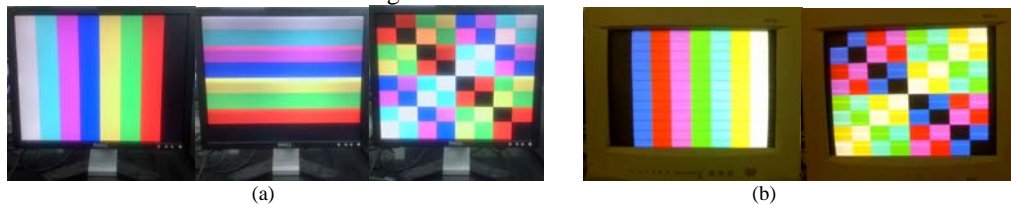


Figure 8. Color Strip displayed on a monitor (a) LCD Monitor, (b) CRT Monitor

Figure 9 shows the experiment results of two kinds of Chinese characters' arrangements, one is the "浙财院", which is three words and arranged by vertically, the other is arranged horizontally with "进德修业与时偕行". Moreover, if the value of the counter which controlling the position of the corresponding data value is changed, display positions of Chinese characters are also changed. There can be displayed more Chinese characters if an external RAM memory be added. And it is very

convenient to change the characters and we can move where the characters are displayed through adjusting coordinates in the display area.



**Figure 9.** Chinese character display

The experimental results of the image color variation (the order is Blue, Green, Cyan, Red, Magenta, Yellow, and White) and image movement is shown in Figure 10. Furthermore, by changing the external clock frequency clock2, we can control the frequency of changes in image color and the movement speed of the image.



**Figure 10.** Image Color Variation (Blue, Green, Cyan, Red, Magenta, Yellow, White) and Image Movement

From the experiment result, we can see that the benefits of using FPGA are obvious. In the process of system design and debugging, we can adjust or modify the system hardware at any time, but do not need to really change the ready-made board and the devices already soldered on the board. Modifications and adjustments can be made in the Altera Quartus II design environment. This controller is developed using only VHDL (hardware description language) based in the IEEE standards, to ensure the portability with any manufacturer, and this is part of the contribution of this work.

#### 4. Conclusion and Future Work

In the proposed VGA control system, FPGA is used for developed this system, which can display horizontal color Strips, vertical color Strips, checkerboard, Chinese characters, image. This architecture may be used in any FPGA device regardless of the brand or model. Experimental results show processing algorithms programmed by VHDL can make design flexible and programming conveniently. This method changes traditional design concept of VGA display system by using the programming devices and also opens up a new road for embedded systems design. The controller will be used for image processing research. In the future we can also use this design to solve some others control task which is high qualified for complexity and real-time, and this design is very useful for using and designing of all kinds of portable devices and embedded systems in miniature. We can also adopt more advanced ARM MCU and FPGA chip to improve the storage speed.

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