Fundaments of Digital Design with FPGAs
Implementation in Xilinx FPGAs

First Day

Introduction to Programmable Logic Devices (PLDs)

- PLDs brief history
- Complex PLDs (CPLDs)
- FPGAs: Arquitecture
- Xilinx FPGAs, Spartan y Virtex: Arquitecture

FPGA Components

- LUTs, CLBs, Slices
- FPGA routing, interconnections
- Clock routing, Clock buffers
- DLLs/PLLs. Different modes
- Memory block. Types of memories
- DSP Blocks. Applications
- Primitives. Applications
- I/O Blocks. DDR FFs
- FPGA configuration

FPGA Design Techniques

- Duplicating Flip-Flops
- Pipelining
- I/O Flip-Flops
- Synchronization circuits
- Avoing Clock Skew
- Multi-clocks design

Introduction to VHDL

- Basic concepts
- oncurrent statements
- Sequential statements
- Component instantiation
- Introduction to the ISE/Web Pack environment
- Introduction to Simulation.
- Lab: design of a memory comparator

Second Day

Synthesis Techniques

- Coding tips
- Instantiating resources. Spartan/Virtex
- Synthesis options. Inferring memories
- Inferring specific components
- Introduction to Synplify Pro Software
- Lab: using different synthesis options

CORE Generator

- Introduction
- CORE Generator System. Use
- CORE Generator flow design
- Lab: Read/Write a double port memory

Constraints

- Timing Constraints
- I/O Pin assignment
- Location constraints (RLOC)
- User Constraint File (.ucf)
- Constraints Editor. Use
- .ucf: text file
- Lab: Constraints usage

Third Day

Reports Analysis

- Map report
- Timing Analyzer report
- Timing report Interpretation
- Place & Route report
- Lab: read and comprehension of different reports

Other ISE Tools

- Floorplanner Demo
- FPGA Editor Demo
- ChipScope demo

Advanced Subjects

- False Paths
- Multi-cycle Paths
- Advanced Place & Route options
- Advanced Timing Constraints options
- Use of Scripts
- Lab: Implementing a complex digital design in FPGA.