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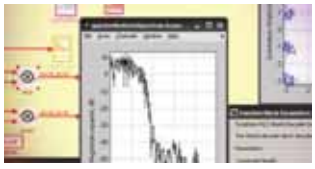

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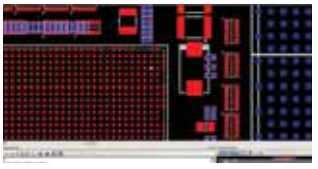

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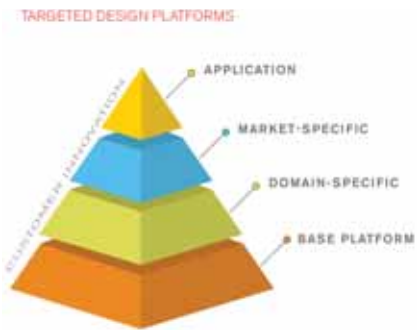
Welcome to the 2010 FPGA and CPLD Solutions Resource Catalog

In the midst of turbulent economic, technological and market conditions throughout 2009, the Xilinx design community embodied a spirit of innovation. You placed your bets on fewer, highly differentiated end product designs, leveraging cost-effective, flexible, programmable solutions to fuel inventiveness across a wide range of markets.

In this year's edition of the FGPA and CPLD Solutions Resource Catalog, you'll learn more about the best-in-class programmable platforms – silicon, software, IP, boards, kits, reference designs – Xilinx and our ecosystem partners are delivering to hardware and software designers. You can pick and choose from a variety of Targeted Design Platform options to jumpstart your development projects in 2010, taking advantage of open standards, common design methodologies, development tools, and run-time platforms.

Our flagship Virtex®-6 and Spartan®-6 FPGA platforms fully exploit the benefits of Moore's Law to deliver increased performance, densities and system-level functionality, while driving down cost and power consumption. Virtex-6 is ideally suited to compute-intensive, high-speed, high-density SoC applications, and Spartan-6 is targeted for applications where size, power, and cost are key considerations. Each family serves as the foundation for simpler, smarter programmable platforms, including: base (silicon, IP, logic tools, boards, reference designs), domain-specific (embedded processing, DSP or logic/connectivity IP & tools, FMC daughter cards), and market-specific (IP, custom tools & boards).



In the coming year, we see tremendous opportunities in electronics infrastructure applications, such as wired communications, 3G and LTE wireless deployment requiring high performance DSP processing in excess of 1000 Giga operations per second and packet processing at a rate of more than 100 Gbps. Green IT will need power efficient, high performance, compute architectures to exploit high level parallel computing. The smart grid will rely on programmable, flexible appliances and metering. And finally, surveillance and security will require sophisticated image processing algorithms. Altogether, these compute-intensive applications are ideally suited to the performance and flexibility of today's leading edge FPGAs.

We look forward to witnessing again the magnificent spirit of innovation you'll bring to the diverse markets you serve. It's just this spirit that led to the invention of the programmable chip 25 years ago by Xilinx founder and 2009 National Inventors Hall of Fame inductee Ross Freeman. A spirit that is alive within today's designers who – like Ross – have the courage to imagine and create the 'impossible.'

Moshe Gavrielov
President and CEO Xilinx

FPGA and CPLD Solutions Resource Catalog 2010

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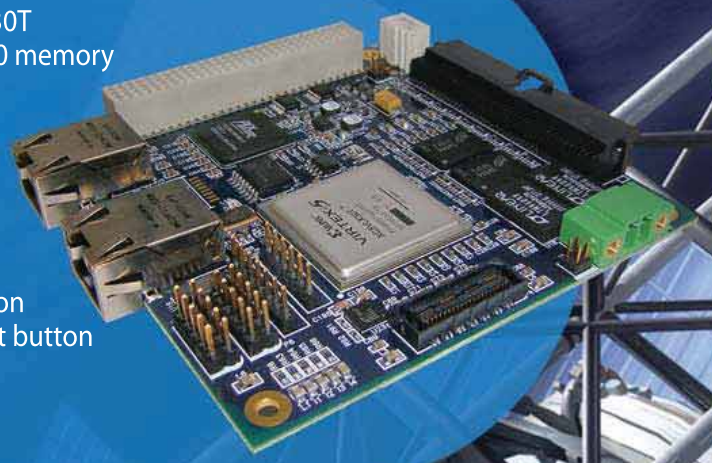

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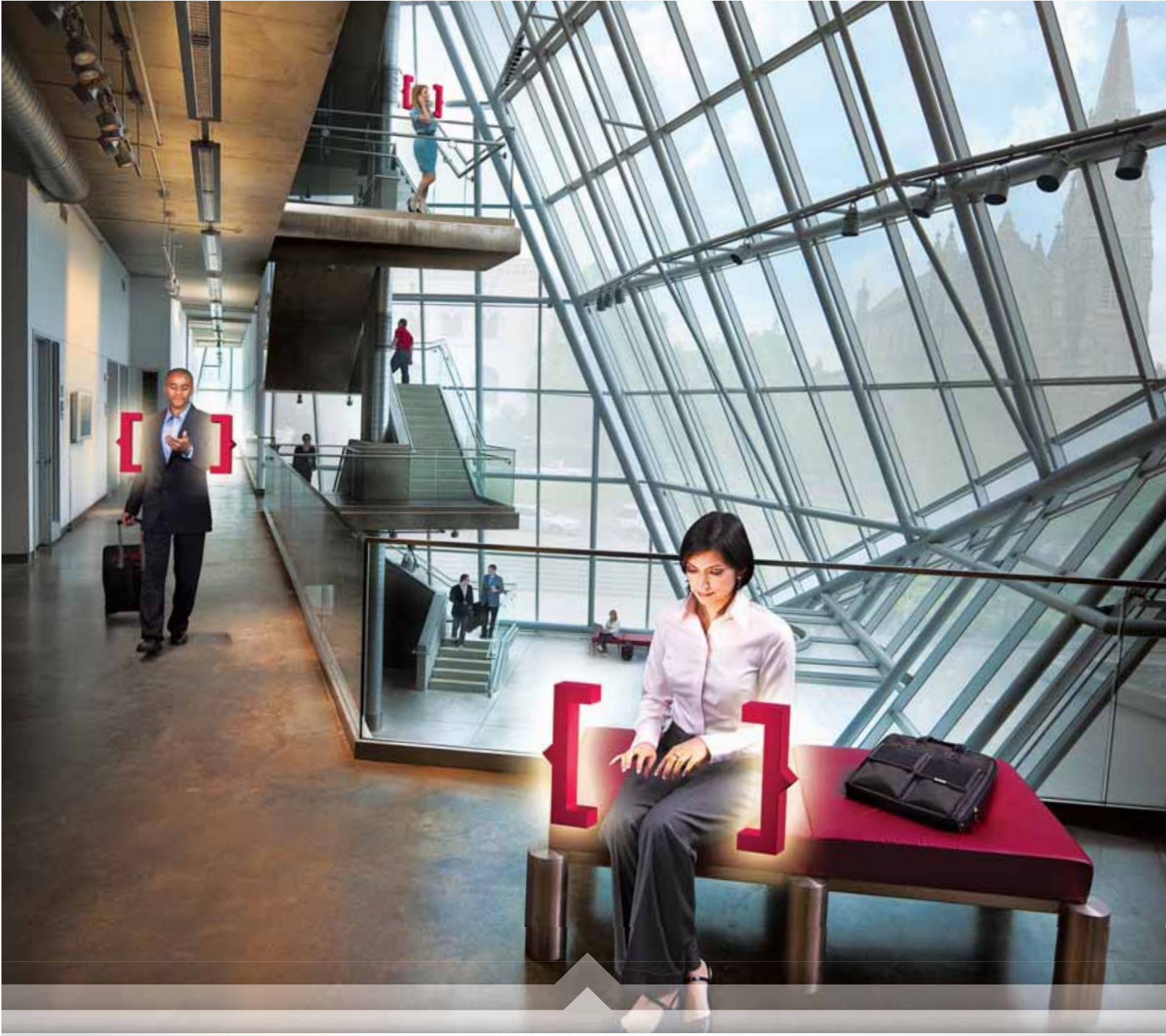

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Industry Forecast

Changes in ASIC Landscape Open Opportunities for FPGAs

by Ann Steffora Mutschler

Economic, financial and competitive conditions are forcing ASIC and ASSP vendors to focus their efforts on very high volume markets and applications thereby creating a gap in the available technical solutions available to the markets being vacated by traditional silicon platforms.

As such, programmable devices are increasingly being used by electronics manufacturers of all types to fill this gap, according to Vin Ratford, Senior VP of World Wide Marketing and Business Development at Xilinx, Inc.

"Because the cost of an FPGA is amortized over multiple customers, we give just about anyone who wants it access to the latest process technologies...and with each new process technology, FPGAs deliver increased levels of performance at lower costs and with lower levels of power consumption," he said.

Dr. Johannes Stahl, VP and GM of CoWare's DSP Solutions Group has noted changes in the market as well. "The FPGA market is clearly poised to enable replacing a lot of SoCs and ASSPs by off-the-shelf FPGAs, which at the advanced silicon nodes will offer the complexity and power efficiency needed to support many applications in the consumer, automotive and wireless markets. Also in some of the traditional network infrastructure markets FPGAs can take on a bigger role through a combination of optimized signal processing IP blocks together with processors on a single chip." An example for such a market is the upcoming LTE wireless standard.

To account for these changes, on the silicon side, Ratford remarked that Xilinx is continuing to drive down cost and power so that more applications can take advantage of FPGA technology, but there is a lot happening on the system, tool and IP side of the equation as well to give a broader set of designers the development flows they need to be productive.

"For example," he continued, "the adoption of open standards, such as the FPGA Mezzanine Card (FMC VITA57) specification that defines high-speed I/O mezzanine card interfacing, and the AMBA standard for on-chip fabric communications, by FPGA vendors, IP and tool providers are also helping to bring programmable logic into the mainstream of system design."

Stahl noted that the design of FPGAs at that level of complexity is no different than the design of complex SoCs, in particular, when the FPGAs carry processor cores. "With costs and risk associated with producing a mask set are gone for FPGA devices, the ROI for OEMs comes down to reducing the development cost for algorithm design, architecture design, software development, that occur on top of the traditional RTL development and backend design. While reprogramming FPGAs sounds conceptually attractive it is not a viable option to get to market fast enough. Therefore tools that apply for SoC/ASSP design and software development apply for FPGA in a similar way."

"The market for Electronic System Virtualization (ESV) solutions that CoWare today sells into semiconductor companies and OEMs is still nascent for FPGAs," he said, "and with the recent announcement of the industry leader Xilinx partnering with ARM to include ARM Cortex® Processors and related ARM interconnects on their chips, a direction is set, that will require wide spread adoption of ESV tools by FPGA customers over the next 2 years. ESV adoption for FPGAs will become the key enabler for FPGA companies going after SoC and ASSP sockets at major OEMs. System OEMs are investing today in ESV solutions that prepare them to take advantage of the broader range of silicon suppliers they can leverage with the advent of platform-based FPGAs."

In terms of consultation and design services, Jim Henderson, president of Innovative Integration has seen a huge surge in the number of customers requesting these services in the early stages of projects to help accelerate customer product launches. "Typically, we are asked to simulate custom signal processing algorithms in Matlab, then embed the resultant code in Virtex 5 FPGAs. Usually, some C++ application code is also provided to create the infrastructure for the final application."

Henderson has also noted a substantial upward trend in the number of customers requiring ruggedized FPGA-based products. "These customers typically required extended temperature operation, but mandate only middle-tier vibration and humidity levels," he said.

From the perspective of Daniel Platzker, product line director of FPGA Synthesis at Mentor Graphics Corp. the biggest trends in the FPGA market are faster and bigger chips running with less power, along with shrinking schedules – all driven by the increased cost of ASIC devel-

opment, increasing capabilities/capacity/speed/low power of FPGAs, shrinking development schedules, and the need to cut costs. "Many projects are converting from ASIC to FPGA. Users are now expecting tool robustness as with ASIC tools. Some applications that could only use ASIC can now be implemented in FPGA," he said.

There are new FPGA vendors with niche capabilities such as more than 1GHZ clock and very low power as well as some FPGA-like designs with ASIC-like costs, Platzker pointed out. "What's happening here is that some existing vendors and some new vendors are making it possible to use FPGAs, developed with FPGA design tools and with FPGA flexibility, as a starting point, and then once the customer has got the design set, the FPGA vendor will deliver an ASIC-like chip. This gives the best of both worlds - the flexibility of an FPGA with ASIC-like pricing."

Another driver for the increasing interest and use of FPGAs in place of ASICs or ASSPs is the fact that FPGAs have become much easier to develop as new, higher-level language-based development flows, leveraging C or Matlab for example, enable developers to approach FPGA development from a more familiar, abstract perspective, Ratford asserted. "Tools such as The MathWorks' Simulink have the potential to provide a graphical-based object-oriented environment for FPGA development as well as the development of hybrid FPGA/processor-based systems. Tools are also being introduced that simplify the integration of multiprocessor systems," he added.

Specific examples of new applications driving FPGAs in different markets are in automotive infotainment where designers are merging in-car access to rich media content typically found in the home with real-time access to road, traffic, and GPS information. Lane departure warning systems and driver fatigue sensing systems are other examples.

Outside of the automotive space, applications such as video surveillance and integrated analytics leverage FPGAs, along with wired and wireless communications, defense, medical and test and measurement applications – all use today's FPGAs to address emerging and changing standards, while at the same time delivering the power, performance and feature requirements that only ASICs did in the past, Ratford said.

Henderson agrees that surveillance and military applications are driving trends in the FPGA industry, and has seen a surprising number of medical or mobile instrumentation applications.

Engineering Challenges

With the increasing use of FPGAs in a wide range of application, customer demands include tools and methodology for vendor-independent designs; making verification easier; complete flow integration including PCB-FPGA co-design; meeting QoR (mainly timing closure); IP integration; embedded software development; synthesis/PAR run time; and less design iterations, according to Platzker.

Henderson noted that since the current crop of high-density FPGAs are power-hungry and run hot, customers request these devices be coupled with state-of-the-art analog I/O resulting in designs with very high power-densities. "Fortunately, the newly-announced Virtex6 devices will mitigate this issue," he said.

Finally, in terms of engineering challenges that customers are asking to be addressed, Ratford pointed to the previously mentioned FMC standard, which he said is a great example. "Because FPGA I/O interfaces are tightly coupled to the device's underlying architecture, circuit boards have to be designed specifically to handle a particular type of I/O, limiting the amount of reuse afforded to board designers. The new VITA 57 standard, also known as the FPGA Mezzanine Card (FMC), addresses this and other related I/O issues by defining an I/O mezzanine module that works intimately with an FPGA so that systems can be built modularly."

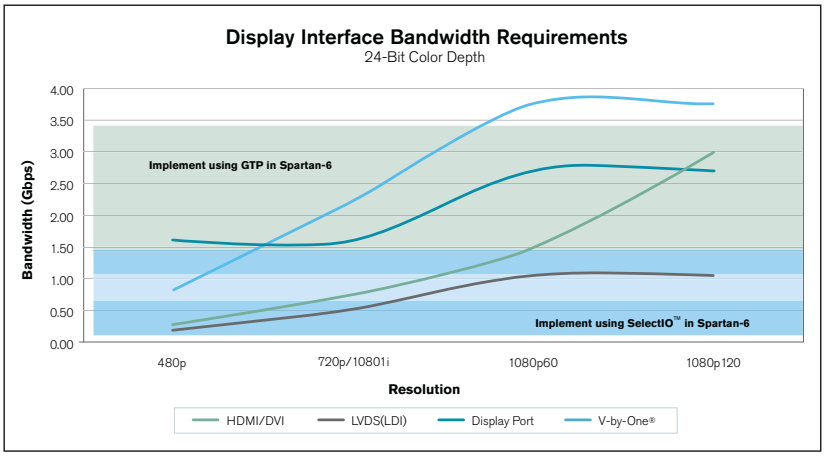
"As today's systems continue to drive more bit bandwidth, it's important to customers that we enable efficient communications between chips on a board, between the cards and equipment that make up a system, and of course on the chip itself. Serial I/O adoption continues to increase, which is why Xilinx has included resources such as hardened PC Express blocks on their chips," he continued.

"Likewise, customers are asking for more serial I/O and memory interface bandwidth on our chips because new applications require ever more memory interface bandwidth. We also need to keep up with cutting edge interface technology such as Interlaken, 100G+ Ethernet, streaming HD video, and so fourth...Power management is obviously critical. The FPGA industry continues to make improvements in the power consumption of our devices as customers require higher performance in smaller and smaller form-factors, and at the same time want to simplify heat sink and airflow. They also want to fewer and lower cost power supplies and many want to be Energy Star compliance. These are all issues you'll be seeing the FPGA industry continuing to address in coming generations of products," Ratford concluded.

Ann Steffora Mutschler is Editor of Extension Media's EECatalog Resource Catalogs, and is also a Contributing Editor to Chip Design Magazine's System-Level Design and Low-Power Design Communities. Her previous experience includes a long stint as a Senior Editor at Reed Business Information for publications including EDN, Electronic News and Electronic Business. She has moderated a number of panels in Silicon Valley and has written for publications worldwide.

Spartan-6 FPGAs —The Crystal Clear Advantage in Flat Panel TVs

By Patrick Dorsey



With integrated 3.125Gbps serial transceivers, the Spartan-6 family is ideally suited to support increasing line rate and bandwidth requirements of emerging TV standards.

IN THE AGE OF the flat panel display, top TV manufacturers have to be extremely innovative. They not only have to figure out what advanced feature set they'll include in their next line of TVs, they must differentiate their TVs from a growing number of competitors, then get those TVs to market quickly. The most innovative OEMs have figured out that the secret to staying on top and keeping their edge in the TV market is to use low-cost Xilinx® Spartan® FPGAs instead of ASSPs. In January, Xilinx in partnership with distributor Tokyo Electron Device Ltd. (TED) will make the Spartan FPGA advantage even more clear with the release of its Spartan-6 FPGA Consumer Video Kit.

A few years ago, OEMs dealt with these design and market challenges by using one ASSP-based chip set across multiple product lines. By creating various software features that leverage these chips' internal processors, they could quickly, though not too resoundingly, distinguish one TV's feature set from the others in their product line. Unfortunately, a slew of competitors followed suit and began using the same ASSP chip sets. This limited differentiation, forced the big OEMs to drop price points, which significantly deteriorated profit margins.

By switching to Spartan FPGAs, OEMs can quickly enhance and optimize the full hardware functionality (as well as software and algorithms) of each product and integrate the functions of multiple chips into a single FPGA—eliminating the restrictions of an ASSP-based solution that only allows for limited modifications. This transition from a multichip ASSP-based system to a single-chip FPGA-based system saves power, space, cooling and improves overall system performance, while reducing overall bill of materials cost, and, above all, enabling end-product differentiation.

What's more, the Spartan series' proven reliability and reprogrammability has helped OEMs drastically reduce defect rates and increase margins as well as consumer satisfaction, garnering their Spartan FPGA-based flat panel displays critical acclaim from editors and customers alike.

To build on this success in the consumer TV market and help OEMs and their suppliers leverage the integrated 3.125Gbps serial transceivers and other advanced features of Xilinx's new Spartan-6 family, in January Xilinx will announce the availability of the Spartan-6 FPGA Consumer Video Kit.

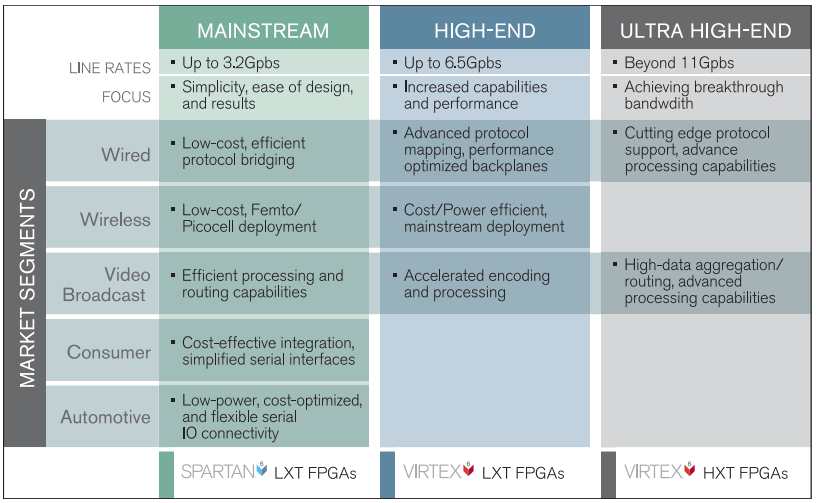
This easy-to-use and expandable kit will include a baseboard along with several FMC daughter cards, integrating soft IP logic blocks from Xilinx and its partner TED to support emerging and de facto high-speed display interfaces, including DisplayPort, V-by-One, high-speed LVDS and HDMI. The kit will streamline customer algorithm development on Spartan-6 based systems and give designers a jump on bringing differentiated products to the market quickly.

To learn more about the Spartan FPGA advantage, visit the Consumer Page at www.xilinx.com/consumer.

About the Author: Patrick Dorsey is the Sr. Director Product Management at Xilinx Inc. (San Jose, Calif.). Contact him at more_info@xilinx.com

Get Up to Speed with Multi-Gigabit Serial Transceivers

By Panch Chandrasekaran



ARE YOU BEING ASKED to make your next-generation product design connect to a high-bandwidth network with an unfamiliar or a yet-to-be-defined protocol? Are you making the transition from parallel to serial I/O chip-to-chip communications? Or do you just need the highest-serial bandwidth, most reliable multi-gigabit transceivers the industry has to offer?

You are not alone. Serial connectivity is no longer just the design domain of communications engineers. Today, a growing number of designers in the consumer, automotive, industrial control, broadcast equipment, aerospace and defense markets are being tasked with developing products that employ multi-gigabit serial transceiver technology to communicate with next-generation, high-demanding, high-speed networks.

Today's quest for more bandwidth and better efficiency means that many designers like you must quickly get up to speed with the analog nuances of multi-gigabit serial transceivers. Luckily, Xilinx® has engineered its Targeted Design Platforms to help you. Over the last two decades, the world's top telecommunications companies have relied upon Xilinx FPGAs' mix of logic functionality, high-speed memory, parallel connectivity, and serial I/O capabilities to create every generation of modern communications equipment.

With many years of experience serving the communication markets, Xilinx is able to help designers in a broad set of markets to quickly master gigabit serial transceiver technology and leverage it to create innovative products.

In 2009, Xilinx introduced both of its next-generation FPGA families — the high performance Virtex®-6 family and low-cost Spartan®-6 family providing Xilinx customers access to a full line of serial transceiver-rich FPGAs that can easily maintain line rates from up to 3.2Gbps in the Spartan-6 family, to up to 6.5Gbps in its Virtex-6 LXT devices, all the way beyond 11Gbps in the Virtex-6 HXT devices.

What's more, Xilinx announced this full range of serial connectivity-enabled FPGAs as the foundation of its new Targeted Design Platform strategy—combining the full line of transceiver-rich FPGAs with world-class tools, validated IP, reference designs, training, and support all delivered in domain and market specific kits. The Targeted Design Platforms allow customers to get their products to market faster than ever before.

With the ISE® Design Suite, customers can now get started on their designs targeting Virtex-6 HXT devices, as well as enhanced support for Spartan-6 LXT and Virtex-6 LXT and Virtex-6 SXT devices. Over the next several months, Xilinx will deliver a number of connectivity enabled design kits targeting wired, wireless broadcast video, packet processing, and traffic management application using either Virtex-6 devices for high performance, or Spartan-6 devices for low cost.

To learn more, visit the Connectivity Page at *www.xilinx.com/connectivity* where you'll find documentation, videos, links to software and IP downloads, and much more for helping you get up to speed no matter which fast lane you're on.

About the Author: Panch Chandrasekaran is the Sr. Product Marketing Manager at Xilinx Inc. (San Jose, Calif.). Contact him at more_info@xilinx.com

Extension MEDIA

Industry Forecast

FPGAs Gain Ground In China

by The EEFocus Staff

FPGAs are booming in China. When Clement Cheung, director of marketing and applications at Xilinx Asia Pacific showed up to give a speech recently, he was worried not many people would come. He need not have worried.

The sales of all the major FPGA vendors show a significant bump in sales to the Asia/Pacific region. In Xilinx's case, they exceed sales in North America, and there has been a huge increase in the number of FPGA engineers and engineers using FPGAs inside of China. This follows the shift of manufacturing to the Asia/Pacific region earlier this decade.

But Cheung said China is particularly important to FPGA vendors: "We pay more attention to the growth of Chinese enterprises because only they can truly influence the country."

The proportion of FPGAs in communications and in the enterprise fell sharply following the 2001 downturn, but FPGA vendors managed to weather the latest downturn relatively intact by limiting their presence in communications to less than 50% and by hedging across multiple other markets.

"The main reason [for growth] is the 3G network deployment in countries like China," said Clement Cheung. This was also one of the key reasons that the Asia/Pacific reason posted strong growth. Xilinx's growth in China has been in the double digits, Cheung said.

FPGAs have been particularly popular because they lower the barrier of entry for design companies. It currently costs millions of dollars for an ASIC mask, but an FPGA is a much less expensive alternative. Huawei, which applied for the most patents inside of China in 2008, based a lot of its work on FPGAs.

"In China, FPGA engineers have a larger number and all of them stand on the same starting line," Cheung said. "But FPGAs are more than a pure chip game. At present, most engineers need to consider signal integrity, layout, timing and other system-level issues."

Xilinx CEO Moshe Gavrielov pointed out that the device functions had changed in the FPGA industry over the past 25 years, evolving from the simple circuit such as peripheral interface and glue logic to the main chip of whole system. "The concept of platform was not obvious because customers didn't need too many application designs in the past. Today, the chip, software and whole design environment all need to be combined together for the project design."

EEFocus is the Chinese media partner of System-Level Design.

Technology Viewpoint

Moving Beyond Processors in the Petaflop Wars

by Dr. Robert Trout, Founder, Pico Computing, Inc.

Wherever the enemy goes, let our troops go also.

That quote, from Ulysses S. Grant, could be applied to modern computation as well as to strategies on the battlefield.

In computing, the enemy is unprocessed data. For decades we have waged war on this data by funneling it into the narrow canyons of traditional CPUs. We have pummeled it with increasingly sophisticated weaponry: pipelined instruction streams, faster caches, faster clock speeds, larger and faster memories. And yet we continue to lose ground, as the amount of data to be processed grows at rates far in excess of available CPU resources.

In recent years, the computing industry has developed and deployed hybrid platforms that combine traditional CPUs with non-traditional co-processor accelerators. These platforms are used in everything from embedded systems, in which DSPs and FPGAs share computing duties with embedded RISC processors, to the largest and fasted supercomputers, in which high-end multicore processors are paired with such devices as Cell processors, GPUs and more exotic coprocessor modules.

For many applications, however, these complex and expensive coprocessor systems are highly wasteful; they continue to move data endlessly in and out of those same computing canyons, consuming vast amounts of power to do so.

How do we increase our successes in the war on data? We take our troops to the enemy. Rather than deploying large numbers of general-purpose CPUs, GPUs and other semi-specialized coprocessors, let us instead get the legacy processors off the front lines. Traditional CPUs and their coprocessor lieutenants may still handle the majority of the world's data, for years to come, but let's stop trying to use them to solve problems for which they were never a good match. Instead, let's consider reconfigurable methods, in which we adapt our computations to meet the challenges of the data.

Consider, for example, applications in genomics and cryptography. Both domains require massive numbers of computations to be performed on very large sets of data. The characteristics of these algorithms make them ideally suited to finer-grained parallel computing methods such as FPGA clusters. These domains are not unique; in fact, many other algorithms that currently consume billions of dollars worth of the world's computing resources can be more efficiently performed using much simpler, more efficient computing methods – methods in which traditional processors provide much less of the total computing.

While they are not perfectly suited to all computations, FPGA clusters are well-proven and reliable, and they are now being deployed in large-scale applications that were until recently in the domains of CPUs. We are seeing enormous gains in computing speeds and astonishing reductions in power usage, in algorithms such as DNA sequencing, password recovery and financial analytics. And there are certain to be other data-intensive application domains in which entirely new algorithmic approaches will appear, as researchers and programmers learn to apply massively parallel computing techniques.

In summary, FPGA-based cluster computing is real and it has the potential to fundamentally change the rules of engagement for an increasingly broad set of applications. The programming of high performance, highly parallel algorithms on FPGAs remains a challenge; new skills are required. But for those who make the effort, the spoils of war are many.

Dr. Robert Trout is President of Pico Computing. Dr. Trout has over three decades of experience with embedded and high performance computing. Prior to founding Pico Computing, he was the Founder and President of Anzus, Inc. where he developed and patented innovative data compression algorithms. Dr. Trout earned his PhD at the University of Illinois. Pico Computing specializes in highly integrated cluster computing platforms based on FPGA technologies, as well as consulting and engineering services. www.pico-computing.com.

Design abstraction – tyranny or triumph?

by Rob Evans, Altium

Decades ago when Microsoft unleashed Windows on the world, a colleague disparagingly dubbed the new operating environment as 'DOS in a clown suit'. He had a point. For all the fanfare generated by Microsoft at the time, Windows was simply a GUI and application layer imposed over plain old DOS.

Yet as a front-end that abstracted the DOS operating system to a more accessible interface, Windows was a success. It removed the need to deal with the low-level complexity of the DOS command line and allowed users to work at a higher, graphical level that was more in tune with what they actually wanted to do.

Windows has now progressed, some might say painfully, to a point of sophistication that bears little resemblance to its genesis as a specialized interface to the 'real' operating system. As an evolutionary example of interface abstraction, it demonstrates the path from 'clown suit' (or more charitably, 'graphical suit') to an accessible working environment that connects into a broad world of applications and systems.

It also indicates that successfully abstracting a process is much more than just adding an interface layer that wraps around it or is imposed on top. Because a process rarely exists in isolation, an applied abstraction system needs to connect and respond to the system that surrounds it. Only then can its full potential be realized.

High Level Design

The abstraction systems used in electronics and software design are also familiar. In fact, so familiar they're considered the normal, rather than abstracted ways to work. Historically, the move to integrated circuits from discrete components is a hardware example of designing at higher abstraction. ICs allowed engineers to adopt a higher-level 'black box' approach to design where they didn't need to know (or care) what was inside the chips. By assuming the boxes would work within specification, they could be simply connected together as functional blocks and tested on some form of hardware development board.

Software design has progressed through a long path of programming languages and systems that all serve to free developers from the horrors of assembly language. Using the familiar implementations of programming interfaces, code syntax and compilers, software development harnesses high level abstraction via a huge range of languages – from Pascal through to object-orientated languages and C++. Embedded application software, the lean, mean cousin of PC application software shares much of the same principles and systems.

Significantly, the upstart and relative newcomer to the electronics development process, programmable hardware, is in the early days of its design abstraction evolution. Hardware description languages (HDLs) are used to describe the design at a register (RTL) level, which is ultimately synthesized to a gate level for implementation in the selected device – traditionally an ASIC, but now more commonly an FPGA. However the arcane nature of HDLs, often compared in complexity to assembly language, can make the task of developing embedded hardware daunting.

As a result, a range of design abstraction systems have been developed in an attempt to ease the pain. These vary widely in methodology, but are commonly schematic-based systems, graphical flow chart approaches or variants and extensions of the C language. As with the other design domains (hardware and application software), the recognizable tactic of implementing high level design systems to reduce complexity has been applied.

But there's a lurking problem – the development of programmable hardware has a unique set of characteristics that restrict the advantages of a high level approach.

Interdependent Design, but Separate Processes

One of the defining characteristics of programmable hardware is that it is intimately bound to both the physical hardware that hosts it in a design (say, an FPGA device), and any application software that runs on it. It's the meat in the sandwich, in effect, and binds the all three parts of the design together.

This in turn means that FPGA development cannot be isolated from the rest of what's now a homogenous, interdependent design process. Yet conventional development tools, regardless of what abstraction layer is imposed on them, are generally separate, disconnected design domains.

The isolation of the design processes mean that crucial decisions such as hardware-software partitioning must be decided and locked in early in the design process – there's

no scope for later variations because the domains cannot interact. Design changes such moving from a soft to hard-wired processor or implementing a software algorithm in programmable hardware would force a significant, and potentially costly, redesign though the domains. The result is a sequential and inflexible approach to design where physical hardware must be developed first, then followed by the programmable hardware and finally the application software. Little chance exists to explore design options to circumvent problems or achieve a better result.

Abstracting FPGA design to a higher level does not get around these limitations, and in some ways exacerbates them by making the domain and its design data even more exclusive. While programmable hardware design becomes significantly easier, it still does not allow for interaction with the interdependent hardware and software domains.

Unified Design Abstraction

What's needed to take the concepts of design abstraction to the next level is a complete design environment that incorporates the concepts from the ground up, so that all domains can freely interact, regardless of the level of individual design abstraction. This requires a design system that's unified at the platform level, where a single application and single pool of design data is used for the entire design process.

Embedded hardware design can then become an integral part of the design process that reaches into the hardware and application software domains. Changes in any domain will modify the single collection of data and become instantly available in the other domains, and any high level design processes are inherently 'understood' by the rest of the design system. Design abstraction in the embedded hardware space moves beyond being a simple, isolated layer that sits on top of the normal process to one that interactively permeates though the complete design system.

With such as system in place, typical tasks like implementing a USB stage in a design are vastly simplified. In this case, the USB stage is likely to have elements that need to be incorporated in all domains – connectors and interface hardware in the physical space, bus interfaces in programmable hardware, plus drivers and protocol layers in the application software domain. The single pool of design data, which includes library parts, holds a single model of the USB block that incorporates all elements. The model can be simply dropped into the design, where it is manifested in all domains regardless of their level of design abstraction. IP cores or saved design can be used in the same way.

System-Wide High Level Design

Design abstraction at this level of sophistication also opens the door to a system-based approach to electronic product development. The processes are no longer isolated, and there is less need to enforce a rigidly sequential workflow since design changes are easier and incur less design disruption.

The high level development process, now implemented globally, allows designers to focus first and foremost on creating the correct end-user experience without being swamped or distracted by low level design complexity. Hardware decisions can be fixed later in the design cycle when the requirements are fully known, the hardware-software partition is easier to move and a more iterative, exploratory approach to development is possible.

Using an abstracted design process that does not fundamentally interconnect to the rest of the system is like using Windows as just an interface to the underlying operating system. Without the base level infrastructure of programming hooks, system calls and APIs, Windows would revert to the clown suit metaphor – even though the suit actually looks rather nice now.

With today's complex electronics design tasks, high design abstraction is no longer just a desirable add-on for an individual process that it may benefit. On the contrary, as design becomes increasingly complex, which it undoubtedly will, and the lines between the design domains continue to blur, 'unified' design abstraction is rapidly becoming essential.

This approach not only makes the next generation of electronics designs possible, but also frees designers to focus on the crucial task of creating innovative and connected designs that deliver a true competitive edge.

Rob Evans studied Electronic Engineering at RMIT in Melbourne, Australia. He has over 20 years experience in the electronics design and publishing industry including several years as the Technical Editor for Electronics Australia. Rob currently holds the position of Technical Editor at Altium Limited

Xilinx Spartan-6 FPGA Family

Supported Xilinx FPGA/CPLDs: Spartan-6 LX, Spartan-6 LXT, Spartan-3/3E/3A/3AN, Spartan-3A DSP, Spartan-3 XA, Spartan-II/E

The Xilinx® Spartan®-6 FPGA family offers an optimal balance of cost, power, and performance for consumer, automotive, surveillance, wireless, and other cost and power-sensitive applications. System developers can meet the demand for new features with twice the capability at half the power consumption, while reducing system costs by up to 50 percent.

Spartan-6 FPGAs are fabricated using mature, low-power 45-nanometer process technology and feature a rich selection of built-in system blocks, including second generation DSP slices, low power (150-180mW per) high-speed serial transceivers, and PCI Express® interface cores. In addition, fast, flexible I/Os deliver over 12Gb/s memory access bandwidth with 3.3 volt compatibility and RoHS-compliant Pb-free packaging.

Spartan-6 FPGAs are 65 percent lower power than previous Spartan families with innovations in system-level power management to reduce static and dynamic power, advanced power control modes, and a low-power device option that lowers operating voltage to 1.0V to reduce power by an additional 30 percent. Developers can get started today with the Spartan-6 FPGA Evaluation Kit that provides all the elements needed to design right out of the box.

FEATURES & BENEFITS

- Advanced power control features such as hibernate and suspend modes for ultra low-power applications
- Low-power operation mode when not in use is ideal for battery powered applications
- Only low-cost and low-power FPGA to have integrated high-speed serial transceivers
- Integrated hard memory controller enables DDR3 memory support in low-cost FPGA
- Accelerates innovation and improves differentiation of lower power, 'greener' electronics with Xilinx Base-level, Domain-specific and Market-specific Targeted Design Platforms

TECHNICAL SPECS

- Spartan-6 LX FPGAs for absolute lowest cost with up to 150K logic density, 4.8Mb memory, integrated memory controllers, and high-performance system IP including up to 180 DSP blocks at 250 MHz
- Spartan-6 LXT FPGAs for lowest risk, lowest cost serial connectivity with up to eight 3.125Gb/s GTP transceivers and embedded PCI Express-compatible core, as well as up to 180 DSP slices at 250MHz

AVAILABILITY

Shipping now with the Spartan-6 FPGA Evaluation Kit available at: *www.xilinx.com/kits*

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communcations, Wireless Communications

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Xilinx, Inc.

Xilinx Virtex-6 FPGA Family

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT, Virtex-6 HXT

The Xilinx® Virtex®-6 FPGA family is optimized for the higher bandwidth and lower power demands of wireless/wired communications, broadcast, and aerospace/defense electronics. Virtex-6 FPGAs deliver more computational performance and faster networking, while simplifying and lowering system costs through integration.

This new FPGA family exploits the performance and cost benefits of advanced 40-nm process technologies to deliver higher bandwidth and more performance with less power at lower costs. DSP bandwidth exceeds 1,000 GMACS with over 2,000 DSP slices and optimized ratios of logic, Block RAM, and distributed RAM. This computational bandwidth is augmented with over 500Gbps of total serial bandwidth that is also optimized to reduce overall system power consumption.

At up to 50 percent lower power and 20 percent lower cost than previous generations, Virtex-6 FPGAs are available today as part of the Xilinx Base Targeted Design Platform enabling developers of high performance, compute-intensive electronic systems to build 'greener' products under tighter design cycles with lower development costs. Designers can start today with Virtex-6 FPGA Evaluation Kits that provide all the elements needed to design right out of the box.

FEATURES & BENEFITS

- Hit performance targets with second generation ExpressFabric™ technology, 600MHz clocking technology, and performance-tuned IP blocks
- Minimize design risk of next-generation graphics, storage, networking and system products with integrated DSP, PCIe®, and Ethernet MAC blocks
- Optimize I/O bandwidth, power, and cost over a backplane, across fiber or copper, or chip-to-chip with easy-to-use high-speed serial solutions
- Satisfy even strictest power budgets with system-level optimizations, enhanced SelectIO™ technology, and low-voltage device options
- Bring innovative products to market faster with Xilinx Base-level, Domain-specific and Market-specific Targeted Design Platforms

TECHNICAL SPECS

- Virtex-6 LXT FPGAs for high-performance logic, DSP and serial connectivity with up to 36 low-power 6.5Gb/s GTX transceivers and 864 DSP slices at 600 MHz
- Virtex-6 SXT FPGAs for ultra high-performance DSP and serial connectivity with up to 36 low-power 6.5Gb/s GTX transceivers and 2,016 DSP slices at 600 MHz
- Virtex-6 HXT FPGAs for highest bandwidth with over 1Tb/s connectivity from up to 720 SelectIO pins and 72 multi-rate transceivers, including GTH transceivers with line rates in excess of 11Gb/s

AVAILABILITY

Shipping now with the Virtex-6 FPGA Evaluation Kit available at: *www.xilinx.com/kits*

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Medical Imaging, Wired Communcations, Wireless Communications

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Spartan-6 FPGA Connectivity Kit

Supported Xilinx FPGA/CPLDs: Spartan-6 LXT

The Xilinx® Spartan®-6 FPGA Connectivity Kit is a complete, easy-to-use connectivity development and demonstration platform using the low-cost Spartan-6 LXT device family. As a Xilinx Connectivity Targeted Design Platform, this kit provides the hardware, software, IP, and Targeted Reference Designs needed to create high-speed serial systems and other connectivity applications right out of the box.

The Spartan-6 LXT FPGA enables designing with industry-standard high-speed serial protocols including PCI Express® (version 1.1), Ethernet (GMII, SFP), and DDR3, as well as enabling designs using other serial standards and proprietary implementations up to 3.125G/ps and multiple parallel protocols including 3.3V I/O standards.

The Connectivity Kit with Spartan-6 LXT FPGA simplifies design, development, and validation of multi-protocol systems with an efficient, low-cost programmable connectivity solution. Production-proven methodologies and tool suites delivered with the kit enable designers to analyze and debug high-speed serial solutions in real time.

The kit integrates the critical components of connectivity development to accelerate design, implement low-cost protocol bridging, and provide higher efficiency alternative to LVDS communication. It also serves as the starting point for market-specific connectivity design platforms with scalable building block architecture, Targeted Reference Designs, and hardware ecosystem of industry-standard FMC daughter card extensions.

FEATURES & BENEFITS

- Comprehensive connectivity development platform with all the hardware, software, firmware, IP, and reference designs needed to create fully functional working system
- ISE® Design Suite Logic and Embedded Editions tailored for system designers with ChipScope™ Pro Analyzer and Serial IO Toolkit (device-locked to Spartan-6 LX45T FPGA)
- Pre-verified, customizable Targeted Reference Design integrates PCIe®, Gigabit Ethernet, and on-board DDR3 memory with virtual FIFO and optimized Packet DMA to accelerate bandwidth
- Multiple example designs including hard memory controller, iBERT, and others

TECHNICAL SPECS

- RoHS-compliant SP605 board with Spartan-6 LX45T FPGA, universal power supply, and accessory cables
- On-board FMC daughter card connector for plug-in scalability
- USB flash drive with device driver files, design source files, applications
- Downloadable documentation with schematics, Gerber files, board BOM, and detailed user guides

AVAILABILITY

Available today at: *www.xilinx.com/kits*

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communcations, Wireless Communications

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Xilinx, Inc.

Spartan-6 FPGA DSP Kit

Supported Xilinx FPGA/CPLDs: Spartan-6 LX, Spartan-6 LXT

The Xilinx® Spartan®-6 FPGA DSP Kit provides a complete development platform for implementing DSP algorithms on low-cost, low power Spartan-6 FPGAs. As a Xilinx DSP Targeted Design Platform, this kit provides the hardware, software, IP, and Targeted Reference Designs needed to get started right out of the box.

At the heart of the Spartan-6 FPGA DSP Kit is the Avnet AS-LX150T development board featuring the Spartan-6 LX150T device. The Spartan-6 FPGA family offers an optimized balance of connectivity, memory, and DSP hardware resources. As the largest device in the family, the Spartan-6 LX150T FPGA provides more than enough hardware resources for even the most demanding high-volume DSP applications.

With the Spartan-6 DSP Development Kit, system designers spend less time developing the infrastructure of a design and more time building differentiating features into DSP applications. The kit also serves as the starting point for market-specific DSP design platforms with scalable building block architecture, Targeted Reference Designs, and hardware ecosystem of industry-standard FMC daughter card extensions.

FEATURES & BENEFITS

- High-volume DSP applications using Spartan-6 LX150T FPGA with 180 enhanced DSP48E1 slices that deliver up to 50 GMACs of DSP performance
- Develop DSP applications without RTL design experience using System Generator for DSP software with The Mathworks Simulink® and MATLAB® DSP modeling environments
- Targeted Reference Designs supply pre-verified design infrastructure and starting point for DSP development
- Extensible to vertical market applications with two industry-standard FMC connectors and ecosystem of FMC I/O daughter card providers
- Get started quickly with graphical user interface that guides new users on basic kit operation

TECHNICAL SPECS

- Avnet Spartan-6 LX150T development board with the Spartan-6 LX150T FPGA
- ISE® Design Suite: System Edition (device locked to Spartan-6 LX150T FPGA)
- Simulink-based DUC/DDC and RTL-based DUC/DDC Targeted Reference Designs
- Comes complete with cables, power supply, and compact flash
- Downloadable documentation with Hardware Setup and Getting Started Guides

AVAILABILITY

Available starting first quarter of 2010 at: *www.xilinx.com/kits*

Register for more information at: *www.xilinx.com/dsp*

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Medical Imaging, Wireless Communications

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Spartan-6 FPGA Evaluation and Development Kits

Supported Xilinx FPGA/CPLDs: Spartan-6 LX, Spartan-6 LXT

Xilinx and Avnet provide a comprehensive offering of Spartan®-6 FPGA evaluation and development kits that enable designers to achieve an optimum balance of cost, power and performance.

Xilinx® Spartan-6 FPGA SP601 and SP605 Evaluation Kits simplify development of FPGA-based SoCs for consumer, infotainment, video, and other cost or power-sensitive applications. As a Xilinx Base Targeted Design Platform, each kit provides the hardware, software, IP, example designs, and documentation needed to design right out of the box.

The SP601 Evaluation Kit is a low-cost, entry-level environment for evaluating the Spartan-6 FPGA family with system design capabilities that include DDR2 memory control, flash, Ethernet, general-purpose I/O, and UART to name a few. The SP605 Evaluation Kit is a highly scalable base platform for developing low-cost applications requiring connectivity with high-speed serial transceivers, DDR3 memory control, DVI, parallel linear flash, and Tri-mode Ethernet.

Avnet introduces the first-ever battery-powered Xilinx FPGA development board with the Xilinx Spartan-6 LX16 Evaluation Kit, featuring Texas Instruments battery management devices and power regulation circuitry and the Cypress PSoC® 3 Programmable System on Chip with embedded 8051 for an ultra-low-power controller. Avnet also offers the full-featured Xilinx Spartan-6 LX150T Development Kit for designing and verifying applications based on the Spartan-6 LXT FPGA family.

FEATURES & BENEFITS

- Xilinx SP601 and Avnet LX16 Evaluation Kits feature base board with Spartan-6 LX16 FPGA and ISE® WebPACK™ Design Suite (supporting Windows and Linux)
- Xilinx SP605 Evaluation Kit features base board with Spartan-6 LX45T FPGA and ISE Design Suite Logic Edition (device-locked)
- Avnet LX150T Development Kit features base board with Spartan-6 LX150T FPGA and ISE Design Suite Logic Edition (device-locked)
- Base reference design with Gigabit host communication, DDR2/DDR3 interface, and example programmable processing and serial loopback optimized for Spartan-6 FPGAs
- Complete with universal power supply, accessory cables, and downloadable documentation with schematics, Gerber files, board BOM, and detailed user guides

TECHNICAL SPECS

- Xilinx SP601 Evaluation Kit for low-cost Spartan-6 FPGA evaluation
- Xilinx SP605 Evaluation Kit for low-cost connectivity applications
- Avnet LX16 Evaluation Kit for low-power, battery-power applications such as handheld data gathering, human machine interface, and embedded control
- Avnet LX150T Development Kit for PCI Express® bridges, Ethernet/Internet and video applications, and embedded controllers
- All kits feature industry-standard FPGA Mezzanine Card (FMC) connector enabling scaling and customization of base boards for specific application and market needs

AVAILABILITY

Available today at: *www.xilinx.com/kits*

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communcations, Wireless Communications

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Xilinx, Inc.

Spartan-6 FPGA Market-specific Kits

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Spartan-6 LXT

Xilinx® Spartan®-6 FPGA market-specific kits simplify the development of cost and power-sensitive electronics systems, such as digital displays, industrial networking, industrial video processing, automotive infotainment, and broadcast connectivity applications among others.

Spartan-6 FPGA market-specific kits provide all the elements needed to design right out of the box, enabling system designers to accelerate innovation and improve differentiation of lower power 'greener' products. Spartan-6 FPGAs offer an optimal balance of cost, power, and performance for consumer, automotive, surveillance, wireless, and other high-volume markets. They provide twice the capability at half the power consumption of previous generations, while reducing system costs by up to 50 percent.

The first in the series of these market-specific kits is the Spartan-6 FPGA Consumer Video Kit providing a programmable Targeted Design Platform specifically optimized for creating digital TV system designs. This easy-to-use and scalable kit includes a base development board along with several FMC daughter cards, Xilinx and third-party soft IP logic blocks supporting emerging and de facto standard high-speed display interfaces, complete design environment, and Targeted Reference Designs. The kit streamlines algorithm development on Spartan-6 FPGA-based systems and gives systems designers a jumpstart on bringing differentiated products to market quickly.

FEATURES & BENEFITS

- Comprehensive video algorithm development platform with all the hardware, software, firmware building blocks, and tools needed to get started out of the box
- RoHS-compliant boards enable integration of picture quality algorithms with DDR3, DisplayPort 1.1, V-by-One®HS, HDMI 1.3, PCI Express®, 1.05Gb/s LVDS, UART interfaces
- Targeted Reference Designs with DisplayPort 1.1, V-by-OneHS, HDMI 1.3, 1.05Gb/s LVDS, multi-port DDR3 memory controller, UART, SPI, I2C, timers, interrupt controller and on-chip memory
- Multiple examples demonstrate how to customize the video algorithm design and provide best practices for compiling, debugging, and profiling Spartan-6 FPGA-based video applications

TECHNICAL SPECS

- Base development board with Spartan-6 LX150T FG676 device, universal power supply, and accessory cables
- Ecosystem of industry-standard FMC daughter cards for DisplayPort 1.1, HDMI 1.3, V-by-OneHS, and 1.05 Gb/s LVDS (also compatible with Virtex®-6 LXT FPGA)
- ISE® Design Suite Embedded Edition with Platform Studio tools, EDK, and SDK (device locked to Spartan-6 LX150T FPGA)
- USB stick with device driver files, design source files, and applications
- Complete documentation with detailed User Guide

AVAILABILITY

For the latest information on Spartan-6 FPGA market-specific kits as they become available, visit: *www.xilinx.com/kits*

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications

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Virtex-6 FPGA Connectivity Kit

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT

The Xilinx® Virtex®-6 FPGA Connectivity Kit is a comprehensive connectivity development and demonstration platform using the high-performance Virtex-6 LXT FPGA family. As a Xilinx Connectivity Targeted Design Platform, this kit provides the hardware, software, IP, and Targeted Reference Designs needed to create high-speed serial and other connectivity applications right out of the box.

The Virtex-6 LXT FPGA enables designing with PCI Express® 1.1/2.0, Ethernet (GMII, SFP, XAUI), SATA, and other proprietary high-speed serial protocols with line rates up to 6.5Gb/s, as well as multiple parallel standards running at ~ 1.4Gb/s with SelectIO technology.

The Connectivity kit with Virtex-6 LXT FPGA simplifies design, development, and validation of high performance and high bandwidth multi-protocol systems amidst changing market requirements. Production-proven methodologies and tool suites delivered with the kit enable designers to analyze and debug high-speed serial solutions in real time.

The kit jumpstarts development with a Targeted Reference Design that integrates PCI Express and XAUI IP in a working system that accesses on-board DDR3 memory through a virtual FIFO and accelerates bandwidth with an optimized high-performance packet DMA. The kit also serves as a starting point for market-specific targeted design platforms with scalable building block architecture, Targeted Reference Design, and hardware ecosystem of industry-standard FMC daughter card extensions.

FEATURES & BENEFITS

- Comprehensive development platform with all the hardware, software, firmware, application IP and GUI to create a fully functional system solution
- ISE® Design Suite Logic and Embedded Editions tailored for system designers with ChipScope™ Pro Analyzer and Serial IO Toolkit (device locked to Virtex-6 LX240T FPGA)
- Pre-verified, customizable and fully supported Targeted Reference Design for PCIe-10GDMA-DDR3-XAUI
- Multiple example designs including SFI4.1, SFI5, and PCIe 2.0 and 1.1 multi-lane configurations

TECHNICAL SPECS

- RoHS-compliant ML605 base board with Virtex-6 LX240T device
- Universal power supply and accessory cables including CX4 loopback module
- VITA57-compliant FMC daughter card with CX4, SATA, and SMA interfaces
- USB flash drive with device driver files, design source files, and applications
- Downloadable documentation with schematics, Gerber files, board BOM, and detailed user guides

AVAILABILITY

Available today at: *www.xilinx.com/kits*

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communcations, Wireless Communications

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Xilinx, Inc.

Virtex-6 FPGA DSP Kit

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT

The Xilinx® Virtex®-6 DSP Development Kit provides a complete development platform for implementing DSP algorithms on high performance Virtex-6 FPGAs. As a Xilinx DSP Targeted Design Platform, this kit provides the hardware, software, IP, and Targeted Reference Designs needed to get started right out of the box.

The Virtex-6 FPGA DSP Kit features the Xilinx ML605 development board with the Virtex-6 LX240T device. With over 700 DSP48 slices delivering in excess of 400 GMACs of DSP processing bandwidth, this development platform is ideal for high performance wireless communications, aerospace and defense applications.

With the Virtex-6 DSP Development Kit, system designers spend less time developing the infrastructure of a design and more time building differentiating features into DSP applications. The kit also serves as the starting point for market-specific DSP design platforms with scalable building block architecture, Targeted Reference Designs, and hardware ecosystem of industry-standard FMC daughter card extensions.

FEATURES & BENEFITS

- High performance DSP applications using Virtex-6 LX240T FPGA with 788 enhanced DSP48E1 slices that deliver up to 472 GMACs of DSP performance
- Develop DSP applications without RTL design experience using System Generator for DSP software with The Mathworks Simulink® and MATLAB® DSP modeling environments
- Targeted Reference Designs supply pre-verified design infrastructure and starting point for DSP development
- Extensible to vertical market applications with two industry-standard FMC connectors and ecosystem of FMC I/O daughter card providers
- Get started quickly with graphical user interface that guides new users on basic kit operation

TECHNICAL SPECS

- Xilinx ML605 development board with Virtex-6 LX240T FPGA
- ISE® Design Suite: DSP Edition (device-locked to Virtex-6 LX240T FPGA)
- Simulink-based DUC/DDC and RTL-based DUC/DDC Targeted Reference Designs
- Comes complete with cables, power supply, and compact flash
- Downloadable documentation with Hardware Setup and Getting Started Guides

AVAILABILITY

Available starting first quarter of 2010 at: *www.xilinx.com/kits*

Register for more information at: *www.xilinx.com/dsp*

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Medical Imaging, Wireless Communications

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Virtex-6 FPGA Market-specific Kits

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT, Virtex-6 HXT

Xilinx® Virtex®-6 FPGA market-specific kits enable developers to build high-bandwidth and high-performance wireless/wired communications, broadcast, and aerospace/defense electronics systems under tighter design cycles with lower development costs.

Virtex-6 FPGA market-specific kits provide all the elements hardware and software developers need to quickly create and run high performance, compute-intensive applications right out of the box. At up to 50 percent lower power and 20 percent lower cost than previous generations, Virtex-6 FPGAs deliver more computational performance and faster networking capabilities, while lowering system costs through integration.The first in the series of these market-specific kits is the Virtex-6 FPGA Broadcast Connectivity Kit that simplifies serial digital interface (SDI) development for high performance broadcast audio and video applications. The kit provides a Connectivity Targeted Design Platform specifically optimized for the creation of multi-protocol broadcast systems that require high-bandwidth and low-power serial connectivity.

The Virtex-6 FPGA Broadcast Connectivity Kit includes a base development board along with FMC card supporting digital audio and video interfaces and protocol bridging technologies, complete design environment, and Targeted Reference Designs for SDI interfaces based on SMPTE standards with support for multiple channels of SD, HD, and 3G-SDI video in a single Virtex-6 device.

FEATURES & BENEFITS

- Targeted Design Platform tuned to the needs of high performance broadcast audio, video and network connectivity applications
- Enables broadcast equipment engineers to focus on product differentiation rather than challenges of implementing multiple SDI rates and formats
- Out-of-the-box system design with hardware, software, Targeted Reference Designs, evaluation IP, and documentation to shorten development and integration cycles
- Full support for triple rate SDI, AES audio, and video over IP designs with scalable platform for bridging to DVI, PCI Express, DisplayPort, and 10Gb Ethernet standards

TECHNICAL SPECS

- ML605 base board with the Virtex-6 LX240T-1FFG1156 device that includes up to 24 power-optimized high-speed transceivers supporting line rates of up to 6.5Gb/s
- Industry-standard FMC Broadcast Mezzanine Card supporting 4x SD/HD/3G-SDI Tx and Rx, 2x AES3 Tx and Rx, 1x AES10 Tx and Rx, and video sync input
- Two optional reference clock cleaner modules
- ISE® Design Suite: Logic Edition (device-locked to Virtex-6 LX240T FPGA)
- USB flash drive with out-of-the-box demos, Targeted Reference Designs, documentation, and applications

AVAILABILITY

Virtex-6 FPGA Broadcast Connectivity Kit available starting early 2010.

APPLICATION AREAS

Aerospace/Defense, Broadcast, Wired Communcations, Wireless Communications

CONTACT INFORMATION

XILINX

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www.xilinx.com/kits

Xilinx, Inc.

Xilinx Embedded Kits

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Spartan-6 LXT
Supported Architecture: Other - MicroBlaze

Xilinx® Embedded Kits simplify development of embedded processor systems on chip with Virtex®-6 FPGA and Spartan®-6 FPGAs. As Xilinx Embedded Targeted Design Platforms, these kits provide the hardware, software, IP, and Targeted Reference Designs needed to create embedded systems right out of the box.

The Virtex-6 FPGA Embedded Kit is a full-featured environment for developing embedded applications that demand high performance processing, serial connectivity, and advanced memory interfacing. The Spartan-6 FPGA Embedded Kit provides a low-cost base platform for embedded applications requiring connectivity. Both kits come with the MicroBlaze™ Processor Subsystem Targeted Reference Design as a starting point for hardware customization and software development, as well as a video processing design example and detailed tutorial demonstrating how to further customize the system.

For standalone (or bare-metal) software development, an Eclipse-based Software Development Kit (SDK) is provided with GNU tools, wizards for creating software applications and linker scripts, flash writer, standard 'C' libraries and drivers for embedded peripherals. Linux or RTOS-based software development is supported with an ecosystem of third-party operating system and middleware solutions that work seamlessly with the Xilinx SDK.

FEATURES & BENEFITS

- Comprehensive development platforms with all the hardware, software, firmware building blocks, and tools needed to jumpstart application development
- RoHS-compliant boards enable integration of embedded processor subsystem with DDR3, PCI Express®, Gigabit Ethernet, UART interfaces and industry-standard FMC for plug-in scalability
- Targeted Reference Design with MicroBlaze processor, multi-port DDR3 memory controller, Tri-mode Ethernet MAC, UART, SPI, I2C, timers, interrupt controller and on-chip memory
- Multiple examples demonstrate how to customize the design and provide best practices for compiling, debugging, and profiling software applications
- Linux and RTOS support includes PetaLinux OS from PetaLogix, uC/OS-II and uC/TCP-IP ports from Micrium with uC/Probe debug tools and Treck high performance TCP/IP stack

TECHNICAL SPECS

- Virtex-6 FPGA Embedded Kit: ML605 base board with Virtex-6 LX240T FG1156 device, universal power supply, and accessory cables
- Spartan-6 FPGA Embedded Kit: SP605 base board with Spartan-6 LX45T FG484 device, universal power supply, and accessory cables
- ISE® Design Suite Embedded Edition with Platform Studio tools, EDK, and SDK (locked to Virtex-6 LX240T or Spartan-6 LX45T FPGA)
- USB flash drive with out-of-box demos, Targeted Reference Design sources, hardware and software tutorials
- Downloadable documentation with schematics, Gerber files, board BOM, and detailed user guides and datasheets

AVAILABILITY

Virtex-6 FPGA Embedded Kit available today at:
www.xilinx.com/v6embkit

Spartan-6 FPGA Embedded Kit available today at:
www.xilinx.com/s6embkit

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging

CONTACT INFORMATION

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Xilinx FPGA Mezzanine Cards

Xilinx® Targeted Design Platforms enable the creation of world-class electronics for a wide variety of industries with simpler and smarter programmable system platforms. These platforms integrate advanced FPGA silicon technologies, design environments, IP cores, and Targeted Reference Designs with a coordinated set of development boards based on the FPGA mezzanine card (FMC) standard sponsored by VITA.

With the unified board strategy enabled by FMC (VITA57) implementation, Xilinx Targeted Design Platforms are designed for maximum scalability and flexibility. Base boards feature on-board FMC connectors that bring the advantages of standards-based modular design to the FPGA domain. Developers can extend the capabilities of base boards with FMC daughter cards to enable domain and market-specific applications. These efficiencies enable developers to spend less time on application infrastructure and more time on creating unique differentiation. The result is better product offerings for more applications and accelerated deployment of solutions into the marketplace.

Initial FMC offerings from Xilinx and its ecosystem partners include carrier cards for parallel and serial interfaces, video interface circuitry, and general purpose. These work in concert with the Virtex®-6 FPGA ML605 and Spartan®-6 FPGA SP601 and SP605 development boards from Xilinx, as well as carrier cards from Avnet and others. Additional carrier cards and FMC daughter cards will be available soon.

FEATURES & BENEFITS

- Unified board strategy and open platform implementation across all Xilinx Targeted Design Platforms with Virtex-6 and Spartan-6 FPGAs
- Extensible mechanism for rapid development and delivery of domain-specific and market-specific platform kits with ecosystem of base boards and FMC modules
- Increases I/O flexibility and lowers costs across broad range of applications with standard mezzanine card form factor, connectors, and modular FPGA interface
- Simplifies design and integration of specialized IP, components, and FMC daughter card extensions by Xilinx and third-party component and board suppliers

TECHNICAL SPECS

- **Spartan-6 FPGA SP601 base board:** FMC-LPC connector with 68 single-ended or 34 differential user-defined signals
- **Virtex-6 FPGA ML605 base board:** FMC-HPC connector with 8 GTX transceivers and 160 SelectIO™ pins, and FMC-LPC connector with 1 GTX transceiver and 68 SelectIO pins
- FMC Broadcast Mezzanine Card for Virtex-6 FPGA Broadcast Connectivity Kit with support for digital audio and video interfaces and protocol bridging technologies
- FMC Debug Mezzanine Card with support for general-purpose I/O through standard debug headers, Mictor connectors, LEDs, and switches

AVAILABILITY

For availability of Xilinx products with FMC support, visit: *www.xilinx.com/fmc*

For complete list of FMC products from Xilinx ecosystem partners, visit VITA web site at: *http://www.vita.com/fmc.html*

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communcations, Wireless Communications

CONTACT INFORMATION

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Xilinx, Inc.

Xilinx Transceiver Characterization Kits

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT

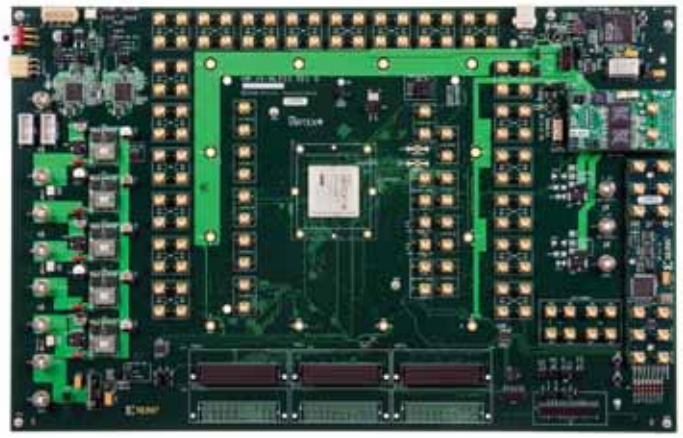
Xilinx® Virtex®-6 FPGA ML623 and Spartan®-6 SP623 Transceiver Characterization Kits simplify the evaluation of Xilinx GTX and GTP low-power, high-speed serial transceivers with the latest generation devices and Xilinx Targeted Design Platforms.

The kits provide hardware and software developers with everything needed to create and fully characterize designs with Virtex-6 FPGA GTX and Spartan-3 FPGA GTP multi-gigabit transceivers, including the ML623 and SP623 characterization boards, ChipScope™ Pro IBERT reference design, PCB design files, and documentation.

The ML623 characterization board features 24 GTX transceivers with high performance Virtex-6 LX240T FPGAs. Virtex-6 FPGA GTX transceivers are ideal for higher bandwidth, low-power connectivity applications with line rates from 750Mb/s to 6.5Gb/s. The SP623 characterization board provides access to 8 GTP transceivers with low-cost, low-power Spartan-6 LX150T FPGAs that offer the lowest risk, lowest cost serial connectivity with line rates from 614Mb/s to 3.125G/ps. Each GTX and GTP transceiver is accessible via four SMA connectors.

FEATURES & BENEFITS

- GTX transceivers offer industry's best signal integrity with eight programmable levels of Transmit Pre-emphasis and four programmable levels of Receive Equalization
- GTP transceivers are power-optimized for 150-180mW per transceiver with programmable Transmit Pre-emphasis and Receive Equalization
- GTX and GTP transceivers are automatically configured with the Xilinx CORE Generator™ software to support different protocols or perform custom configuration



TECHNICAL SPECS

- ML623 characterization board with Virtex-6 LX240T-FF1156 devices
- SP623 characterization boards available with Spartan-6 LX150T-FGG676 devices
- Configured with SystemACE 2G CF card, JTAG, USB to UART bridge and USB host controller, LED displays, and control buttons/switches
- Industry-standard low-pin count FMC connector
- Selectable 1.0V or 1.2V VCCINT jumper cable and 3.3V, 2.5V, 1.8V, and 1.2V power supplies

AVAILABILITY

Both kits available starting first quarter 2010 at: *www.xilinx.com/kits*

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communcations, Wireless Communications

CONTACT INFORMATION

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ADM-XRC-5T2-ADV

Supported Xilinx FPGA/CPLDs: Virtex-5 LXT, Virtex-5 SXT, Virtex-5 FXT

The ADM-XRC-5T2-ADV is a high performance reconfigurable PMC/XMC (PCI Mezzanine Card) based on the Xilinx® Virtex-5 range of Platform FPGAs. The optional fitting of the XMC connector provides 8 High-Speed Serial Links out to the carrier card.

The ADM-XRX-5T2-ADV provides dual JPEG 2000 decoders allowing analysis and filtering of streams of JPEG compressed images.

User connectivity either via the host system or through the external FCN connectors, each provides 4 high speed serial interfaces.

A comprehensive cross platform API with support for Microsoft Windows™, Linux and VxWorks™ provides access to the full functionality of these hardware features.

Product development is aided by the ADM-XRC Software Development Kit. The SDK is a set of resources that assist the creation of applications using Alpha Data's ADM-XRC range of reconfigurable computing hardware. The SDK consists of the example hardware and software applications to ease the development of the user application.. The ADM-XRC SDK is free of charge to all customers who have purchased Alpha Data reconfigurable computing hardware.

Alpha Data has successfully implemented many custom projects. The ultimate option is of course the delivery of a complete, turnkey system to your specification. Contact us to discuss the previous projects we have completed.

Alpha Data have worked closely with Xilinx® for many years and are Xilinx® Diamond XPERT partners. Specialization includes PCI Express®, PCI/PCI-X®, DSP, EDK and MicroBlaze.

FEATURES & BENEFITS

- Dual JPEG 2000 decoder devices
- Multi-platform SDK for system application design
- High Speed Serial I/O Connectivity
- Simple I/O protocol for user design to interface with
- Multiple DMA engines for efficient data transfer between user application and Host system

TECHNICAL SPECS

- Up to 2GBytes of on-board memory
- 8 High Speed Serial Interfaces connected via standard FCN connectors
- Example hardware and software applications provided

AVAILABILITY

Available Now

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Medical Imaging

CONTACT INFORMATION

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Innovative Integration

X3 Family PCI Express Cards cPCI, PCI or XMC

Supported Xilinx FPGA/CPLDs: Spartan-3/3E/3A/3AN, Spartan-3A DSP

The X3 Family PCI Express cards are available on a standard half-height, single slot PCI Express plug-in card with a PCI Express interface or a 3U card with a cPCI interface, or XMC mezzanine module. Intelligent, Customizable I/O, High Performance I/O & FPGA Core. Eliminate custom hardware by harnessing the power of PCI Express & Customizable FPGA.

All X3 family cards utilize the common bus interface to deliver high data throughput to the Host, along with the flexibility of user-customizable FPGA signal processing. Board specific analog or digital I/O flows directly into the user-configurable Spartan 3 logic device. The supplied stock logic functionality allows the board to be used out-of-the-box as high-speed I/O board in which the large onboard RAM is configured as a virtual FIFO, to increase the instantaneous load-carrying capacity of the board to eliminate data overruns/underruns during real-time streaming.

However, using the VHDL source code or MatLab board support package contained within the optional Framework Logic software package, you can readily customize the functionality of the FPGA to include real-time processing such as independent FIR & IIR filters on each channel, real-time FFT processing, ultra-fast feedback & control loops & much more. Use of MatLab/Simulink in conjunction with the supplied MatLab board support package opens an entirely new range of real-solution possibilities.

FEATURES & BENEFITS

- **X3-10M** - 8 simultaneous channels of 25 MSPS 16-bit A/D, and 1.8M FPGA with DSP
- **X3-25M** - (2) 105 MSPS A/Ds, (2) 50 MSPS D/As, Spartan 3A DSP 1.8M FPGA
- **X3-A4D4** (4) 4 MSPS A/Ds, (4) 50 MSPS DACs and 1.8M FPGA with DSP
- **X3-Servo** PCI Express XMC Module - (12) 250 KSPS A/Ds, (12) 2MSPS DACs, 1.8M FPGA with DSP
- **X3-DIO** - LVDS or LVCMOS Digital IO and 1M FPGA with DSP
- **X3-SD** - 16 Channel, 216 KHz, 24-bit Analog Input
- **X3-SDF** PCI Express XMC Module, (4) 24-bit, Fast Sigma-Delta A/D <110 dB, 1M FPGA, 4 MB Memory
- **X3-Servo** - (12) 250 KSPS A/Ds, (12) 2MSPS DACs, 1.8M FPGA with DSP
- **X3-Timing Precision Timing** for Sample Rate Generation and Triggering Controls with GPS-disciplined and 1 PPM Reference Clocks

TECHNICAL SPECS

- Xilinx Spartan3A-DSP or Spartan 3 1-2M Gate FPGA Two 2MB SRAMsPCI Express with <150 MB/s data rates Analog and digital IO integrated with FPGA core Lower Overall Cost
- Industry-standard COTS works with any PCI Express system or host card Add DSP and customize features to meet unique requirements Data buffering supports high rates and large data sets for FFTsFast
- Industry-standard host bus eliminates custom hardware & achieves higher channel counts
  Improve performance with real-time signal processing
- Eliminate custom hardware & simplify system design using intelligent IO and PCI Express
- All cards are also readily installed into Innovative Integration's eInstrument Embedded PC, SBC-ComEx Single-Board Computer, and Andale Data Loggers.

AVAILABILITY

Now!

APPLICATION AREAS

Aerospace/Defense, Broadcast, Industrial Automation, Medical Imaging, Motor Control, Wireless Communications

CONTACT INFORMATION

Innovative Integration
... real time solutions!

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X5 Family PCI Express cPCI, PCI, or XMC

Supported Xilinx FPGA/CPLDs: Virtex-5 SXT, Virtex-5 FXT

The X5 family integrates high performance I/O with a Xilinx Virtex5 FPGA computing core. Available on a standard half-height, single slot PCI Express plug-in card with a PCI Express interface or a 3U card with a cPCI interface, or XMC mezzanine module. Intelligent, Customizable I/O, High Performance I/O & FPGA Core.

Innovative's unique architecture provides high performance data streaming to the host that is flexible & extensible for all types of applications. It's fast & easy to use – allowing you to concentrate on your application work because it handles all the data flow & routing. You can freely mix high rate data streams with control & status making it easy to adapt to your application, yet still achieve the full GB/s data rate capabilities of the PCIe interface.

All X5 cards are architected to deliver high data throughput to the Host, along with the flexibility of user-customizable FPGA signal processing.

Board specific analog or digital I/O flows directly into the user-configurable Xilinx 5 logic device. The supplied stock logic functionality allows the board to be used out-of-the-box as high-speed I/O board in which the large onboard DDR2 DRAM is configured as an enormous virtual FIFO, to dramatically increase the instantaneous load-carrying capacity of the board to eliminate data overruns/underruns during real-time streaming.

FEATURES & BENEFITS

- **X5-400M** - Two 400 MSPS, 14-bit TI ADS5474 ADCs and Two 500 MSPS, 16-bit DACs, Virtex5 FPGA and 512 MB Memory
- **X5-COM** - Four Ethernet/SRIO/Gigabit Serial Ports, Virtex5 SXT or FXT FPGA and 512MB Memory
- **X5-GSPS** - Two 8-bit National ADC08D1500 A/Ds, Virtex5 FPGA and 512 MB Memory
- **X5-TX** - Four 500 MSPS or Dual 1 GSPS, 16-bit DACs, Virtex5 FPGA with 512MB DDR2 DRAM and 4 MB QDR SRAM Memories
- **X5-G12** - Dual channel 1 GSPS,12-bit Digitizer, Virtex5 FPGA and 512MB Memory
- **X5-210M** - Four 250 MSPS 14-bit A/Ds, Virtex5 FPGA, and DDR2/QDR-II Memory
- **X5-RX** - Four 200 MSPS 16-bit A/Ds, Virtex5 FPGA, 512MB DRAM/ 4MB SRAM
- Modules are also readily installed into Innovative Integration's eInstrument Embedded PC, SBC-ComEx Single-Board Computer, and Andale Data Loggers.

TECHNICAL SPECS

- MATLAB and RTL tools in the FrameWork Logic Board Support Packages enable you to customize the X5 modules for your application requirements
- Compact IEEE 1386 card format (75x150mm), Integrate into any VITA 42.3 PCI Express system, <30 GMACs/s (SX95T) integrated with memory blocks and logic, Real-time memory performance to 4 GB/s for FPGA data buffering and computation
- <1GB/s transfer rates to host eliminates custom hardware requirementsReal-time signal processing integrated with the IOTight, real-time host card integration with Serial RIO, Aurora & custom protocols
- PCI Express, 8 lane interface, Analog and Digital IO integrated with FPGA, <1 GB/s dedicated secondary host interface

AVAILABILITY

Now!

APPLICATION AREAS

Aerospace/Defense, Broadcast, Industrial Automation, Medical Imaging, Wireless Communications

CONTACT INFORMATION

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Xilinx, Inc.

Virtex-6 FPGA ML605 Evaluation Kit

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT

The Xilinx® Virtex®-6 FPGA ML605 Evaluation Kit provides a development environment for system designs that demand high performance, serial connectivity and advanced memory interfacing. As a Xilinx Base Targeted Design Platform, the kit provides all the hardware, software, IP and targeted reference designs needed to design right out of the box

The ML605 Evaluation Kit simplifies development of systems-on-chip (SoC) for wired telecommunications, wireless infrastructure, broadcast, and other high performance applications. Integrated tool suites streamline creation of elegant solutions to complex design requirements. Multiple pre-verified targeted reference designs jumpstart development. Industry-standard FPGA Mezzanine Card (FMC) base boards and daughter card extensions provide plug-in scaling and customization.

The ML605 Evaluation Kit with Virtex-6 LX240T FPGA enables 50 percent lower power and 20 percent lower cost designs than previous generations. System-level capabilities include built-in high-speed serial transceivers, PCI Express® 2.0 Endpoint blocks, and DDR3 memory control to name just a few.

The kit is also supported by mainstream industry standard peripherals, such as PCI Express x8 edge connector (version 1.1 and 2.0), Tri-mode Ethernet, DDR-3 SO-DIMM, BPI linear flash, USB 2.0 (host and device), DVI output, SFP, LCD character display, GTX port (TX, RX) with four SMA connectors and two VITA-57 compliant FMC connectors.

FEATURES & BENEFITS

- Full-featured FPGA evaluation board with x8 PCI Express and standalone form factor
- ISE® Design Suite: Logic Edition tailored for logic and connectivity designers (Device-locked to Virtex-6 LX240T FPGA)
- Base reference design with Gigabit Ethernet, DDR3, DSP, and serial loopback
- Pre-verified demonstrations for PCI Express 2.0 x4 , PCI Express 1.1 x8, DDR3, ChipScope™ Pro Serial IO Toolkit IBERT transceiver test, and board diagnostic

TECHNICAL SPECS

- Virtex-6 FPGA ML605 board with Virtex-6 LX240T-1FFG1156 device, universal power supply, and accessory cables
- Communication and networking ports for PCI Express, Tri-mode Ethernet, USB 2.0, SFP, FMC, and SMA
- Supported by BPI Liner Flash and DDR3 memory
- Downloadable documentation with schematics, Gerber files, board BOM, and detailed user guides

AVAILABILITY

Available today at: *www.xilinx.com/ml605*

APPLICATION AREAS

Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communcations, Wireless Communications

CONTACT INFORMATION

XILINX

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www.xilinx.com/ml605

Wireless IP Cores for Software Digital Radio Applications

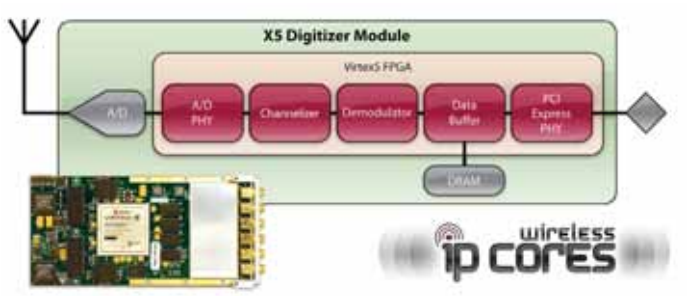
Supported Xilinx FPGA/CPLDs: Virtex-5 LXT, Virtex-5 SXT, Virtex-5 FXT

The Wireless IP Cores for Software Digital Radio Application products offer a range of capabilities for both narrowband & wideband receiver applications from 16 to 4096 channels with sampling rates up to 400 MSPS and over 90 dB dynamic range. The 16 & 32 channel cores are more flexible & adaptable than the higher channel density cores, providing independently programmable features for tuning, decimation, filtering & gain control making these products ideal for multi-protocol applications. The 256 channel tunable channelizer and 4096 equi-space channel cores provide a very high number of channels for cellular test equipment, surveillance, & satellite communications applications.

The IP cores are implemented on Innovative's X5-400M, a PCI Express XMC module with Xilinx Virtex5 SX95T & dual channel 400 MSPS digitizers. System designers can buy the X5-400M card pre-configured with the receiver IP of their choice ready to use. These new products based on Virtex 5 & PCI Express offer system designers a variety of COTS SDR receiver solutions with the latest technologies. They offer a lower overall system cost per channel & reduced development risk, while providing a flexible platform for adopting new & evolving standards for the future. Download data sheets & pricing now at *www.innovative-dsp.com*

FEATURES & BENEFITS

- **IP-RI-MDDC16** - 16 ind. ch. of DDC with prog. gain & 121 tap pulse filters
- **IP-RI-MDDC32** - 32 ind. ch. of DDC with prog. gain & 121 tap pulse filters
- **IP-RI-CHTU128/256** - 128 or 256 channelizer with prog. tuning, gain & ch. filtering
- **IP-RI-CHTU32/4096** - 32 to 4096 channelizer with fixed, equi-spaced channels
- **IP-PSK-DEMOD** - Demodulator for BPSK, QPSK, OQPSK, and 8-PSK data with carrier tracking
- **IP-TINY-DDS** - Small footprint Programmable Direct Digital Synthesizer with 90 dB SFDR
- **IP-RI_FRU** - High resolution fractional resampler



TECHNICAL SPECS

- Modern PCI Express interface also dramatically improves system data transfer rates, enabling higher channel data rates and new features such as logging raw digitized data at full rate.
- Receiver IP cores are available in netlist or source form for custom applications Innovative's X5 FrameWork Logic Tools allow developers using RTL & MATLAB to rapidly integrate the SDR cores into their application logic.
- Full simulation models for the receiver and hardware IP provide comprehensive support for signal processing design and hardware integration
- MATLAB Simulink tools support end-to-end simulation of the receiver channel & give a complete verification of the signal processing, including the capability to go directly into hardware while using MATLAB for debug & verification.
- The X5 digitizers are state-of-the-art high performance front ends for wireless, RADAR, and medical applications on an industry-standard XMC (VITA 42.3) PCI Express module.

AVAILABILITY

Shipping now.

APPLICATION AREAS

Broadcast, Industrial Automation, Medical Imaging, Wireless Communications

CONTACT INFORMATION

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... real time solutions!

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SoftJin Technologies Pvt. Ltd.

IP Cores for FPGA based Applications

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT, Virtex-6 HXT, Virtex-5 LX, Virtex-5 LXT, Virtex-5 SXT, Virtex-5 FXT, Virtex-5 TXT, Virtex-4 LX, Virtex-4 SX, Virtex-4 FX, Spartan-6 LX, Spartan-6 LXT, Spartan-3/3E/3A/3AN, Spartan-3A DSP

SoftJin Technologies provides Design IP cores, IP customization services and IP based system development services for various FPGA based applications, with special focus on the audio/ video and communication domain applications such as TV, set-top box, DVB modulator/ demodulator, personal video recording.

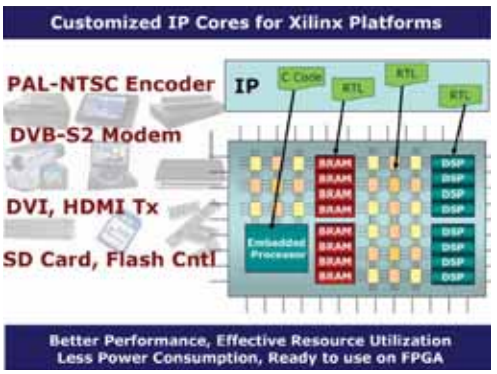
The key IPs in SoftJin's portfolio includes:

- **Audio/ Video Processing:** PAL-NTSC-SECAM Encoder, HD Encoder, DVI/HDMI Transmitter, VGA Controller, Graphics LCD, Speech Codec, I2S, S/PDIF, 24-bit Audio Processor
- **Image Processing:** JPEG Encoder/Decoder, Edge Detection, Dilation/Erosion, Median Filter
- **Digital Video Broadcasting:** DVB-S2 compliant LDPC Codec, DVB-S2 compliant BCH codec, PSK modulator/ demodulator
- **Memory Controller:** SD Card controller, NAND Flash controller, Static RAM Controller
- **Encryption/ Decryption:** AES , MD5, SHA
- **Interfaces:** I2C, SPI, RS232, USB-FPGA host/peripheral interface, PS/2 interface
- **DSP:** FFT, DCT, FIR, Matrix multiplier, IEEE floating point add/sub/multiply

SoftJin offers the IP cores under source code (both RTL and C code) licensing as well as FPGA Netlist licensing targeted for particular FPGA device.

FEATURES & BENEFITS

- SoftJin provides **IP customization services** to achieve better speed and efficient resource utilization on a particular FPGA device by various techniques like usage of hard macros (multiplier/ DSP slices), architecture specific PLL/ clock manager configuration, tool flow specific annotation in RTL code as well as in configuration file and tuning of parameters for synthesis, P&R according to the target application.
- SoftJin provides **system development services** by reusing SoftJin's or third party IPs. This includes system level design, HW-SW partitioning, co-simulation and co-verification, RTL development and verification, FPGA implementation, Schematic engineering, Layout engineering and prototype PCB manufacturing.
- SoftJin also provides **system optimization services** by virtual prototyping (SystemC), algorithmic optimization, performance/cost/ risk analysis at system level.



- SoftJin provides firmware, driver application which can be integrated with the hardware to build complete working system.

TECHNICAL SPECS

- **PAL-NTSC-SECAM Encoder:** Supports BT601/ BT656/ RGB/ YUV inputs and generates output video in NTSC(M)/ PAL(B,D,G,H,I)/ PAL (M)/ PAL(N)/ SECAM standards. Supports RGB/ YUV/ S-Video/Composite output video formats. It has programmable luma and chroma filters and luma delay.
- **JPEG Encoder:** Supports baseline ISO/IEC 10918-1 standard. It has 8x8 two dimensional fixed point DCT and configurable Huffman and Quantization table.
- **DVB-S2 LDPC Decoder:** Supports both normal (64800) and short (16400) frame lengths. It also supports all code rates (1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10) and programmable iteration length.
- **DVB-S2 BCH Decoder:** It is compatible with all code and data rate and has provision for changing code rate dynamically. It supports both error and erasure decoding.
- **SD Card Controller:** It meets SD physical layer specification version 2.0. It supports standard SD card memory, and SDHC.

AVAILABILITY

Now

APPLICATION AREAS

Broadcast, Consumer, Data Processing and Storage, Wired Communcations, Wireless Communications

CONTACT INFORMATION

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www.softjin.com

ISE Design Suite

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT, Virtex-6 HXT, Virtex-5 LX, Virtex-5 LXT, Virtex-5 SXT, Virtex-5 FXT, Virtex-5 TXT, Virtex-4 LX, Virtex-4 SX, Virtex-4 FX, Spartan-6 LX, Spartan-6 LXT, Spartan-3/3E/3A/3AN, Spartan-3A DSP, Spartan-3 XA, Spartan-II/E, CoolRunner, XC9500/XL/ XV

The ISE® Design Suite is truly the next-generation in Xilinx FPGA design environments, delivering fully interoperable domain-specific design flows and tool configurations for logic, digital signal processing, embedded processing, and system-level design.

Simpler, smarter design methodologies for creating system-on-chip solutions with Xilinx® Targeted Design Platforms enable designers ranging from the push-button user to the ASIC designer to achieve the ultimate in productivity, fastest design completion, and optimal quality of results.

The ISE Design Suite is easy to use with seamless interoperability between all configurations and inter-tool communication within design flows. Tight connection between embedded and DSP flows further simplifies integration of embedded, DSP, IP, and custom blocks into one system. In this way, ISE users can work with the design language and at the design abstraction of their choice. The design language may vary from VHDL/ Verilog to C, C++ or MATLAB® software from The Mathworks. Likewise, design abstraction moves from the block to component and system level.

The result is a complete flow spanning design creation, design implementation, and design verification that is tailored to the way designers work. This approach delivers breakthrough productivity, power, and performance advantages with the latest generation Virtex®-6 and Spartan®-6 FPGAs and Xilinx Base Targeted Design Platform.

FEATURES & BENEFITS

- **ISE Design Suite:** Logic Edition offers a complete front-to-back RTL design environment for Xilinx FPGAs
- **ISE Design Suite:** Embedded Edition delivers an integrated software solution for designing embedded processing systems
- **ISE Design Suite:** DSP Edition provides flows and IP tailored to the needs of algorithm, system, and hardware developers
- **ISE Design Suite:** System Edition is fully integrated software environment supporting logic/connectivity, embedded, and DSP design methodologies

- All Editions provide foundation IP and Xilinx exclusive tools and technologies, including PlanAhead™ Design and Analysis, ChipScope™ Pro Analyzer and Serial IO Toolkit, and SmartGuide™ technology

TECHNICAL SPECS

- ISE Foundation™ with the ISE Simulator offers front-to-back design flow for design entry, synthesis, implementation, verification, and device programming
- DSP and System Editions additionally include System Generator for DSP design suite and DSP-specific-IP portfolio
- Embedded and System Editions provide Platform Studio tools, Embedded Development Kit, Software Development Kit, embedded-specific IP and device drivers including Xilinx MicroBlaze™ soft processor

AVAILABILITY

Shipping today. Full-featured 30-day evaluation version available for immediate download at no charge.

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communcations, Wireless Communications

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Synopsys

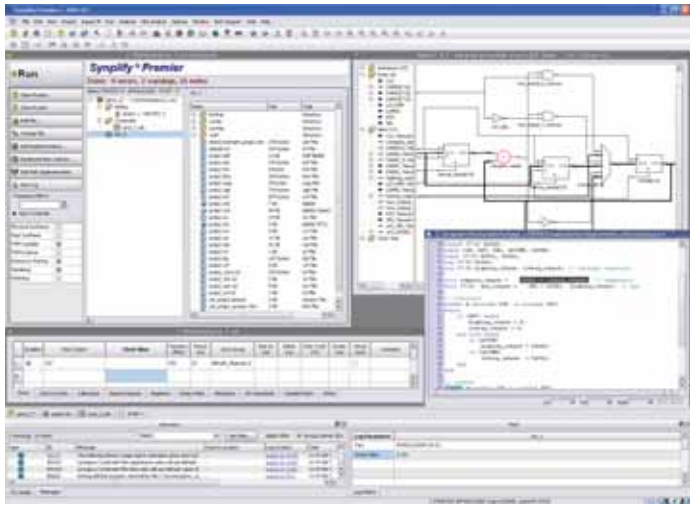
Synplify Premier, FPGA Implementation and Debug

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT, Virtex-6 HXT, Virtex-5 LX, Virtex-5 LXT, Virtex-5 SXT, Virtex-5 FXT, Virtex-5 TXT, Virtex-4 LX, Virtex-4 SX, Virtex-4 FX, Virtex-II Pro, Virtex-II, Spartan-6 LX, Spartan-6 LXT, Spartan-3/3E/3A/3AN, Spartan-3A DSP, Spartan-3 XA, Spartan-II/E, CoolRunner, XC9500/XL/ XV

Synopsys' Synplify Premier Solution is the industry's ultimate FPGA implementation and debug environment. It provides a comprehensive suite of tools and technologies for advanced FPGA designers as well as ASIC prototypers targeting single FPGA-based prototypes. The Synplify Premier software is a technology independent solution that addresses the most challenging aspects of FPGA design including timing closure, logic verification, IP usage, ASIC compatibility, DSP implementation, debug and tight integration with FPGA vendor back-end tools. The Synplify Premier software provides in-system verification of FPGAs, dramatically accelerates the debug process, and provides a rapid and incremental method for finding elusive design problems. For more information on Synplify Premier and other Synopsys FPGA implementation tools, visit us at *www.synopsys.com/fpga*.

FEATURES & BENEFITS

- **ASIC verification using FPGAs:** Synplify Premier is the most comprehensive system for implementing FPGA-based prototypes of ASICs and ASSPs including gated clock conversion and DesignWare support.
- **Integration with high level synthesis for DSP:** Synplify Premier allows FPGA designers to rapidly explore and implement DSP algorithms in a range of FPGA architectures and vendors from a single model.
- **Fastest time-to-results for complex FPGAs:** Unique timing-driven and graph-based physical synthesis technologies enable designers to reach aggressive timing goals in the shortest amount of time.
- **Area optimization for cost reduction:** Synplify Premier can reduce the logic required to achieve required performance, allowing the design to fit in the smallest, least expensive part possible.
- **Powerful design analysis and debug:** Analyze and debug in RTL. Instantly see a high-level graphical representation of the design that is linked back to the source code that produced it.



TECHNICAL SPECS

- Comprehensive language support including Verilog, VHDL, System Verilog and mixed-language
- Supports Windows 2000, XP Pro, Server 2003, and Vista
- Supports Linux, RHEL3, RHEL4, RHEL5, and SLES9 (32/64 bit)
- Supports Solaris Sparc 8, 9, and 10
- Minimum hardware requirements: CPU 1 GHz speed or better, RAM 512Mb, HDD 200Mb free space

AVAILABILITY

Synopsys' Synplify Premier FPGA implementation software is available now. Request an evaluation at *www.synopsys.com/fpga*

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communcations, Wireless Communications

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www.synopsys.com/fpga

CoWare SPW Xilinx® Implementation Flow

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT, Virtex-6 HXT, Virtex-5 LX, Virtex-5 LXT, Virtex-5 SXT, Virtex-5 FXT, Virtex-5 TXT, Virtex-4 LX, Virtex-4 SX, Virtex-4 FX, Spartan-6 LX, Spartan-6 LXT, Spartan-3/3E/3A/3AN, Spartan-3A DSP, Spartan-3 XA, Spartan-II/E, CoolRunner, XC9500/XL/ XV

CoWare® SPW accelerates the design of complex, digital signal processing (DSP) systems. Its efficient creation of complex DSP system models and extremely fast simulation makes SPW the premier choice for today's complex, multi-standard designs in the wireless and satellite communications market. CoWare SPW is deployed at leading network operators, consumer and Mil/Aero OEMs as well as in many semiconductor companies. It has been in production use for more than 20 years.

SPW enables designers to quickly capture the target product algorithms as well as the environment of the target system. Over 4000 proven library blocks are available in the SPW libraries, starting with basic DSP functions, and communication system design blocks up to complete wireless standards reference libraries for standards like GSM, WCMDA and LTE. All library blocks are provided in source giving the designer unmatched value for understanding the system behavior. The industry's fastest simulator leverages server farms for exploring many design alternatives as well as multi-threaded simulation on multi-core servers for speeding up individual investigations. Co-simulation with MATLAB® functions and providing results into MATLAB allow smooth transition from initial algorithm studies into design of actual products with SPW. Powerful, yet very easy to use analysis capabilities allow for complex post-processing of simulation results. SPW has a multi-million gate design-proven implementation path that supports both diagram-based RTL generation as well as direct translation from C-models into RTL code. This is now fully integrated with the Xilinx® ISE® flow.

FEATURES & BENEFITS

- Fastest data-flow simulator supporting regression on server farms for structured exploration of target design in the system context
- Multi-threaded simulation on multi-core hosts for rapid, interactive system exploration
- DSP implementation library including hierarchical FSM capabilities, proven in hundreds of ASIC designs now available for the Xilinx® flow
- Direct translation from C to RTL allowing efficient system modeling while greatly speeding RTL creation

- Automated test bench creation and cosimulation with Mentor Modelsim before and after place & route enables seamless verification flow
- Native C-based analysis scripts and results visualization provide maximum flexibility in system performance analysis and parameter specifications for DSP blocks
- MATLAB models execute in SPW through an efficient, automatically created interface to the MATLAB engine. Results can also be written into a MATLAB data base

SYSTEM REQUIREMENTS

- Microsoft Windows XP Professional, Service Pack 2 and Microsoft Visual C++ 2008 Express Edition
- Red Hat Enterprise Linux 4.0 WS Update 4, gcc 4.1.2

AVAILABILITY

Q1- 2010

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communcations, Wireless Communications

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Lauterbach

TRACE32-PowerTools

Supported Xilinx FPGA/CPLDs: Virtex-5 LX, Virtex-5 LXT, Virtex-5 SXT, Virtex-5 FXT, Virtex-5 TXT, Virtex-4 LX, Virtex-4 SX, Virtex-4 FX, Virtex-II Pro, Virtex-II, Spartan-3/3E/3A/3AN, Spartan-3A DSP, Spartan-3 XA

TRACE32 comprises a complete set of development and testing tools for the MicroBlaze, PowerPC PPC405, PPC440 and ARM Cortex processor IP. The modularity of TRACE32-PowerTools allows the user to extend the debugger with a trace extension and logic analyzer tools. The trace extension provides full support for program flow and data trace. In the context of FPGA system TRACE32-PowerTools enables the Xilinx ChipScope analyzer to access the target via the Lauterbach debug interface, fully parallel with an ongoing debugging session.

It also allows to configure the FPGA via the debugger and thus obviates the need for dedicated programming cables.

TRACE32 works with a high variety of host interfaces. The communication link to the host is done by USB or Ethernet, allowing a high-speed data transfer. It is possible to share TRACE32 tools in a LAN of PCs and workstations.

TRACE32-PowerTools are controlled by TRACE32-PowerView, a powerful IDE allowing HLL debugging on C or C++ level. It supports all third party compilers. TRACE32-PowerView allows unlimited software breakpoints and also supports the on-chip hardware break- and watchpoints. A fast flash programming utility is included. The comfortable graphical user interface is completely configurable by the user. No other system offers more flexibility.

FEATURES & BENEFITS

- Interface to all compilers for C/C++
- RTOS awareness
- FLASH programming utility
- Cache debugging and MMU support
- Trace extension up to 550 MHz and 4 GByte trace memory

TECHNICAL SPECS

- Download speed up to 5 MByte/s
- Display of internal and external peripherals at a logical level (peripheral browser)
- Powerful script language
- High-speed link via Ethernet or USB
- Universal hardware for all supported debuggers

AVAILABILITY

All products are available.
More information can be found under:
http://www.lauterbach.com/pro_xilinx.html

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communcations, Wireless Communications

CONTACT INFORMATION

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www.lauterbach.com

Aldec Active-HDL

Comprehensive FPGA design, simulation, and verification environment

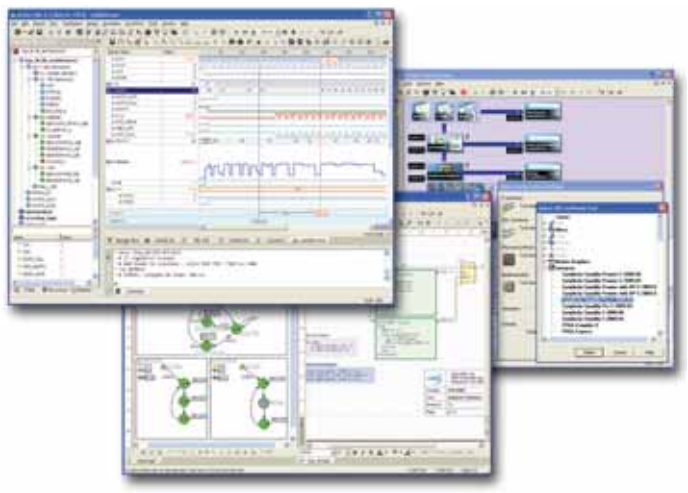
Xilinx® FPGA devices are everywhere in electronic design due to their flexibility and time to market advantages. With these advantages comes the challenge of designing, validating, and implementing the increasingly complex logic for these programmable devices. Aldec® Active-HDL™ is the digital design and simulation tool with all the capabilities necessary for an FPGA designer to successfully develop and validate FPGAs.

This RTL and gate-level simulator operates at fast simulation run times and supports single or mixed language IEEE VHDL1076 (1987-2008), IEEE Verilog® 1364 (1995-2005), and IEEE SystemVerilog 1800-2005 (Design Std.) HDL designs.

Extensive project management tools help track design progress and interface with FPGA vendor tools, allowing the user to design through a single user interface. The multi-vendor FPGA Design Flow Manager controls simulation, synthesis, and implementation for industry-leading Xilinx FPGA devices and over 80 other popular EDA tools. The Revision Control Interface allows operation on subsequent versions of a design and revisions of design source files directly from the Active-HDL environment. In addition, design teams can track changes made to a design, view differences between multiple versions of source files, and recover previous file versions at any time.

FEATURES & BENEFITS

- Multiple Design Entry Tools
- High-Speed RTL and Gate-Level Simulator
- IEEE VHDL, Verilog, SystemVerilog (Design), SystemC
- Advanced Debugging
- Code Coverage
- Xilinx® SecureIP and IEEE IP Encryption
- Assertion-Based Verification (ABV)
- DSP Co-Simulation with MATLAB®/Simulink®
- PCB Design Interface
- Design Documentation Export
- Microsoft® Windows® 7/Vista/XP/2003 – 32/64 Bit Support



About EMA Design Automation

EMA Design Automation offers leading product development solutions including electrical CAD and mechanical CAD tools, a complete range of product lifecycle management systems, consulting services, training, and technical support. EMA is a Cadence® Channel Partner serving all of North America, an Autodesk® Authorized Value Added Reseller, and is an Authorized North American Distributor of Aldec Active-HDL. EMA manufactures the Component Information Portal™, TimingDesigner®, and CircuitSpace™, and all are distributed through a worldwide network of value added resellers. EMA is a privately held corporation headquartered in Rochester, New York. Visit EMA at www.ema-eda.com for more information.

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Aldec® Corporation

Aldec Verification

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT, Virtex-6 HXT, Virtex-5 LX, Virtex-5 LXT, Virtex-5 SXT, Virtex-5 FXT, Virtex-5 TXT, Virtex-4 LX, Virtex-4 SX, Virtex-4 FX, Virtex-II Pro, Virtex-II, Spartan-6 LX, Spartan-6 LXT, Spartan-3/3E/3A/3AN, Spartan-3A DSP, Spartan-3 XA, Spartan-II/E, CoolRunner, XC9500/XL/ XV

Xilinx SecureIP and Encrypted IP

Aldec Simulators compile and simulate leading source-level encrypted Xilinx SecureIP, and the latest IEEE VHDL 2008 and IEEE Verilog 2005 encrypted IP. Aldec products may be used with today's most popular IP Cores such as: PCIe, RocketIO™ Transceivers, SERDES, EMAC, TEMAC and SWIFT SmartModels.

Xilinx EDK Integration

Aldec Simulators provide an option for integration with Xilinx EDK tools used to develop microprocessor systems within Xilinx FPGA devices. Based on the EDK simulation script, the simulator adds all necessary EDK sources to its own project files, and is simulated as any other simulation.

Assertion-Based Verification (ABV)

Aldec Simulators are ABV enabled and support three Assertion types: IEEE 1800 SystemVerilog Assertions (SVA), Property Description Language (PSL) and Open Vera Assertions (OVA).

DSP/HDL Design and Simulation

The Aldec Solution interfaces to The Mathworks™ MATLAB® and Simulink® products, and solves key HDL "Pain-points" for DSP designers, including: DSP/HDL co-design system viewer/editor, HDL Block/Black Box and IP Core support, DSP design conversion to pure HDL, fast mixed language RTL and gate-level co-simulation and pain-free verification of pure HDL code that operates at optimum performance.

DO-254 Compliance

Aldec offers a DO-254/ED-80 FPGA Verification Compliance solution. Aldec DO-254/CTS™ supports the "Design Assurance Guidance for Airborne Electronic Hardware" (DO-254/ED80) chapter 6.2 "Verification Process" assurance levels A-D; and Chapter 11.4 "Tool Assessment and Qualification Process". DO-254/CTS is a patented solution (US Patent 5,479,355).

About Aldec

Aldec® Corporation is an industry-leader and offers a patented technology suite including: RTL Design, RTL Simulators, Hardware-Assisted Verification, Design Rule Checking, IP Cores, DO-254 Functional Verification and Military/Aerospace solutions. Aldec is "The Design Experts Choice" for over 30,000 Design Engineering experts worldwide.

PRODUCT FEATURES & BENEFITS

- **Active-HDL™**
  The Windows® FPGA Simulator of Choice
  - HDL Design Tools
  - Mixed-language RTL Simulation
  - VHDL, Verilog®, SystemVerilog (Design), SystemC/C/C++
  - Xilinx SecureIP and IEEE IP Encryption
  - Advanced Debugging & Code Coverage
  - Assertion-Based Verification (ABV)
  - Windows® 7/Vista/XP/2003

- **Riviera-PRO™**
  Advanced System-Level Simulation and Debugging
  - Fast RTL, gate and system-level Simulation
  - VHDL, Verilog®, SystemVerilog, SystemC/C/C++
  - Advanced Verification Inside™ (ESL, ABV, TLM, OVM and VMM)
  - Accelerated Waveform Viewer
  - Code Coverage Tools
  - DSP Co-Simulation with MATLAB® and Simulink®
  - Linux and Windows® 32/64 bit support

- **ALINT™**
  Fast Design Closure™
  - HDL Design Rule Checker
  - VHDL, Verilog and Mixed-Language support
  - Integrated Results Analysis and Debugging
  - VHDL and Verilog Rule Plug-in
  - DO-254 Rule Plug-in
  - User-defined Design Rules
  - Linux and Windows® 32/64 bit support

- **DO-254/CTS™**
  DO-254 FPGA Verification Compliance
  - Software, Hardware, Analysis and Documentation
  - At-Speed Design Verification
  - Independent EDA Tool Assessment
  - Custom Engineering Development Services

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Neoventus Design Group, LLC

Providing Solutions & Support in Your Extended Engineering Ecosystem

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT, Virtex-6 HXT, Virtex-5 LX, Virtex-5 LXT, Virtex-5 SXT, Virtex-5 FXT, Virtex-5 TXT, Virtex-4 LX, Virtex-4 SX, Virtex-4 FX, Virtex-II Pro, Virtex-II, Spartan-6 LX, Spartan-6 LXT, Spartan-3/3E/3A/3AN, Spartan-3A DSP, Spartan-3 XA, Spartan-II/E, CoolRunner, XC9500/XL/ XV

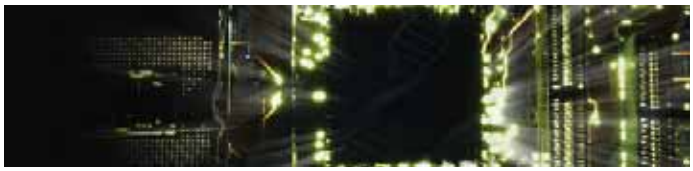
Neoventus Design Group is an engineering services company with core competencies in FPGA development and high speed digital circuit design. Drawing on several decades of experience, Neoventus engineers deliver custom design collateral meeting our clients' requirements on time and on budget. Our engineers have developed scores of custom IP targeting Virtex, Spartan, CoolRunner, and XC9500 devices. For system-on-chip (SOC) designs, Neoventus leverages Xilinx's EDK and SDK tools to develop applications based on a MicroBlaze or PowerPC microprocessor cores.

Neoventus is small, nimble, and employee owned, so we have a vested interest in fostering a solid customer relationship by providing quality engineering services with a responsive work ethic and a sense of project ownership. Our background is diverse with design experience covering medical, industrial, and commercial applications. We understand the challenges of a rugged environment and meeting stringent industry standards. We are senior engineers who can take on the development of an entire project or serve in a support role responsible for a piece of the puzzle.

For companies finding themselves temporarily short staffed or in need of additional design resources, Neoventus Design Group is ready to serve as your extended engineering team.

FEATURES & BENEFITS

- Neoventus offers a team of experienced engineers capable of rapid prototyping for proof of concept analysis and schedule driven product development for quick time to market.
- Custom IP development sourced in HDL. Custom IP can be standalone or designed to function as a peripheral to an embedded processor (PPC, MicroBlaze, PicoBlaze or third party core). Designs are fully simulated, synthesized, and fit to the target device.
- Complete embedded system design including hardware and firmware development.



Endless Solutions — One Company

- Through relationships with companies specializing in mechanical design and mathematical analysis & modeling, Neoventus can offer its clients full turnkey solutions.
- Neoventus works closely with contract manufactures (CM) to optimize the fabrication and assembly process with sound DFM/DFT techniques. This, and a relationship with an off shore CM, leads to the lowest possible per unit product cost.

SERVICES

- FPGA Development
- Hardware Design & PCB Layout
- Firmware Development
- Market Segment Experience
  - Industrial
  - Medical
  - Military
  - Design for EMC Compliance (CISPR II, IEC61000-4)
  - Extensive DFM/DFT
- Development Tools
  - Xilinx ISE, EDK, SDK, Plan Ahead, DSP, ChipScope
  - Aldec Active-HDL
  - IAR Embedded Workbench
  - Mentor Graphics DxDesigner, PADS

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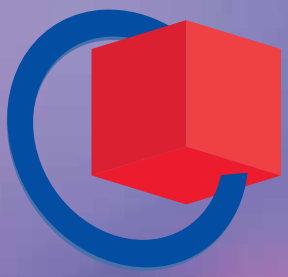
Nuremberg, Germany

March 2 – 4, 2010



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