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Trends to Watch in the Evolution of Programmable Logic

Dual-Architecture FPGAs Provide New
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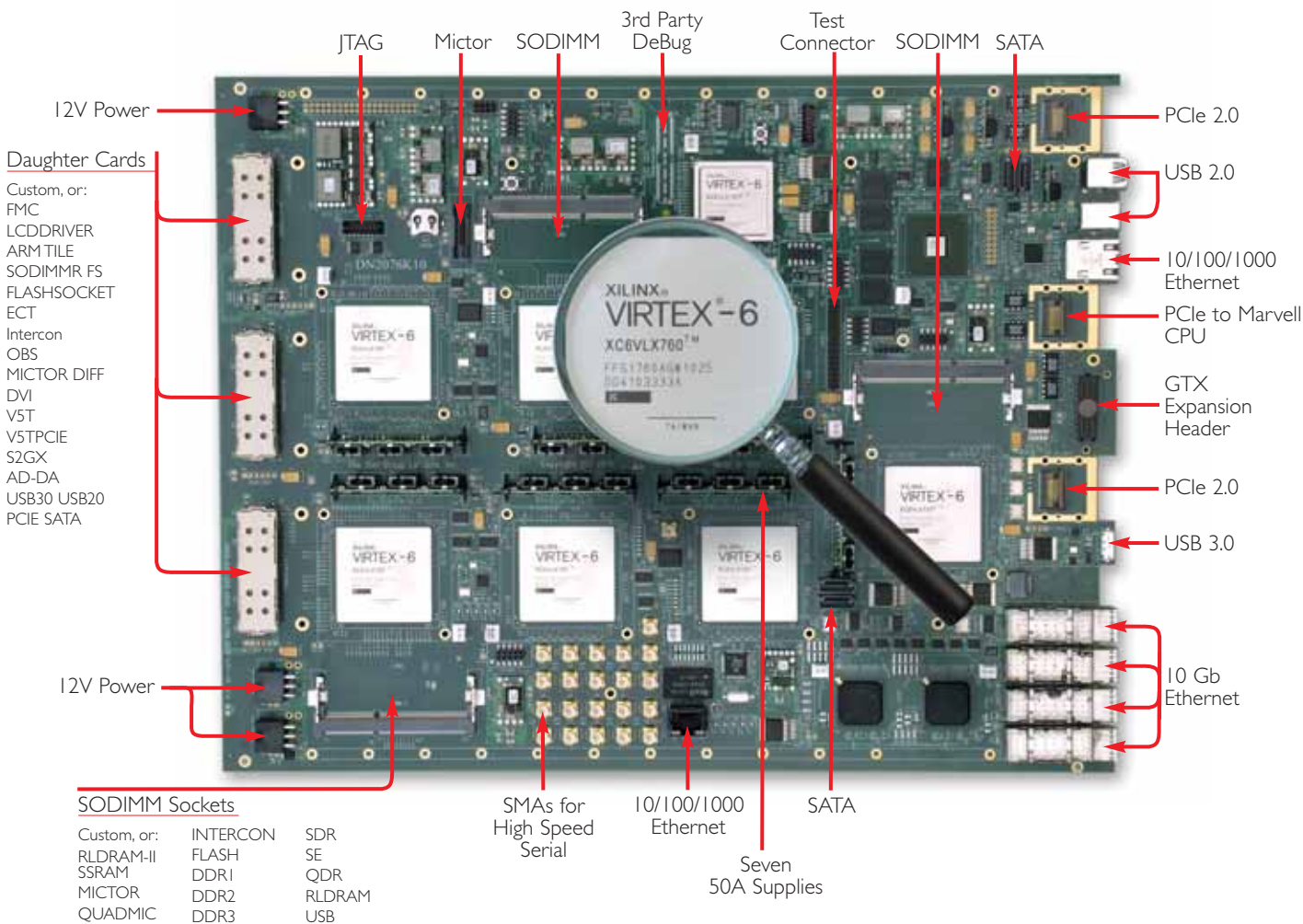


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Welcome to the 2011 Engineers' Guide to FPGA and CPLD Solutions

In this year's edition of the 2011 Engineers' Guide to FPGA and CPLD Solutions, you'll learn more about the best-in-class programmable platforms – silicon, software, IP, boards, kits, reference designs – Xilinx and our ecosystem partners are delivering to hardware and software designers.

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In 2011 and beyond, a key growth driver for the electronics industry – and FPGAs – is an insatiable bandwidth demand from all corners of the globe. In 2014, annual global IP traffic is projected to exceed 3/4 of a zettabyte (1,000,000,000,000,000,000 bytes).



This phenomenon extends far beyond the traditional communications sector into a broad set of end markets: automotive infotainment and driver safety, 3-D digital displays (handheld camcorders, TV, cinema projection), ultrasound imaging, high-definition video surveillance, robotic surgical instruments, even reconfigurable multi-processor computing in outer space, to name just a few.

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Today, FPGA designers are at the forefront of low-cost innovation, bringing to market inventive new products that enrich the quality of our everyday lives. We look forward to witnessing again the magnificent spirit of innovation you'll bring to the diverse markets you serve.



Moshe Gavrielou
President and CEO Xilinx

Contents

Trends to Watch in the Evolution of Programmable Logic

By Cheryl Coupé 4

Cut your development time and cost with smart debugging and ZeBu

By EVE-USA Inc. 6

Dual-Architecture FPGAs Provide New Opportunities for Embedded Developers

By Cheryl Coupé 8

View from the EDA Side

By Cheryl Coupé 11

Intellectual Property and FPGA-based Designs

By Cheryl Coupé 13

FPGAs Pave Way for 5G, 400Gb/s Communications

By Gilles Garcia, director, Wired Communication Business Unit, Xilinx Inc. 40

Products and Services

FPGAs & CPLDs

FPGA Chips

Lattice Semiconductor

LatticeECP3 FPGAs 15

Xilinx, Inc.

Xilinx Spartan-6 FPGAs 16

Xilinx Virtex-6 FPGAs 17

Boards & Kits

Boards / Hardware

Innovative Integration

X5 Family PCI Express XMC Modules 19

X6-RX 20

Xilinx, Inc.

Spartan-6 FPGA Connectivity Kit 21

Spartan-6 FPGA DSP Kit 22

Spartan-6 FPGA Evaluation and Development Kits 23

Spartan-6 FPGA Market-specific Kits 24

Virtex-6 FPGA DSP Kit 25

Virtex-6 FPGA Market-specific Kits 26

Xilinx Embedded Kits 27

Xilinx Transceiver Characterization Kits 28

Development Boards & Kits

Xilinx, Inc.

Virtex-6 FPGA Connectivity Kit 29

FPGA Boards

Alpha Data

ADM-XRC-6T1 - Xilinx Reconfigurable Computer - XMC 30

CES - Creative Electronic Systems SA

VCP-8166 31

Lyrtech

Perseus 601X 32

Pentek, Inc.

Now Shipping The NEW Cobalt Series of Virtex-6 VPX Modules! 33

Scan Engineering Telecom

SAMC-713 High performance Virtex-6 AMC with VITA 57.1 expansion site 34

XDSP-55 Programmable FPGA Accelerator board 35

Xilinx, Inc.

Virtex-6 FPGA ML605 Evaluation Kit 36

Development Tools

Design Tools

Synopsys, Inc.

Synplify Premier - Fast, Reliable FPGA Implementation and Debug 37

Development Tools

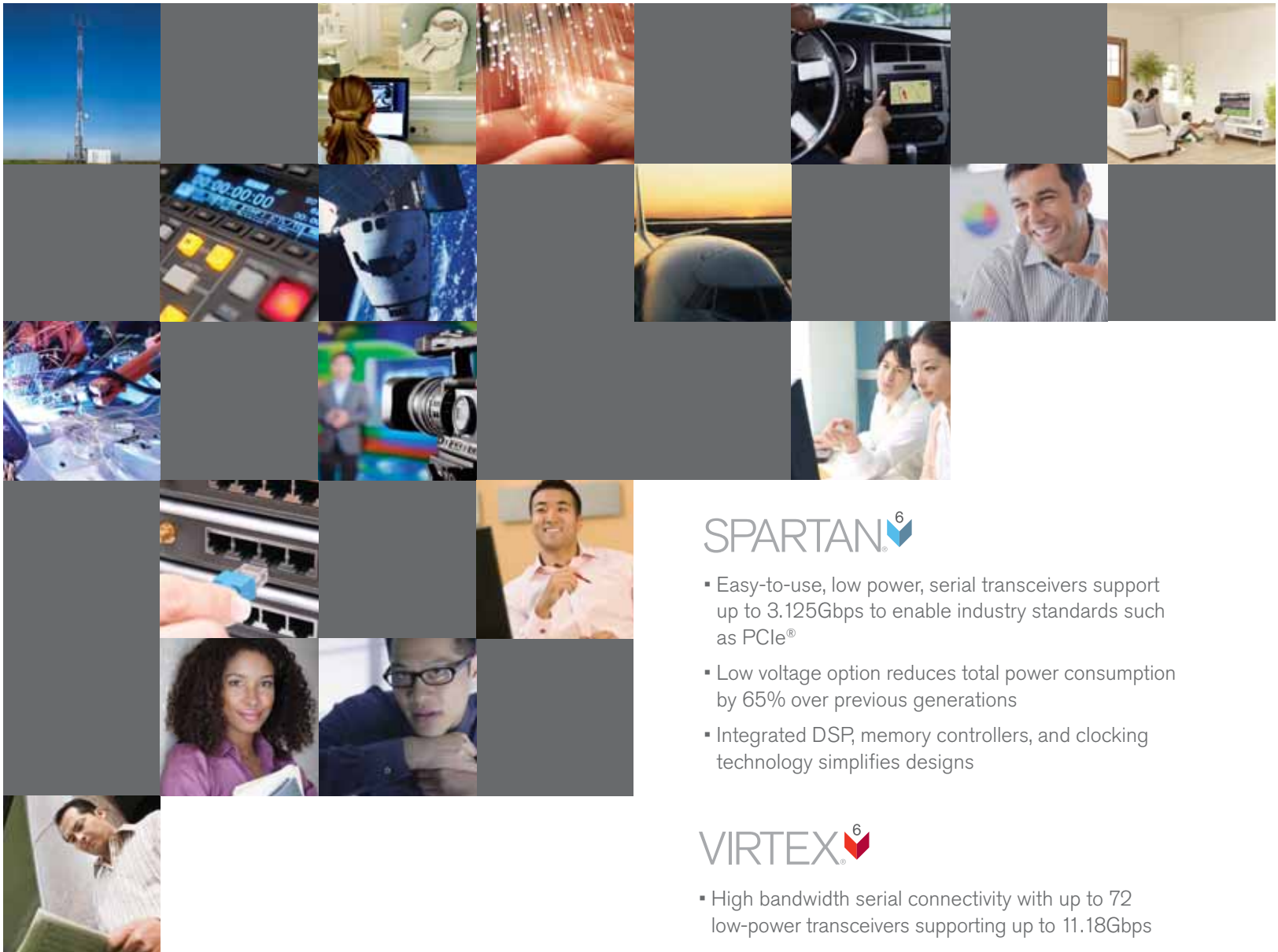
Xilinx, Inc.

Xilinx ISE Design Suite 12 38

DSP and Embedded Development Tools

Lauterbach

TRACE32 PowerTools 39



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Trends to Watch in the Evolution of Programmable Logic

From one-of-a-kind fabrication agreements to dual-architecture system-on-chips, there are plenty of developments to keep track of

By Cheryl Coupé

With a steady stream of news around strategic alliances, mergers, acquisitions, start-ups (and blow-outs), it can be tough to keep track of what's important in the evolution of programmable logic devices and tools. Here are a few FPGA trends and announcements EE Catalog is keeping an eye on, with the help of industry experts to put that news into perspective.

ASICs yield some ground in the face of FPGA performance improvements

As the performance and power consumption of FPGAs improves and the design costs for complex ASICs rise, FPGAs have become viable options for a wider range of new designs. Programmable logic offers low non-recurring engineering (NRE) charges, off-the-shelf availability and the advantage of reprogrammability to accommodate design changes with little impact to design schedules and costs. But while ASICs are yielding ground to programmable devices, designers should expect to see coexistence for some time into the future.

According to Richard Wawrzyniak, senior analyst at Semico Research, FPGAs still have two remaining areas of concern – power consumption and price point – although both of these have become more manageable over time as FPGA manufacturers make improvements to their products. And as design costs for ASICs and systems-on-chips (SoCs) continue to rise, the need for an acceptable alternative also increases. Wawrzyniak believes that as power issues are addressed, FPGAs will find their way into more applications that were closed to them just a few years ago.

Dual-architecture devices change the competitive landscape

A trend that continues to bear watching is the combination of microprocessor and FPGA in a range of configurations as hard- or soft-core dual architectures. Common CPU cores and instruction sets, such as ARM and the Intel Atom, are familiar and widely used. According to Wawrzyniak,

“it then makes sense for FPGA vendors to capitalize on the knowledge and expertise that already exists in the industry and to add these CPU cores to their parts. They are providing their customers with easily recognizable CPU cores that are already widely accepted and known to the industry, allowing for designs done with these parts to more closely match what designers are looking to put into their end silicon solutions.” Wawrzyniak expects to see more of these dual-architecture devices as Intel and ARM make competitive thrusts into each other's traditional markets, and developers will be the beneficiaries of this intersection, with new, innovative tools and devices to meet design challenges.

While ASICs are yielding ground to programmable devices, designers should expect to see coexistence for some time into the future.

Jeff Garrison, Synopsys director of marketing, FPGA implementation, agrees. “The combination of FPGA and microprocessor allows designers to customize their embedded systems for a target applica-

tion – increasingly important in vertical markets such as industrial, automotive, wireless, military and aerospace,” he says. Standard processors offer an existing ecosystem of operating system and IP support that can be leveraged, and designers are typically familiar with available tools for software development for both the processor core as well as the programmable portion of the design. Garrison cautions designers to allocate time early in the design schedule, however, to decide what logic to implement in the software that runs on the processor and what to implement in the FPGA. “Clearly the timing-critical portions of the design should go in the faster FPGA while non-critical portions should go in the processor; however this partitioning is not always so black and white,” he states.

While debug is an increasingly difficult and time-consuming task for FPGA designers, EDA vendors continue to enhance debug technology for embedded (and non-embedded) FPGA design, and have developed software that interfaces with FPGA vendor-provided tools to support processor-based design in their FPGAs. As Synopsys' Garrison says, “Distinguishing problems in the hardware versus the software can

be difficult enough, and then further isolating to the true source can be very time-consuming. For this reason it is important to supplement simulation with debug tools that work with operating hardware.”

Intel-Achronix fab announcement raises questions

Beyond current dual-architecture devices, the November announcement that Intel will build FPGAs for startup Achronix Semiconductor Corp. raises additional questions. With both Xilinx and Actel (now Microsemi) developing products that combine their programmable logic technology with hard ARM processor cores, industry watchers wonder if the Intel-Achronix agreement is a precursor to Intel eventually combining programmable logic with its Atom cores on the same die.

Semico’s Wawrzyniak cautions against reading too much into the announcement, which is still early in the implementation process, but offers three points of speculation:

- Intel is signaling that they are willing to make their cutting-edge manufacturing capability available to small companies on a limited basis to enable new technology to enter the market sooner than would otherwise be the case.
- Intel seems to be interested in matching their existing processor capability with programmable logic, with the requirement that the programmable logic can function at close to, or at the same level, as the performance of their processor technology.
- Since the entire manufacturing supply chain for these high-performance devices is now within the US, the Department of Defense may be very interested in these parts, which will more closely match the performance levels of mil/aero systems being deployed.

New technologies arise in FPGA chips and prototyping tools

Joe Gianelli, vice president of marketing and business development for InPA Systems, an integrated FPGA prototyping start-up, sees a range of opportunities for new FPGA chip and prototyping companies. For chip companies, he sees two main opportunities: vertical niches that are financially unattractive for big players, and leapfrog technology for larger end markets that the big players aren’t likely to innovate. In the first case, he mentions Silicon

Blue as “serving the high-volume/low-price programmable segment with better low-power technology and simplicity in design that enables it to price lower.” For the latter case, he identifies Achronix as “serving the very high-speed programmable market segment with asynchronous clocking technology that creates a new segment.”

Semico’s Wawrzyniak taps Tabula as a company to watch, saying, “I believe their ‘Space-Time’ technology brings a large increase in performance to designers who need it—especially in the communications area. I also believe that their technology could be deployed to solve system-level issues in other areas outside of strictly programmable logic issues.”

It makes sense for FPGA vendors to capitalize on the knowledge and expertise that already exists in the industry and to add these CPU cores to their parts.

Gianelli also sees opportunities for InPA as a supplier of leapfrog EDA technology in the area of rapid FPGA prototyping. “I see the greatest opportunity in serving the verification needs of the ever-growing complex SoC designs,” he states. “I see this today with full custom SoCs but see a growing opportunity in the near future as programmable platforms will become almost as large and complex, and there will be far more of these design starts.”

Wawrzyniak also comments on FPGA-market acquisitions from an IP standpoint. “The acquisition of Virage Logic by Synopsys and of Denali by Cadence earlier this year shows that the IP market is entering another phase of its evolution,” he posits. “I believe a few of the larger IP vendors will now, either through acquisition or through already existing internal resources, offer IP subsystems as products to the market at large. This could have a very large impact on how SoC are designed and represents the first major change in SoC design methodology in many years.” Wawrzyniak suspects that more acquisitions of IP companies might be made over time to facilitate the trend towards IP subsystem products.

Cheryl Berglund Coupé is Editor of EECatalog.com. Her articles have appeared in EE Times, Electronic Business, Microsoft Embedded Review and Windows Developer’s Journal and she has developed presentations for the Embedded Systems Conference and ICSPAT. She has held a variety of production, technical marketing and writing positions within technology companies and agencies in the Northwest.



Cut your development time and cost with smart debugging and ZeBu

EVE complements their high-performance, low-cost hardware-assisted verification platforms with tools and methodology for effective debugging, including new CSA technology.

By *EVE-USA Inc.*

FPGA based hardware-assisted verification tools – like EVE’s family of Xilinx based ZeBu systems – provide a high-performance, low-cost solution for fast System-On-Chip (SOC) emulation. However, providing multi-MHz performance and offering the most cycles per dollar aren’t the only requirements for a world class emulator like ZeBu. Sure, ZeBu users can boot Linux on an embedded processor design in just minutes, or process a full HD video frame in under a second – but what happens when a failure occurs after a billion cycles of testing? Billion-cycle debugging requires not only advanced debugging technology, but also a smart methodology to leverage that technology effectively.

EVE is a pioneer in providing debugging technology and design access within FPGA based hardware-assisted verification platforms. ZeBu fast emulators provide complete Register Transfer Level (RTL) access to your emulated design – even to the combinational signals. In addition to supporting multiple probe types for design access and waveform generation, ZeBu systems are well-appointed with a wide array of debugging technology, including: SystemVerilog Assertion (SVA) support, built-in logic analysis and trace memory, ZEMI-3 transactors, save & restore capabilities, and an offline debugging framework. These tools enable an efficient debugging methodology to quickly reproduce, isolate and identify the source of billion-cycle failures.

Before you can even start looking for a billion-cycle bug, you must be able to quickly reproduce the failing test. And since debugging in emulation is typically a multi-pass affair, maintaining the highest performance possible throughout the bulk of the debug process is critical. ZeBu emulators are the fastest on the market and support designs of up to 1 billion ASIC gates, so reproducing an error after a billion cycles takes only minutes, even at the full-chip level. Additional ZeBu technology, such as save & restore and the offline debugging framework, provides users with further improvements in the reproduction of tests in co-simulation, co-emulation, and in-circuit emulation environments.

Also critical for a smart debugging methodology is the generation and use of relevant information over raw data. Even for small designs, dumping a billion cycles worth of waveforms is often an unrealistic debugging solution. Wading through that much waveform data without any context could take forever – if your waveform viewer could even open up a file that big! For smart debugging, you need high-abstraction debugging technology that provides insight into the root cause of the failure without sacrificing performance. ZeBu users can leverage software debuggers, ZEMI-3 monitor transactors, logic analysis, SVAs, and pre-compiled Static and Flexible probe sets to isolate the sub-system and the appropriate time window or trigger point of the failure. These technologies execute at MHz speeds and above, enabling multiple rounds of convergent debugging without giving up vital performance.

Waveform generation and detailed debugging should only occur after a realistically usable time window and sub-system has been isolated. With ZeBu’s Dynamic probes, integrated with EVE’s new Combinational Signal Access (CSA) technology, users have run-time access to any sequential or non-sequential net in the design without requiring any re-compilation or the insertion of additional probe logic. RTL waveforms can be generated live during a run, or offline for improved performance and efficient resource utilization, and can be used to ultimately identify the source of the billion-cycle failure.

With ZeBu, you get more than just a high-performance, low-cost FPGA based emulation system. You also get the debugging technology you need, including CSA and offline waveform generation, to implement a smart debugging methodology to quickly reproduce, isolate and identify bugs. ZeBu cuts the development time and cost of your entire SOC project, enabling billion-cycle hardware verification, software validation and hardware/software co-verification. To learn more about ZeBu emulators and smart debugging, please contact the professionals at info@eve-team.com or visit <http://www.eve-team.com>.



SW debuggers, log files isolate the window of failure to a few million cycles



Monitors, Checkers, Assertions further isolate the window to a few thousand cycles



Waveform analysis finally identifies the HW bug (or re-focuses the search to SW)

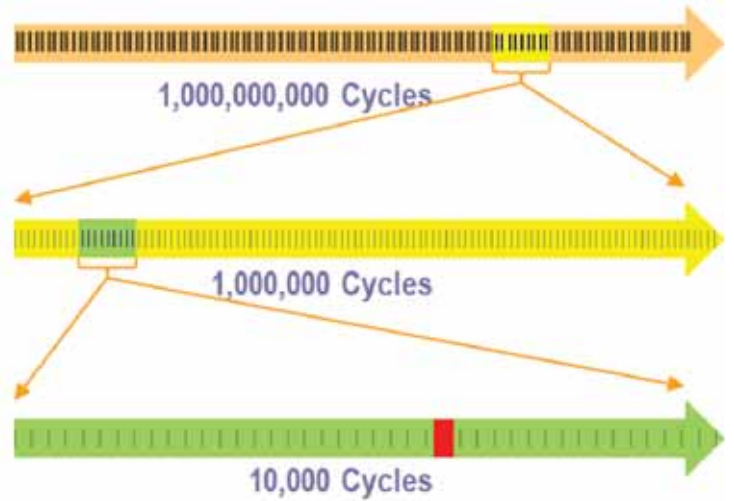


Figure 1: Reproduce, isolate and identify the source of a billion-cycle failure with ZeBu

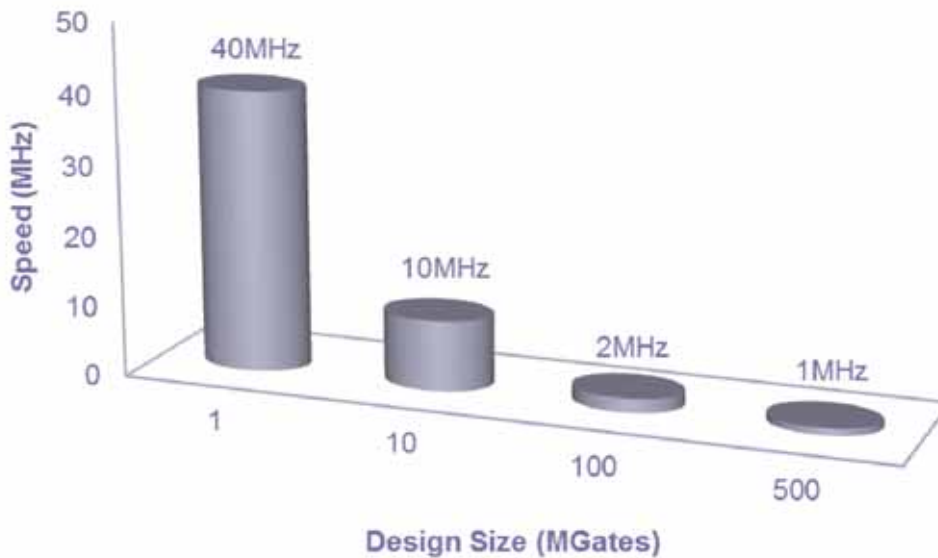


Figure 2: ZeBu Performance by Design Size

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Dual-Architecture FPGAs Provide New Opportunities for Embedded Developers

While FPGAs still require trade-offs in price and performance, advances in architectures and development tools can address a wide range of design goals

By Cheryl Coupé

With the integration of hard or soft-core microprocessors, today's FPGAs give embedded developers new levels of performance and flexibility. But as always, there are trade-offs to consider in the ASIC-FPGA decision. EECatalog spoke to Glenn Steiner, senior processor technical manager at Xilinx, Mike Kendrick, manager of software product planning at Lattice Semiconductor and Matt Ferraro, engineer at Connect Tech about what those trade-offs are, and how developers can best take advantage of new FPGA devices and tools.

EE Catalog: How are FPGA vendors helping embedded developers address design goals such as reduced bill-of-material (BOM) costs, reduced power consumption or shortened design cycles?



Glenn Steiner, Xilinx: Embedded processing using FPGAs for customization and improving system performance has become an integral part of a growing number of applications across a wide range of end markets, including aerospace and defense, wired and wireless communications, automotive, audio/video broadcast, industrial control, test and measurement and consumer. Driving this trend is the need to reduce cost, weight, area and power by means of large-scale integration through SoC design, while at the same time enabling design reuse and mitigating design risk as well as obsolescence. As a SoC platform, FPGAs provide embedded designers with deep levels of integration and high levels of parallel processing performance. But they also offer design flexibility so that designers can respond to changing standards, evolving customer needs and any other change in design requirements and still meet their time-to-market window.

Embedded designers have traditionally purchased general-purpose processors, or ASSP-based processors, in an attempt to match processing and peripheral capabilities against system requirements. While FPGAs can be used to bridge missing IP and system performance gaps in their traditional role, today's FPGAs with integrated hard or soft processors enable designers to implement complete systems-on-a-chip to reduce BOM costs. In addition, placing data processing either with the processor or the FPGA logic results in lower system costs as well as lower

power consumption compared to other implementations. For example, a Pentium-style processor can perform data processing on an HD video stream at the cost of over \$100 and tens of watts, while an FPGA costing one tenth the price can perform the same function at one tenth the power.

In an effort to substantially simplify and accelerate the means by which both embedded software and hardware designers gain access to these benefits, FPGA vendors like Xilinx are developing fully-functional, tested and supported targeted reference designs for its FPGAs in addition to tools and development platforms to enable a productive design environment.



Mike Kendrick, Lattice Semiconductor: Soft processors embedded within the FPGA allow high-functional density for many different functions that do not require high-speed parallelism. This is the standard value proposition of a processor – it takes up minimal silicon area to execute sequential software that is highly malleable, but low performance. Now this capability is available integrated into an FPGA.

As the cost per FPGA look-up table (LUT) falls quickly, processor LUT count remains constant, so the economics of integrating a processor within an FPGA continue to improve compared to a two-chip solution. Also, the reduced chip count, compared to a two-chip solution, reduces manufacturing costs and mean time between failure among other benefits, resulting in a less expensive, more reliable product.

Using an embedded processor can lead to lower power, particularly if the processor does not increase the size of the FPGA needed in the first place for the particular design. Finally, soft processors are insurance against obsolescence versus the discrete processor catalog.



Matt Ferraro, Connect Tech: By embedding a microprocessor within an FPGA you can simplify the overall design. In many complex applications, the FPGA and processor require separate memory, flash, debug ports and pro-

gramming chains – which now can be shared. As well, the processor's requirement for additional voltage rails, power sequencing and power on reset circuits is all but eliminated, with current FPGAs having very lenient startup conditions. Not only is BOM cost reduced, but the complexity of the PCB design and layout is significantly reduced. Now designers only need learn the intricacies of one complex device instead of two, significantly reducing the time to market.

EE Catalog: What's happening with dual-architecture FPGA/microprocessor packages? Where is this trend heading and what are the application needs that are driving this evolution?

Steiner: Processor-centric solutions—including microprocessors, ASICs, ASSPs, and application processors – are a dominant force in today's semiconductor market. Many of these products are designed as SoC solutions, including a core processor engine that is complemented by common- and application-specific IP. Yet, with the continuing progression of Moore's Law, new product investments continue to escalate, resulting in fewer new product starts with products optimized for only the highest volume markets. This trend towards a commodity model limits customers' ability to optimize and differentiate, which makes achieving a competitive advantage an increasingly difficult goal. FPGAs with embedded processors enable the reversing of this trend.

The coupling of processor and FPGA continues to evolve. Compact, soft processors such as the Xilinx PicoBlaze processor were developed for small, early-generation FPGAs, and were ideal for state machine or simple functions such for GPIO, keyboard and display control. Next, complex soft processors like the MicroBlaze processor are capable of running operating systems such as Linux and are used in applications ranging from motor control to portable medical devices. Hardened processor cores, such as the PowerPC processor, have now been in multiple generations of FPGAs where higher performance processors have been required for applications such as radar imaging.

Next-generation architectures will focus on processor centricity with complete hardening of the processor, peripherals, memory interfaces and IO paths. This approach provides software developers a familiar programming environment within an optimized, full featured, powerful, yet low-cost, low-power processing platform. Meanwhile, system architects and logic

designers can fully leverage the programmable logic to extend, customize, optimize and differentiate their solutions.

Kendrick: The question is whether an FPGA with an embedded hard processor can find a viable application space, compared to the use of a discrete processor plus an FPGA, or the use of an embedded soft processor.

As the cost per FPGA look-up table (LUT) falls quickly, processor LUT count remains constant, so the economics of integrating a processor within an FPGA continue to improve compared to a two-chip solution.

Compared to a two-chip solution (discrete processor and FPGA), the FPGA with an embedded hard processor limits the choice of processor to use and, in most applications, delivers much less performance. This is because new generations of discrete processors are released frequently and their performance quickly surpasses the FPGA's on-chip processor. On the other hand, using

an on-chip processor can be the less expensive approach, but only if performance requirements for speed and capability are modest.

Compared to a SoC ASIC, the on-FPGA chip processor approach results in a higher unit cost and provides less flexibility (e.g., the bus structure). However, the on-FPGA chip solution presents less risk, since it is possible to go to production with a prototype.

Ferraro: In the early days of FPGA embedded processing, 'soft core' processors were implemented using FPGA resources (LUT and flip fops). Most of these processors were developed by the FPGA companies, having proprietary architectures and instruction sets, like the Xilinx MicroBlaze or Altera NIOS. Third-party processor IP existed to implement more common architectures, but the cost was prohibitive to all but the largest companies with high-volume applications. These soft processors were significantly slower than external processors, and not capable of handling anything more than a complex statemachine. Then FPGA vendors started to incorporate hard processor IP directly onto the FPGA die, licensing architectures like the PowerPC (in Xilinx's Virtex family). For many applications, the cost of a high-end FPGA is too high, while the capability of a PowerPC is overkill. So more recently the focus has been incorporating more popular embedded architectures, like ARM Cortex and eventually Intel's Atom.

EE Catalog: What do engineers need to know about development tools for these dual architectures? What will the learning curve be? How will that impact adoption?

Steiner: Programmable logic devices are well-supported by sophisticated tools suites. These tools provide logic designers an environment rich in features to optimize their IP solutions and render them onto FPGA. In this environment, the programming languages are hardware-oriented such as Verilog and VHDL.

However, software developers work almost exclusively in high-level languages, such as C/C++, which are also well supported by today's processor-based solutions. For the Extensible Processing Platform, Xilinx will support familiar software development and debug environments, using tools such as ARM Real View and related third-party tools, Eclipse-based IDEs, GNU, Xilinx Software Development Kit and others. The programmable logic portion can be developed and debugged using the standard ISE Design Suite, and other third party HDL and algorithmic design tools.

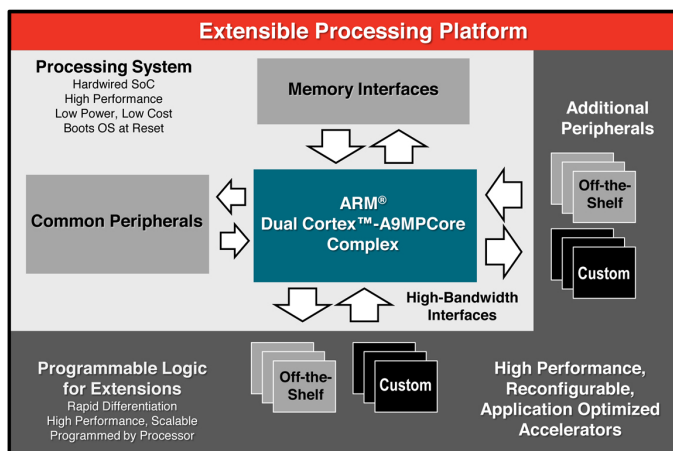
Because the Extensible Processing Platform takes a processor-centric approach (it boots the Processing System at reset and then manages the programmable logic configuration), a more software-centric development flow is enabled. This flow enables the system architect, logic designer and software developer to work in parallel, using their familiar programming environments, then merge the final releases into the software baseline. As a result, key partitioning decisions on system functions/performance can be made early and throughout the development process.

This is critical for embedded systems where application complexity is driving tremendous levels of system performance against tightly-managed cost, schedule and power budgets. It is important to note that the AMBA-AXI interfaces are key in enabling the software-centric flow because they present a seamless, common and well-defined environment for the hardware extensions. While the logic designer will need to deeply understand this technology, for the software developer the AMBA interfaces abstract the extended logic as memory mapped calls. This allows for a straightforward interplay of hardware and software programming in a parallel state of development.

Kendrick: The biggest issue for new SoC designers using this dual-architecture technology will be getting visibility of what is going on internally when the processor and complex logic are all integrated onto one chip.

Current SoC ASIC designers will see an improvement in debug because they will have more ability to do board-level testing and validation rather than relying so heavily on modeling and verification.

Embedded designers will have a challenge with the hardware shifting under them. They will be used to a much more static hardware platform (e.g., a catalog discrete processor), so this will have to be managed with the new flexibility afforded by processors integrated with programmable logic



Xilinx's architecture for a new Extensible Processing Platform is optimized for system power, cost and size. Based on ARM's dual-core Cortex-A9 MPCore processor and Xilinx's 28 nm programmable logic fabric, the Extensible Processing Platform takes a processor-centric

Ferraro: Many of the FPGA vendors have well-supported tool chains, advertising the drag-and-drop approach of building up peripherals for an embedded processor system within an FPGA. However, the new developer should be forewarned that this supposedly seamless approach works well with development boards, but not so much with custom hardware which will require tweaking peripheral parameters and likely timing constraints. Creating custom peripherals for hardware co-processing can require a more advanced knowledge of VHDL or Verilog. In addition, many popular embedded operating systems will offer board support packages (BSPs) for FPGA/microprocessor architecture, but again these BSPs target development boards. The designers must be prepared to develop their BSP, specifically boot loaders and other startup routines. While the learning curve is steep, attending a training seminar and experimenting with development boards cuts the time dramatically.

Cheryl Berglund Coupé is Editor of EECatalog.com. Her articles have appeared in EE Times, Electronic Business, Microsoft Embedded Review and Windows Developer's Journal and she has developed presentations for the Embedded Systems Conference and ICSPAT. She has held a variety of production, technical marketing and writing positions within technology companies and agencies in the Northwest.



View from the EDA Side

EDA vendors speak out on strategies to meet embedded design goals with FPGAs

By Cheryl Coupé

While shiny new chip designs draw attention, electronic design automation (EDA) firms work diligently behind the scenes to create tools and systems that help embedded developers address design goals such as reduced bill-of-materials (BOM) costs, reduced power consumption and shortened design cycles. EE Catalog asked several EDA vendors how they are helping embedded developers meet these goals.

Juergen Jaeger, senior product manager at Cadence, responds, “At first, the answer seems very obvious: just put the hardware part (the chip), including the embedded processor(s) into one or more FPGAs, thus providing a pre-silicon platform that allows the developer to experiment and make decisions about what should be realized in the hardware and software. These findings can be used to guide the partitioning between hardware and software and to achieve the BOM and power consumption goals.” But, he continues, “as it often the case, the devil lies in the details.”

For this approach to deliver the expected results, the developer must be able to easily map the hardware portion of the design into the FPGA and quickly implement hardware design iterations to experiment with multiple hardware/software partitioning scenarios. The developer must also be able to preserve the integrity and functionality of the original RTL; that is, there are no FPGA-specific changes required.

In order to accomplish this, embedded developers need to look beyond the FPGA to the overall design and verification flow. Jaeger states, “The key requirement for this flow is not to optimize it for maximum FPGA performance, but rather for implementation and iteration speed, as well as for ease-of-use.”

Taking a somewhat different approach is InPA Systems, a start-up integrating custom or fixed FPGA prototypes with existing EDA verification environments (from Cadence, Mentor Graphics, and Synopsys) to achieve fast time-to-pre-silicon-prototypes. Joe Gianelli, InPA’s VP of marketing and business development, sees risks and opportunities for developers moving to new technologies. These decisions can affect high-level design goals such as leapfrogging competitors.

While today’s economic climate doesn’t necessarily support riskier approaches, I see this changing as companies realize that without some risk-taking, they’ll never move out of their incremental box.

Gianelli says, “In most cases, moving to a new device from an FPGA prototyping vendor (e.g., Altera or Xilinx), or moving to a new tool from a full-line EDA vendor (e.g., Cadence or Synopsys) is low risk, and the opportunity is fairly incremental.” While this path involves the least amount of change and risk, developers taking the well-paved road in favor of a riskier path

that may not work may also miss opportunities to leapfrog past their competitors.” While today’s economic climate doesn’t necessarily support riskier approaches,” Gianelli continues, “I see this changing as companies realize that without some risk-taking, they’ll never move out of their incremental box.”

Let’s take a closer look at a few common design goals and see what EDA vendors have to say.

Cost reduction

Jeff Garrison, director of marketing for FPGA implementation at Synopsys, states that using a synthesis tool that is timing-driven is key to cost-reduction efforts as the performance requirement can be specified and then, once met, the tool will focus on area optimization. “By minimizing logic cell use while meeting required timing performance, a design’s power consumption and size can often fit into a smaller, less expensive FPGA and possibly a cheaper package,” he says. “Using a one-size smaller FPGA

can save 20% or more, which is significant, especially when volume is in the hundreds or thousands of parts.”

Daniel Platzker, product marketing director at Mentor Graphics, takes a similar approach. Because the FPGA may be the most expensive component on the board, BOM costs can be significantly reduced by targeting the least expensive device that still meets requirements. This is where EDA vendors – which are typically device agnostic – can help. Their tool flows allow designers to flexibly target the most competitively priced device for each project from any FPGA supplier. “Third-party tool vendors develop and continue to improve technologies such as physical synthesis so development teams can maximize design performance for the cheapest possible device—from multiple FPGA vendors,” Platzker says.

Power consumption

Mentor’s Platzker notes that reducing power consumption is becoming a higher priority as more FPGAs are adopted in portable devices. While static power is largely driven by the silicon architecture, and hence up to the FPGA vendors to address, EDA vendors offer system-level design methodologies and implementation flows that can help designers reduce power in other ways.

“At the system level, transaction-level modeling methodologies are now available for writing ESL models with associated power estimates, allowing designers to evaluate and optimize the interaction and power consumption of various IP components at an early stage of the design cycle,” says Platzker. “Once the design is stabilized in RTL form, RTL synthesis can reduce dynamic power of clock networks, design logic, memories and I/O banks through algorithms transparent to the user. For example, optimal clock buffers can be put in place to shut off logic networks not in use, and memories can be split in ways so each memory access activates fewer embedded RAM components.”

Synopsys’ Garrison also addresses smaller designs, which tend to consume less power. He notes that Synopsys FPGA synthesis can optionally power down bits in BlockRAMs and DSP blocks when they are not being used, in order to reduce dynamic power consumption. In addition, “partial

reconfiguration allows for a section of the design to be reconfigured on the fly, which can result in power reduction by making it possible to power down parts of the design,” he comments.

Productivity/shortened design cycle

One concern for productivity is design tool turnaround time for today’s very large FPGAs. Luckily, EDA and FPGA vendors are working together to address this by supporting incremental design flows and improving tool runtime. As an example, Garrison explains that Synopsys and Xilinx have been working together to support the Xilinx Design Preservation flow, which allows portions of the design that have met timing to be ‘preserved’ so that further changes at the top level don’t introduce new problems. EDA vendors are also helping with support for partial reconfiguration in FPGAs, which allows for a section of the design to be reconfigured on the fly, enabling logic changes to be made in the deployed system.

Mentor’s Platzker states, “EDA vendors are working to reduce the FPGA design cycle at every point of the flow, from design creation, through verification, implementation and finally board integration. Design houses are best served by standardizing on a well-integrated solution that includes ESL design, advanced verification methodologies such as test-bench coverage and assertions, vendor independent synthesis and I/O assignment solutions that simplifies the board integration process. A comprehensive ESL-to-FPGA gate flow not only ensures consistent results but also provides a single point of support for quick problem resolution. It’s a combination that ultimately shortens the design cycle.”

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Intellectual Property and FPGA-based Designs

Insight from the Trenches

By Cheryl Coupé

Intellectual property (IP) subsystems allow developers to add functionality quickly and effectively. But as these subsystems proliferate, a range of design and test issues arise. EE Catalog asked several industry pundits what issues developers need to be aware of relating to IP subsystems, especially for specific vertical-market applications such as medical, automotive and others. Insight comes from Richard Wawrzyniak, senior analyst at Semico Research; Glenn Steiner, Xilinx senior processor technical manager; Jeff Garrison, Synopsys director of marketing, FPGA implementation; Mike Kendrick, manager of software product planning at Lattice Semiconductor Corporation; and Joe Gianelli, VP marketing and business development, InPA Systems.

Look for horizontal, rather than vertical, markets for IP subsystems

Richard Wawrzyniak, senior analyst, Semico Research



SoC designers are looking to acquire IP that addresses system-level problems instead of merely licensing many discrete IP blocks from many separate vendors and then taking that IP to build up to the system-level solutions they really need. SoC designers are looking to move up a layer of abstraction to reduce the amount of effort they are expending to design this type of functionality into their systems.

Because designers are looking to acquire system-level functionality instead of a collection of discrete IP blocks, I believe the market for this type of solution will not be vertical in nature, but horizontal. Designers are looking for a communications subsystem, or a video subsystem, etc. that will be aimed at a particular market segment like medical, automotive, etc. I do not believe IP subsystem vendors will be able to address all the possible market niches for subsystem solutions with specific products. Instead, IP subsystem vendors will create subsystems that provide a certain amount of functionality at the system level that SoC designers will then shape into the correct configuration through applications software. In addition, since these subsystem products are configured around their own internal interconnects, it will be possible for the SoC designers to swap out individual IP blocks within the subsystem for other IP blocks that more fully meet

the needs of the application as required. This will provide the designer with the correct level of granularity, but at a fraction of the effort and cost he had been expending previously.

FPGAs have been the vehicle of choice for several years for SoC designers who were looking to test or prove out a specific type of IP or even many types of IP before actually needing to design the SoC and taking a test chip through a shuttle program at a silicon foundry. The advent of the IP subsystem will not change this relationship between SoC designers and FPGA vendors. If anything, the relation will become tighter and more important as SoC designer look to try out many different types of IP subsystems to find the right one for their design.

Incidentally, the Intel-Achronix, Intel-Altera and ARM-Xilinx announcements lend support to the development of the IP subsystem trend – although I don't believe it was at all intentional – merely co-incidental. IP solutions that function at the system level require FPGAs that both have the right level of performance (so that applications software can be executed at close to system speeds) and that have the right types of CPU cores (CPU cores that match what SoC designers will use) that closely mirror what will be used in the final silicon solutions.

Having FPGAs that can execute at system speeds and that have the right types of CPU cores will give a boost to Soc designers in evaluating the IP subsystem products about to enter the market.

Embedded kits support parallel hardware and software development

Glenn Steiner, Xilinx senior processor technical manager



Embedded software developers have very different environmental needs than their hardware engineering counterparts. Specifically, the software developer wants a compiler, a debugger, an Eclipse-based integrated design environment, an industry-standard operating system (e.g., Linux, μ C/OS), a robust set of software libraries and a stable processor system with well-defined peripherals. Embedded hardware designers, however, are more concerned about system architecture, IP

verification and timing closure. They require pre-verified hardware reference designs as starting points to evaluate the underlying FPGA platform. From there, they might add standard IP, integrate some custom IP and also remove IP blocks that they do not need. Ideally, they need a high-level environment to make these design changes quickly, without having to modify RTL code (VHDL or Verilog) for each change.

For example, Xilinx has developed an embedded processing targeted reference design in the form of a fully functional and widely applicable MicroBlaze Processor Sub-System (PSS), accompanied by all of the requisite software design environment components that specifically and uniquely fulfill these requirements. Serving as the base for a new generation of embedded processing platforms, the MicroBlaze PSS integrates essential processing, memory and I/O functions and is supported by a strong software ecosystem, offering middleware stacks and industry-leading operating systems such as Linux and μ C/OS-II.

When used with the new Spartan-6 and Virtex-6 FPGA Embedded Kits, the MicroBlaze PSS allows software application developers to begin writing and porting their application code to the embedded platform before any hardware development has begun. Moreover, application software developers can immediately evaluate the performance of the processor, internal and external memory, bus architectures and I/Os against their system requirements. The developers can even begin optimizing their application software to the MicroBlaze PSS in parallel with the hardware design effort. Similarly, the new embedded kits provide everything the hardware design team needs to quickly evaluate the Xilinx embedded platform capabilities, as well as modify and extend these to their specific application needs.

Recognizing the needs of specific vertical markets, kits are now available targeting applications such as industrial Ethernet, industrial video processing, broadcast connectivity and high-performance digital signal processing. Thus, the kits create the opportunity for both the hardware and software design teams to move quickly and simultaneously through their respective evaluation and development processes. This methodology will of course support the Extensible Processing Platform.

Efforts under way to enable multi-vendor IP use while protecting it from unlawful practices

Jeff Garrison, Synopsys director of marketing, FPGA implementation



Using IP in today's FPGA designs is the norm for almost all vertical market applications. Of course the type of IP required for the different vertical markets vary, but the

basic need for integrating IP into an FPGA design flow is widespread. The IP can come from in-house development on a previous design, the FPGA vendor themselves or from a third-party IP provider. In most cases the cost to develop standard functions like USB, SATA, PCIe, Ethernet, memory controllers, etc. is more than buying from a third party.

Developing IP in house and then remaining competitive by continuing to quickly adapt to standards changes and enhancements is much more than acquiring third-party IP. Third-party IP is typically delivered with constraints applicable to its interfaces, and with test harnesses applicable to specific nodes within the IP. For this reason, it is vital that synthesis tools provide controls that allow users to preserve IP boundaries for constraints application and preserve specific test nodes within the IP that will be probed during test.

One of the key challenges the industry faces is enabling IP use across a range of design tools from multiple vendors while still protecting the IP from reverse engineering and other unlawful practices. Tools such as simulators need to be able to decrypt protected IP to accurately simulate the IP's behavior within the design, while transformative tools such as synthesis need to both decrypt and encrypt the results in order to produce the fastest, smallest, lowest power design implementation. For this reason there needs to be a standard way for all EDA / FPGA vendors and IP providers to enable and protect IP used throughout the tool chain.

Synopsys, Xilinx and others are working toward the ratification of IEEE-P1735 which seeks to establish a standard for encryption and rights management for electronic design IP. Synthesis tools for example, must be able to read the IP in order to optimize logic surrounding the IP in the context of the overall design while producing an encrypted result that can be used by further downstream tools like place and route. Likewise, it would be extremely beneficial for debugging tools to be able to report on key signals within the IP for debug purposes. With rights management implemented, an IP provider could identify key signals within their IP that debug tools could access for this purpose.

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LatticeECP3™ is the best-in-class mid-range FPGA with high-performance SerDes, full-featured DSP blocks, and support for state-of-the-art memory interfaces including DDR3. It offers 35% to 100% more silicon resources in smaller packages compared to competitors. The low-power LatticeECP3 FPGAs are used in a wide-range of applications, such as wireless and wireline communication, video processing, security and surveillance, industrial networking, industrial automation, computing, storage, medical equipment, and consumer.

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FEATURES & BENEFITS

- ◆ Low-power, high-value FPGA fabric. Logic densities from 17K to 150K LUTs, up to 7 Mbits of embedded block RAM, up to 300 Kbits of distributed RAM.
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APPLICATION AREAS

Wireless and Wireline Communication, Large and Small LCD Display Interfaces, Video Game Consoles, Video and Image Processing, Security & Surveillance, Industrial Networking, Industrial Automation, Computing, Storage Controllers, Gaming Equipment, Medical Equipment, Consumer, etc.

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Xilinx, Inc.

Xilinx Spartan-6 FPGAs

The Xilinx® Spartan®-6 FPGA family offers an optimal balance of cost, power, and performance for consumer, automotive, surveillance, wireless, and other cost and power-sensitive applications.

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FEATURES & BENEFITS

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TECHNICAL SPECS

- ◆ Spartan-6 LX FPGAs - The industry's lowest risk and lowest cost solution for high-performance logic
- ◆ Spartan-6 LXT FPGAs - The industry's lowest risk and lowest cost solution for serial connectivity



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- ◆ Start designing today with the Spartan-6 FPGA Evaluation Kit that provides all elements needed to design right out of the box

AVAILABILITY

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APPLICATION AREAS

Automotive, Broadcast Video, Consumer Electronics, Wired/Wireless Communications, Aerospace & Defense, and Industrial, Scientific and Medical Instrumentation

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Xilinx Virtex-6 FPGAs

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FEATURES & BENEFITS

- ◆ Low power and high performance with greatly simplified power system design
- ◆ Optimized feature mix delivers two-fold increase of Flipflops and BRAM with six times more DSP than similar-sized devices
- ◆ Integrated system blocks save up to 10X static power compared to soft implementations
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TECHNICAL SPECS

- ◆ Virtex-6 LXT FPGAs for high-performance logic, DSP and serial connectivity with up to 36 low-power 6.6Gbps GTX transceivers and 864 DSP slices at 600 MHz



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- ◆ Start designing today with the Virtex-6 FPGA Evaluation Kit that provides all elements needed to design right out of the box

AVAILABILITY

Available now! Visit: <http://www.xilinx.com/virtex6>

APPLICATION AREAS

Automotive, Broadcast Video, Consumer Electronics, Wired/Wireless Communications, Aerospace & Defense, and Industrial, Scientific and Medical Instrumentation

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FEATURES & BENEFITS

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TECHNICAL SPECS

- ◆ 400 MSPS, 14-bit A/D channels
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XMC Module (75x150 mm)
PCI Express (VITA 42.3)
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Adapters for VPX, Compact PCI, Desktop PCI and Cabled PCI Express System

AVAILABILITY

Shipping

APPLICATION AREAS

- ◆ Wireless Receiver and Transmitter
- ◆ WLAN, WCDMA, WiMAX front end
- ◆ RADAR
- ◆ Electronic Counter Measures (ECM)
- ◆ Electronic Warfare
- ◆ High Speed Data Recording and Playback
- ◆ High speed servo controls
- ◆ Spectral Analysis
- ◆ IP development

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Innovative Integration

X6-RX

OS Support: Windows, Linux, and VXWorks/Wind River

Bus Interface: natively xmc/pmc adapters to VPX, cPCI, PCI, PCI Express

The X6-RX is a flexible receiver that integrates IF digitizing with signal processing on a PMC IO module. Up to 24 configurable receiver channels with a powerful Xilinx Virtex 6 FPGA signal processing core, & high performance PCI Express/PCI host interface. With the X6-RX, IF recorders can log both the digitized raw data & channels real-time sustaining rates over 2 GB/s.

The X6-RX features four, 16-bit 160 MSPS A/Ds with dual digital downconverters (DDC). IF frequencies of up to 300 MHz are supported. The sample clock is from either a low-jitter PLL or external input. Multiple cards can be synchronized for sampling & downconversion.

A Xilinx Virtex6 SX315T (LX240T at initial release) with 4 banks of 128MB DRAM provide a very high performance DSP core with over 2000 MACs (SX315T). The close integration of the analog IO, memory & host interface with the FPGA enables real-time signal processing at extremely high rates.

Onboard DDC ASIC device, connected directly to the FPGA, provides up to 24 narrowb &/or 8 wideb & channels with input from two A/D channels. The DDC performs complex or real downconversion, with flexible controls for mixing, filtering, decimation, output formats & data rates. Channels can be synchronized to support beam forming or frequency hopped systems.

Power is less than 15W for typical operation. VITA 20 conduction cooling is used with a heat-spreader & sink are Ruggedization levels for wide-temperature operation & conformal coating are supported.

FEATURES & BENEFITS

- ◆ Four 160 MSPS, 16-bit A/D channels
Down-Converter ASIC supporting up to 24 Narrow-band or 8 Wideband Channels
+/-1V, AC-Coupled, 50 ohm, SMA inputs
- ◆ Xilinx Virtex6 SX315T/SX475T or LX240T
4 Banks of 128MB DRAM
Ultra-low jitter programmable clock
- ◆ x8 PCI Express Gen2, providing 2 GB/s sustained transfer rates
PCI 32-bit, 66 MHz with P4 to Host card
- ◆ PMC/XMC Module (75x150 mm)
15W typical
Conduction Cooling per VITA 20



- ◆ Ruggedization Levels for Wide Temperature Operation
Adapters for VPX, Compact PCI, desktop PCI and
cabled PCI Express systems

TECHNICAL SPECS

- ◆ Available XMC carrier adapters offer conduction & convection cooling & are available for a range of interfaces including Desktop PCI, Desktop PCI Express, Cabled PCI Express, CompactPCI, & PXI/PXI Express.
- ◆ Extremely versatile, easily adapted for use in virtually any type of system.
The X6-RX is also readily installed into Innovative Integration's Instrument Embedded PC, SBC-ComEx Single-Board Computer, & Andale Data Loggers.
- ◆ PCI gen 2 to 24 Megabytes per second.
200 fS clock jitter
- ◆ 15 watt nominal power dissipation!
- ◆ Military rugged versions available.

AVAILABILITY

Shipping

APPLICATION AREAS

- ◆ Wireless Receiver
- ◆ WLAN, WCDMA, WiMAX front end
- ◆ RADAR
- ◆ Medical Imaging
- ◆ High Speed Data Recording and Playback
- ◆ IP Development

CONTACT INFORMATION



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Spartan-6 FPGA Connectivity Kit

Supported Xilinx FPGA/CPLDs: Spartan-6 LXT

The Xilinx® Spartan®-6 FPGA Connectivity Kit is a complete, easy-to-use connectivity development and demonstration platform using the low-cost Spartan-6 LXT device family. As a Xilinx Connectivity Targeted Design Platform, this kit provides the hardware, software, IP, and Targeted Reference Designs needed to create high-speed serial systems and other connectivity applications right out of the box.

The Spartan-6 LXT FPGA enables designing with industry-standard high-speed serial protocols including PCI Express® (version 1.1), Ethernet (GMII, SFP), and DDR3, as well as enabling designs using other serial standards and proprietary implementations up to 3.125G/ps and multiple parallel protocols including 3.3V I/O standards.

The Connectivity Kit with Spartan-6 LXT FPGA simplifies design, development, and validation of multi-protocol systems with an efficient, low-cost programmable connectivity solution. Production-proven methodologies and tool suites delivered with the kit enable designers to analyze and debug high-speed serial solutions in real time.

The kit integrates the critical components of connectivity development to accelerate design, implement low-cost protocol bridging, and provide higher efficiency alternative to LVDS communication. It also serves as the starting point for market-specific connectivity design platforms with scalable building block architecture, Targeted Reference Designs, and hardware ecosystem of industry-standard FMC daughter card extensions.

FEATURES & BENEFITS

- ◆ Comprehensive connectivity development platform with all the hardware, software, firmware, IP, and reference designs needed to create fully functional working system
- ◆ ISE® Design Suite Logic and Embedded Editions tailored for system designers with ChipScope™ Pro Analyzer and Serial IO Toolkit (device-locked to Spartan-6 LX45T FPGA)
- ◆ Pre-verified, customizable Targeted Reference Design integrates PCIe®, Gigabit Ethernet, and on-board DDR3 memory with virtual FIFO and optimized Packet DMA to accelerate bandwidth
- ◆ Multiple example designs including hard memory controller, iBERT, and others



TECHNICAL SPECS

- ◆ RoHS-compliant SP605 board with Spartan-6 LX45T FPGA, universal power supply, and accessory cables
- ◆ On-board FMC daughter card connector for plug-in scalability
- ◆ USB flash drive with device driver files, design source files, applications
- ◆ Downloadable documentation with schematics, Gerber files, board BOM, and detailed user guides

AVAILABILITY

Available today at: www.xilinx.com/kits

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications

CONTACT INFORMATION



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Spartan-6 FPGA DSP Kit

Supported Xilinx FPGA/CPLDs: Spartan-6 LX, Spartan-6 LXT

The Xilinx® Spartan®-6 FPGA DSP Kit provides a complete development platform for implementing DSP algorithms on low-cost, low power Spartan-6 FPGAs. As a Xilinx DSP Targeted Design Platform, this kit provides the hardware, software, IP, and Targeted Reference Designs needed to get started right out of the box.

At the heart of the Spartan-6 FPGA DSP Kit is the Avnet AS-LX150T development board featuring the Spartan-6 LX150T device. The Spartan-6 FPGA family offers an optimized balance of connectivity, memory, and DSP hardware resources. As the largest device in the family, the Spartan-6 LX150T FPGA provides more than enough hardware resources for even the most demanding high-volume DSP applications.

With the Spartan-6 DSP Development Kit, system designers spend less time developing the infrastructure of a design and more time building differentiating features into DSP applications. The kit also serves as the starting point for market-specific DSP design platforms with scalable building block architecture, Targeted Reference Designs, and hardware ecosystem of industry-standard FMC daughter card extensions.

FEATURES & BENEFITS

- ◆ High-volume DSP applications using Spartan-6 LX150T FPGA with 180 enhanced DSP48E1 slices that deliver up to 50 GMACs of DSP performance
- ◆ Develop DSP applications without RTL design experience using System Generator for DSP software with The Mathworks Simulink® and MATLAB® DSP modeling environments
- ◆ Targeted Reference Designs supply pre-verified design infrastructure and starting point for DSP development
- ◆ Extensible to vertical market applications with two industry-standard FMC connectors and ecosystem of FMC I/O daughter card providers
- ◆ Get started quickly with graphical user interface that guides new users on basic kit operation



TECHNICAL SPECS

- ◆ Avnet Spartan-6 LX150T development board with the Spartan-6 LX150T FPGA
- ◆ ISE® Design Suite: System Edition (device locked to Spartan-6 LX150T FPGA)
- ◆ Simulink-based DUC/DDC and RTL-based DUC/DDC Targeted Reference Designs
- ◆ Comes complete with cables, power supply, and compact flash
- ◆ Downloadable documentation with Hardware Setup and Getting Started Guides

AVAILABILITY

Available Today at <http://www.xilinx.com/kits>

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Medical Imaging, Wireless Communications

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Spartan-6 FPGA Evaluation and Development Kits

Supported Xilinx FPGA/CPLDs: Spartan-6 LX, Spartan-6 LXT

Xilinx and Avnet provide a comprehensive offering of Spartan®-6 FPGA evaluation and development kits that enable designers to achieve an optimum balance of cost, power and performance.

Xilinx® Spartan-6 FPGA SP601 and SP605 Evaluation Kits simplify development of FPGA-based SoCs for consumer, infotainment, video, and other cost or power-sensitive applications. As a Xilinx Base Targeted Design Platform, each kit provides the hardware, software, IP, example designs, and documentation needed to design right out of the box.

The SP601 Evaluation Kit is a low-cost, entry-level environment for evaluating the Spartan-6 FPGA family with system design capabilities that include DDR2 memory control, flash, Ethernet, general-purpose I/O, and UART to name a few. The SP605 Evaluation Kit is a highly scalable base platform for developing low-cost applications requiring connectivity with high-speed serial transceivers, DDR3 memory control, DVI, parallel linear flash, and Tri-mode Ethernet.

Avnet introduces the first-ever battery-powered Xilinx FPGA development board with the Xilinx Spartan-6 LX16 Evaluation Kit, featuring Texas Instruments battery management devices and power regulation circuitry and the Cypress PSoC® 3 Programmable System on Chip with embedded 8051 for an ultra-low-power controller. Avnet also offers the full-featured Xilinx Spartan-6 LX150T Development Kit for designing and verifying applications based on the Spartan-6 LXT FPGA family.

FEATURES & BENEFITS

- ◆ Xilinx SP601 and Avnet LX16 Evaluation Kits feature base board with Spartan-6 LX16 FPGA and ISE® WebPACK™ Design Suite (supporting Windows and Linux)
- ◆ Xilinx SP605 Evaluation Kit features base board with Spartan-6 LX45T FPGA and ISE Design Suite Logic Edition (device-locked)
- ◆ Avnet LX150T Development Kit features base board with Spartan-6 LX150T FPGA and ISE Design Suite Logic Edition (device-locked)
- ◆ Base reference design with Gigabit host communication, DDR2/DDR3 interface, and example programmable processing and serial loopback optimized for Spartan-6 FPGAs
- ◆ Complete with universal power supply, accessory cables, and downloadable documentation with schematics, Gerber files, board BOM, and detailed user guides



TECHNICAL SPECS

- ◆ Xilinx SP601 Evaluation Kit for low-cost Spartan-6 FPGA evaluation
- ◆ Xilinx SP605 Evaluation Kit for low-cost connectivity applications
- ◆ Avnet LX16 Evaluation Kit for low-power, battery-power applications such as handheld data gathering, human machine interface, and embedded control
- ◆ Avnet LX150T Development Kit for PCI Express® bridges, Ethernet/Internet and video applications, and embedded controllers
- ◆ All kits feature industry-standard FPGA Mezzanine Card (FMC) connector enabling scaling and customization of base boards for specific application and market needs

AVAILABILITY

Available today at: www.xilinx.com/kits

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications

CONTACT INFORMATION



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Xilinx, Inc.

Spartan-6 FPGA Market-specific Kits

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Spartan-6 LXT

Xilinx® Spartan®-6 FPGA market-specific kits simplify the development of cost and power-sensitive electronics systems, such as digital displays, industrial networking, industrial video processing, automotive infotainment, and broadcast connectivity applications among others.

Spartan-6 FPGA market-specific kits provide all the elements needed to design right out of the box, enabling system designers to accelerate innovation and improve differentiation of lower power 'greener' products. Spartan-6 FPGAs offer an optimal balance of cost, power, and performance for consumer, automotive, surveillance, wireless, and other high-volume markets. They provide twice the capability at half the power consumption of previous generations, while reducing system costs by up to 50 percent.

The first in the series of these market-specific kits is the Spartan-6 FPGA Consumer Video Kit providing a programmable Targeted Design Platform specifically optimized for creating digital TV system designs. This easy-to-use and scalable kit includes a base development board along with several FMC daughter cards, Xilinx and third-party soft IP logic blocks supporting emerging and de facto standard high-speed display interfaces, complete design environment, and Targeted Reference Designs. The kit streamlines algorithm development on Spartan-6 FPGA-based systems and gives systems designers a jumpstart on bringing differentiated products to market quickly.

FEATURES & BENEFITS

- ◆ Comprehensive video algorithm development platform with all the hardware, software, firmware building blocks, and tools needed to get started out of the box
- ◆ RoHS-compliant boards enable integration of picture quality algorithms with DDR3, DisplayPort 1.1, V-by-One®HS, HDMI 1.3, PCI Express®, 1.05Gb/s LVDS, UART interfaces
- ◆ Targeted Reference Designs with DisplayPort 1.1, V-by-OneHS, HDMI 1.3, 1.05Gb/s LVDS, multi-port DDR3 memory controller, UART, SPI, I2C, timers, interrupt controller and on-chip memory
- ◆ Multiple examples demonstrate how to customize the video algorithm design and provide best practices for compiling, debugging, and profiling Spartan-6 FPGA-based video applications



TECHNICAL SPECS

- ◆ Base development board with Spartan-6 LX150T FG676 device, universal power supply, and accessory cables
- ◆ Ecosystem of industry-standard FMC daughter cards for DisplayPort 1.1, HDMI 1.3, V-by-OneHS, and 1.05 Gb/s LVDS (also compatible with Virtex®-6 LXT FPGA)
- ◆ ISE® Design Suite Embedded Edition with Platform Studio tools, EDK, and SDK (device locked to Spartan-6 LX150T FPGA)
- ◆ USB stick with device driver files, design source files, and applications
- ◆ Complete documentation with detailed User Guide

AVAILABILITY

For the latest information on Spartan-6 FPGA market-specific kits as they become available, visit: www.xilinx.com/kits

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications

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Virtex-6 FPGA DSP Kit

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT

The Xilinx® Virtex®-6 DSP Development Kit provides a complete development platform for implementing DSP algorithms on high performance Virtex-6 FPGAs. As a Xilinx DSP Targeted Design Platform, this kit provides the hardware, software, IP, and Targeted Reference Designs needed to get started right out of the box.

The Virtex-6 FPGA DSP Kit features the Xilinx ML605 development board with the Virtex-6 LX240T device. With over 700 DSP48 slices delivering in excess of 400 GMACs of DSP processing bandwidth, this development platform is ideal for high performance wireless communications, aerospace and defense applications.

With the Virtex-6 DSP Development Kit, system designers spend less time developing the infrastructure of a design and more time building differentiating features into DSP applications. The kit also serves as the starting point for market-specific DSP design platforms with scalable building block architecture, Targeted Reference Designs, and hardware ecosystem of industry-standard FMC daughter card extensions.

FEATURES & BENEFITS

- ◆ High performance DSP applications using Virtex-6 LX240T FPGA with 788 enhanced DSP48E1 slices that deliver up to 472 GMACs of DSP performance
- ◆ Develop DSP applications without RTL design experience using System Generator for DSP software with The Mathworks Simulink® and MATLAB® DSP modeling environments
- ◆ Targeted Reference Designs supply pre-verified design infrastructure and starting point for DSP development
- ◆ Extensible to vertical market applications with two industry-standard FMC connectors and ecosystem of FMC I/O daughter card providers
- ◆ Get started quickly with graphical user interface that guides new users on basic kit operation



TECHNICAL SPECS

- ◆ Xilinx ML605 development board with Virtex-6 LX240T FPGA
- ◆ ISE® Design Suite: DSP Edition (device-locked to Virtex-6 LX240T FPGA)
- ◆ Simulink-based DUC/DDC and RTL-based DUC/DDC Targeted Reference Designs
- ◆ Comes complete with cables, power supply, and compact flash
- ◆ Downloadable documentation with Hardware Setup and Getting Started Guides

AVAILABILITY

Available Today at <http://www.xilinx.com/kits>

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Medical Imaging, Wireless Communications

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Xilinx, Inc.

Virtex-6 FPGA Market-specific Kits

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT, Virtex-6 HXT

Xilinx® Virtex®-6 FPGA market-specific kits enable developers to build high-bandwidth and high-performance wireless/wired communications, broadcast, and aerospace/defense electronics systems under tighter design cycles with lower development costs.

Virtex-6 FPGA market-specific kits provide all the elements hardware and software developers need to quickly create and run high performance, compute-intensive applications right out of the box. At up to 50 percent lower power and 20 percent lower cost than previous generations, Virtex-6 FPGAs deliver more computational performance and faster networking capabilities, while lowering system costs through integration. The first in the series of these market-specific kits is the Virtex-6 FPGA Broadcast Connectivity Kit that simplifies serial digital interface (SDI) development for high performance broadcast audio and video applications. The kit provides a Connectivity Targeted Design Platform specifically optimized for the creation of multi-protocol broadcast systems that require high-bandwidth and low-power serial connectivity.

The Virtex-6 FPGA Broadcast Connectivity Kit includes a base development board along with FMC card supporting digital audio and video interfaces and protocol bridging technologies, complete design environment, and Targeted Reference Designs for SDI interfaces based on SMPTE standards with support for multiple channels of SD, HD, and 3G-SDI video in a single Virtex-6 device.

FEATURES & BENEFITS

- ◆ Targeted Design Platform tuned to the needs of high performance broadcast audio, video and network connectivity applications
- ◆ Enables broadcast equipment engineers to focus on product differentiation rather than challenges of implementing multiple SDI rates and formats
- ◆ Out-of-the-box system design with hardware, software, Targeted Reference Designs, evaluation IP, and documentation to shorten development and integration cycles
- ◆ Full support for triple rate SDI, AES audio, and video over IP designs with scalable platform for bridging to DVI, PCI Express, DisplayPort, and 10Gb Ethernet standards



TECHNICAL SPECS

- ◆ ML605 base board with the Virtex-6 LX240T-1FFG1156 device that includes up to 24 power-optimized high-speed transceivers supporting line rates of up to 6.5Gb/s
- ◆ Industry-standard FMC Broadcast Mezzanine Card supporting 4x SD/HD/3G-SDI Tx and Rx, 2x AES3 Tx and Rx, 1x AES10 Tx and Rx, and video sync input
- ◆ Two optional reference clock cleaner modules
- ◆ ISE® Design Suite: Logic Edition (device-locked to Virtex-6 LX240T FPGA)
- ◆ USB flash drive with out-of-the-box demos, Targeted Reference Designs, documentation, and applications

AVAILABILITY

For the latest information on Virtex-6 FPGA market-specific kits as they become available, visit <http://www.xilinx.com/kits>

APPLICATION AREAS

Aerospace/Defense, Broadcast, Wired Communications, Wireless Communications

CONTACT INFORMATION



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Xilinx Embedded Kits

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Spartan-6 LXT

Supported Architecture: Other - MicroBlaze

Xilinx® Embedded Kits simplify development of embedded processor systems on chip with Virtex®-6 FPGA and Spartan®-6 FPGAs. As Xilinx Embedded Targeted Design Platforms, these kits provide the hardware, software, IP, and Targeted Reference Designs needed to create embedded systems right out of the box.

The Virtex-6 FPGA Embedded Kit is a full-featured environment for developing embedded applications that demand high performance processing, serial connectivity, and advanced memory interfacing. The Spartan-6 FPGA Embedded Kit provides a low-cost base platform for embedded applications requiring connectivity. Both kits come with the MicroBlaze™ Processor Subsystem Targeted Reference Design as a starting point for hardware customization and software development, as well as a video processing design example and detailed tutorial demonstrating how to further customize the system.

For standalone (or bare-metal) software development, an Eclipse-based Software Development Kit (SDK) is provided with GNU tools, wizards for creating software applications and linker scripts, flash writer, standard 'C' libraries and drivers for embedded peripherals. Linux or RTOS-based software development is supported with an ecosystem of third-party operating system and middle-ware solutions that work seamlessly with the Xilinx SDK.

FEATURES & BENEFITS

- ◆ Comprehensive development platforms with all the hardware, software, firmware building blocks, and tools needed to jumpstart application development
- ◆ RoHS-compliant boards enable integration of embedded processor subsystem with DDR3, PCI Express®, Gigabit Ethernet, UART interfaces and industry-standard FMC for plug-in scalability
- ◆ Targeted Reference Design with MicroBlaze processor, multi-port DDR3 memory controller, Tri-mode Ethernet MAC, UART, SPI, I2C, timers, interrupt controller and on-chip memory
- ◆ Multiple examples demonstrate how to customize the design and provide best practices for compiling, debugging, and profiling software applications
- ◆ Linux and RTOS support includes PetaLinux OS from PetaLogix, uC/OS-II and uC/TCP-IP ports from Micrium with uC/Probe debug tools and Treck high performance TCP/IP stack



TECHNICAL SPECS

- ◆ Virtex-6 FPGA Embedded Kit: ML605 base board with Virtex-6 LX240T FG1156 device, universal power supply, and accessory cables
- ◆ Spartan-6 FPGA Embedded Kit: SP605 base board with Spartan-6 LX45T FG484 device, universal power supply, and accessory cables
- ◆ ISE® Design Suite Embedded Edition with Platform Studio tools, EDK, and SDK (locked to Virtex-6 LX240T or Spartan-6 LX45T FPGA)
- ◆ USB flash drive with out-of-box demos, Targeted Reference Design sources, hardware and software tutorials
- ◆ Downloadable documentation with schematics, Gerber files, board BOM, and detailed user guides and datasheets

AVAILABILITY

Virtex-6 FPGA Embedded Kit available today at:
www.xilinx.com/v6embkit

Spartan-6 FPGA Embedded Kit available today at:
www.xilinx.com/s6embkit

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging

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Xilinx Transceiver Characterization Kits

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT

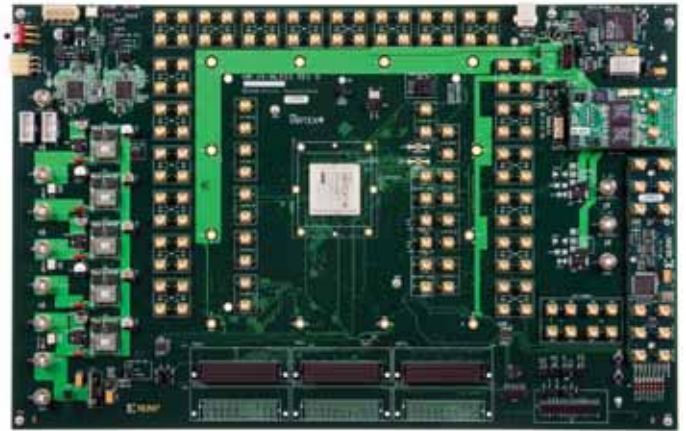
Xilinx® Virtex®-6 FPGA ML623 and Spartan®-6 SP623 Transceiver Characterization Kits simplify the evaluation of Xilinx GTX and GTP low-power, high-speed serial transceivers with the latest generation devices and Xilinx Targeted Design Platforms.

The kits provide hardware and software developers with everything needed to create and fully characterize designs with Virtex-6 FPGA GTX and Spartan-3 FPGA GTP multi-gigabit transceivers, including the ML623 and SP623 characterization boards, ChipScope™ Pro IBERT reference design, PCB design files, and documentation.

The ML623 characterization board features 24 GTX transceivers with high performance Virtex-6 LX240T FPGAs. Virtex-6 FPGA GTX transceivers are ideal for higher bandwidth, low-power connectivity applications with line rates from 750Mb/s to 6.5Gb/s. The SP623 characterization board provides access to 8 GTP transceivers with low-cost, low-power Spartan-6 LX150T FPGAs that offer the lowest risk, lowest cost serial connectivity with line rates from 614Mb/s to 3.125G/ps. Each GTX and GTP transceiver is accessible via four SMA connectors.

FEATURES & BENEFITS

- ◆ GTX transceivers offer industry's best signal integrity with eight programmable levels of Transmit Pre-emphasis and four programmable levels of Receive Equalization
- ◆ GTP transceivers are power-optimized for 150-180mW per transceiver with programmable Transmit Pre-emphasis and Receive Equalization
- ◆ GTX and GTP transceivers are automatically configured with the Xilinx CORE Generator™ software to support different protocols or perform custom configuration



TECHNICAL SPECS

- ◆ ML623 characterization board with Virtex-6 LX240T-FF1156 devices
- ◆ SP623 characterization boards available with Spartan-6 LX150T-FGG676 devices
- ◆ Configured with SystemACE 2G CF card, JTAG, USB to UART bridge and USB host controller, LED displays, and control buttons/switches
- ◆ Industry-standard low-pin count FMC connector
- ◆ Selectable 1.0V or 1.2V VCCINT jumper cable and 3.3V, 2.5V, 1.8V, and 1.2V power supplies

AVAILABILITY

Available Today at <http://www.xilinx.com/kits>

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications

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Virtex-6 FPGA Connectivity Kit

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT

The Xilinx® Virtex®-6 FPGA Connectivity Kit is a comprehensive connectivity development and demonstration platform using the high-performance Virtex-6 LXT FPGA family. As a Xilinx Connectivity Targeted Design Platform, this kit provides the hardware, software, IP, and Targeted Reference Designs needed to create high-speed serial and other connectivity applications right out of the box.

The Virtex-6 LXT FPGA enables designing with PCI Express® 1.1/2.0, Ethernet (GMII, SFP, XAUI), SATA, and other proprietary high-speed serial protocols with line rates up to 6.5Gb/s, as well as multiple parallel standards running at ~ 1.4Gb/s with SelectIO technology.

The Connectivity kit with Virtex-6 LXT FPGA simplifies design, development, and validation of high performance and high bandwidth multi-protocol systems amidst changing market requirements. Production-proven methodologies and tool suites delivered with the kit enable designers to analyze and debug high-speed serial solutions in real time.

The kit jumpstarts development with a Targeted Reference Design that integrates PCI Express and XAUI IP in a working system that accesses on-board DDR3 memory through a virtual FIFO and accelerates bandwidth with an optimized high-performance packet DMA. The kit also serves as a starting point for market-specific targeted design platforms with scalable building block architecture, Targeted Reference Design, and hardware ecosystem of industry-standard FMC daughter card extensions.

FEATURES & BENEFITS

- ◆ Comprehensive development platform with all the hardware, software, firmware, application IP and GUI to create a fully functional system solution
- ◆ ISE® Design Suite Logic and Embedded Editions tailored for system designers with ChipScope™ Pro Analyzer and Serial IO Toolkit (device locked to Virtex-6 LX240T FPGA)
- ◆ Pre-verified, customizable and fully supported Targeted Reference Design for PCIe-10GDMA-DDR3-XAUI
- ◆ Multiple example designs including SFI4.1, SFI5, and PCIe 2.0 and 1.1 multi-lane configurations



TECHNICAL SPECS

- ◆ RoHS-compliant ML605 base board with Virtex-6 LX240T device
- ◆ Universal power supply and accessory cables including CX4 loopback module
- ◆ VITA57-compliant FMC daughter card with CX4, SATA, and SMA interfaces
- ◆ USB flash drive with device driver files, design source files, and applications
- ◆ Downloadable documentation with schematics, Gerber files, board BOM, and detailed user guides

AVAILABILITY

Available today at: www.xilinx.com/kits

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications

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Alpha Data

ADM-XRC-6T1 - Xilinx Reconfigurable Computer - XMC

Supported Xilinx FPGA/CPLDs: Xilinx Virtex6 : LX240T, LX365T, LX550T, SX315T, SX475T

The ADM-XRC-6T1 is a high performance reconfigurable XMC (VITA 42.3 Mezzanine Card) based on the Xilinx® Virtex-6 LXT and SXT ranges of Platform FPGAs.

Features include PCI Express® Gen2 interface, external memory, high density I/O, temperature monitoring, battery backed encryption and flash boot facilities. A comprehensive cross platform API with support for Microsoft Windows™, Linux and VxWorks™ provides access to the full functionality of these hardware features.

FEATURES & BENEFITS

- ◆ A comprehensive cross platform API with support for Microsoft Windows™, Linux and VxWorks™ provides access to the full functionality of these hardware features.
- ◆ Alpha Data mezzanine boards provide support for many different physical interfaces and connectivity requirements. Front panel I/O can be customized with a large selection of I/O adapters (XRM modules) that connect to a base FPGA card.
- ◆ Up to 146 digital I/O signals, x8 Rocket I/O lanes ADC inputs up to 3Gsps, DAC outputs 2.3GHz Ethernet, CX4, Fiber-Optics, CameraLink, LVDS, RS-485, FPDP, SMPTE, DVI, and many more Custom I/O adapters are also available
- ◆ The Virtex®-6 family provides the newest, most advanced features in the FPGA market.
- ◆ Industrial operating temperature and ruggedized options available

TECHNICAL SPECS

- ◆ **Board Format:** XMC
Host I/F: PCI Express Gen2 x4



- ◆ **Memory:**
 - SDRAM** - 1GByte in 4 independent banks (2GByte option) of DDR3 SDRAM @ 800MT/s (32-bit wide 3.2GB/s)
 - FLASH** - Configuration Flash providing an initialization design for automatic loading into the target FPGA.
- ◆ **Front Connector I/O:**
Up to 146 LVCMOS/LVDS I/O. Programmable signaling levels of 1.5V, 1.8V or 2.5V. 8 High-Speed Serial Links
- ◆ **Rear Connector I/O:**
 - 8 Serial Links (allowing second x4 PCI Express® Gen 2 channel)
 - 10 Serial Links (VITA 46.9 X8d+X12d)
 - 38 LVTTTL GPIO connections (VITA 46.9 X38s)
 - 64 I/O connections (2.5V levels with 3.3V compatible inputs)
- ◆ **Applications:**
 - Radar/Sonar Beamforming
 - ELINT
 - Fingerprint Recognition
 - Data Encryption

AVAILABILITY

Now

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Medical Imaging, Wired Communications

CONTACT INFORMATION



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VCP-8166

Supported Xilinx FPGA/CPLDs: Xilinx Spartan-6

Other Supported Xilinx FPGA/CPLDs:

The VCP-8166 is designed for real-time video compression/decompression of 2 HD-SDI channels in parallel. It features several SDI I/O solutions (1 onboard, 2 on P6, 1 parallel on P4) compatible with SD and HD input signals at up to 3 Gb/s. HDMI I/O and several analog input formats are also supported. The advanced video coding functionality is provided to guarantee real-time, high-quality and low-latency coding up to HD formats. Compressed video is available from the processor board via PCI or PCIe. Both video channels can be processed at the same time and inputs can be duplicated. Scaling down of frame rate and size is possible, as well as control of bitrate, quality and frame cropping. Further channels can be processed at lower resolutions.

TECHNICAL SPECS

- ◆ Air-cooled/conduction-cooled Video PMC or XMC with Xilinx Spartan-6 LX100T FPGA + dedicated H.264 co-processor
- ◆ Multi-stream H.264 / AVC Baseline Profile Codec (+ interlaced format support in Main Profile)
- ◆ Multiple HD-SDI input and output (1.5 Gbits/s and 3.0 Gbits/s HD) / HD-SDI parallel input on P4
- ◆ HDMI video input and output / Analog video input (HD, NTSC, PAL, RGB). Uncompressed video frame capture available on PCIe
- ◆ Stand-alone video over Ethernet (MicroBlaze). Audio analog / AC97 input/output

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Perseus 601X

Supported Xilinx FPGA/CPLDs: Virtex-6

The Perseus 601X AMC is designed around the powerful Virtex-6 FPGA, combining unsurpassed fabric flexibility and a colossal external memory, as well as benefiting from multiple high-pin-count, modular add-on FMC-based I/O cards.

The Perseus 601X is intended for high-performance, high-bandwidth, low-latency processing applications, drawing from the Virtex-6 FPGA's power and combining it to Lyrtech's advanced software development tools. The result: an AMC capable of reducing the size, complexity, risks and costs of leading-edge telecommunications, networking, industrial, defense and medical applications. Moreover, the Perseus 601X's FMC expansion site offers almost endless I/O possibilities — A/D & D/A conversion, SFP(+), RF transceivers, etc.

The FPGA and IPMI JTAGs are available from the standard AMC backplane or from the onboard Mestor interface. Lyrtech offers two optional Mestor debugging modes: Mestor-to-FPGA JTAG adapter that offers a direct, onboard access to the FPGA's JTAG chain, and the Mestor expander that offers front-panel accesses to the FPGA and IPMI JTAGs, 14 user LVDS I/Os, one clock, and an FPGA UART interface (serial RX/TX — Mini-B USB).

The Perseus 601X also comes with a comprehensive set of integrated, multilayer software development tools that offer users a choice of environments — from a base-level hand-coded design environment (board software development kit) to a high-level graphical model-based design environment (model-based design kit).

FEATURES & BENEFITS

- ◆ Mid-size AMC for μ TCA and AdvancedTCA platforms
- ◆ Choice of powerful LXT and SXT Virtex-6 FPGAs
- ◆ High-pin-count VITA 57.1 FMC expansion site for I/Os
- ◆ DDR3 SODIMM interface to upgrade system memory
- ◆ Supports multiple switch fabrics (PCIe, SRIO, XAUI, GigE)



TECHNICAL SPECS

- ◆ Xilinx Virtex-6 FPGA
 - Perseus 6010: LX240T
 - Perseus 6011: LX550T
 - Perseus 6012: SX315T
 - Perseus 6013: SX475T
- ◆ Default 1 GB, 64-bit DDR3 SDRAM SODIMM
- ◆ Mid-size and full-size AMC compliant
- ◆ High-pin-count VITA 57.1 FMC site
- ◆ IPMI controller (based on the AVR version of the Pigeon Point AdvancedMC MMC)

AVAILABILITY

Now

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Medical Imaging, Wired Communications, Wireless Communications

CONTACT INFORMATION



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www.lyrtech.com

Now Shipping The NEW Cobalt Series of Virtex-6 VPX Modules!



Pentek's Cobalt™ family of Virtex-6 products provide the newest, most advanced features in the FPGA market. In addition to the high-performance logic fabric, Virtex-6 FPGAs contain many built-in system-level blocks. These features allow logic designers to build the highest levels of performance and functionality into their FPGA-based systems.

Model 53620

A/D & D/A Virtex-6 FPGA
COTS and Rugged Board

Cobalt Virtex-6 FPGA Boards:

- 1 GHz A/D & D/A (Model 53630)
- 2 Ch 500 MHz A/D & 2 Ch 800 MHz D/A (Model 53650)
- 3 Ch 200 MHz A/D & 2 Ch 800 MHz D/A (Model 53620)
- 3 Ch 200 MHz A/D, 2 Ch 800 MHz D/A, DUC & DDC (Model 53621)
- 4 Ch 200 MHz & 16-bit A/D (Model 53660)
- 4 Ch 200 MHz & 16-bit A/D with Multiband DDC (Model 53661)
- L-Band RF Tuner with 2 Ch 200 MHz A/D (Model 53690)

Cobalt Products Include:

- A/D sampling ranges from 10 MHz to 1 GHz
- Dedicated memory for each I/O stream
- Intelligent chaining DMA engines
- Secondary serial gigabit interface
- Multichannel, multiboard synchronization
- ReadyFlow® Board Support Libraries
- GateFlow® FPGA Design Kit & Installed IP
- Ideal for wideband communications, radar, SIGINT and beamforming
- VPX, XMC, PCI, PCIe, cPCI, VME, VXS, Rugged



High Performance L-Band Reception

Pentek recently announced the Model 71690 L-Band RF tuner and dual digitizer module with on-board Xilinx Virtex-6 FPGA. The instrument targets reception and processing of digitally-modulated RF signals such as satellite television and terrestrial wireless communications. The Model 71690 requires only an antenna and a host system, such as a personal computer, to form a complete L-band SDR development platform.

- Directly acquires L-Band RF signals as low as -75 dBm from antenna connection
- Amplifies and downconverts RF, then digitizes I & Q signals at 200 MSPS
- Supports digital demodulation of satellite and telecommunications signals
- Onboard Virtex-6 FPGA preconfigured with data acquisition and radio tuning features

For more information on the Cobalt product family, go to www.pentek.com/go/cobaltguide.



Putting FPGAs to Work for Software Radio Handbook

Written by Rodger Hosking, Vice President and Co-founder of Pentek

FPGAs are becoming an increasingly important resource for software radio systems. This handbook introduces the basics of software radio followed by a brief review of the evolution of programmable logic technology which now offers significant advantages for implementing software radio functions.

An overview of Pentek's GateFlow FPGA Design Resources is followed by product descriptions and finally by some software radio system examples that utilize FPGA technology.

Download at: www.pentek.com/go/fpgaguide

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Setting the Standard for Digital Signal Processing

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Scan Engineering Telecom

SAMC-713 High performance Virtex-6 AMC with VITA 57.1 expansion site

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT, Virtex-6 SXT

The SAMC-713 Advanced Mezzanine Card (AMC) is designed around Virtex-6 FPGA LXT and SXT families, combining great fabric flexibility and a colossal external memory benefiting from multiple high-pin-count, modular add-on FMC-based I/O cards.

The SAMC-713 is designed for applications requiring high performance, high bandwidth and low latency. The board takes full advantage of the Virtex-6 FPGA's power which makes the SAMC-713 perfect for reducing size, complexity and costs associated to leading-edge telecommunications, networking, data processing, industrial and medical applications. Moreover, FMC expansion site on the board offers almost unlimited I/O possibilities.

Combining Virtex-6 FPGAs LXT (up to VLX365T) or SXT (up to VSX475T) with four independent 2Gb DDRIII SDRAM memory banks and twelve high performance full-duplex GTX lines supporting Gigabit Ethernet, PCI express x1..x8 and Serial RapidIO x1..x4 The SAMC-713 gives OEMs an effective solution for wide range of applications. Scan Engineering Telecom also provides customization, turnkey integration and support to ensure that OEMs can focus where they prefer to add their own unique value.

FEATURES & BENEFITS

- ◆ High performance AMC FPGA board with FMC expansion site
- ◆ Combines great Xilinx Virtex-6 FPGAs power, colossal amount of memory and numerous interface lines
- ◆ Cost-effective platform for xTCA-based solutions
- ◆ For OEMs in telecom, datacom, industrial, medical, test & measurement and defence & aerospace industries

TECHNICAL SPECS

- ◆ Virtex-6 FPGA (from LX130T/195T/240T/365T to SX315T/475T), 20000-74400 Logic Slices, 9500-38300Kbit Block RAM, 480-2016 DSP48E1 Slices, up to 1000GMACS of processing power



- ◆ Four independent 2Gb DDRIII SDRAM memory banks, total memory capacity 8Gb
- ◆ 12 full-duplex lines provides Gigabit Ethernet and PCI Express x1..x8 or Serial Rapid IO x1..x4 interfaces
- ◆ VITA 57.1 (FMC) expansion site, supports air cooled commercial and conduction cooled with region 1 form-factors with or w/o front panel
- ◆ Single Mid-Size or Single Full-Size AMC board

AVAILABILITY

Available now

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications, Other (please state below)

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XDSP-55 Programmable FPGA Accelerator board

Supported Xilinx FPGA/CPLDs: Virtex-4 LX, Virtex-4 SX

The XDSP-55 FPGA accelerator board is intended for high-performance SDR or data processing applications. The board also takes full advantage of the Virtex-4 FPGA's power, which makes the XDSP-55 perfect for telecommunications, networking, industrial, defense and medical applications based on CompactPCI form-factor and supports PCI 33/66MHz 32/64bit.

The XDSP-55 design is based on combined power of two Virtex-4 FPGAs which are operating as main FPGAs while service FPGA provides management and interconnection to the backplane. Using most powerful Virtex-4 FPGAs the board provides over 300000 logic cells or up to 1024 Xtreme DSP blocks while four ZBT SRAM memory banks connected to each main FPGA provides interconnect frequency up to 200MHz.

On top of this the XDSP-55 has reference quartz oscillator provides base frequency at 200MHz and frequency range from 10 to 550MHz. The board also has full-duplex LVDS channel for integration with other boards in CompactPCI chassis and speed over 800Mbit/s in each direction.

The XDSP-55 is intended for OEMs in telecommunications, data communications, industrial, defence & aerospace and medical markets.

FEATURES & BENEFITS

- ◆ CompactPCI form-factor, supports PCI 33/66MHz 32/64bit
- ◆ Two main FPGAs and one service FPGA from Xilinx Virtex-4 LX or SX families
- ◆ Four ZBT SRAM memory banks for each of main FPGA with high throughput
- ◆ Full-duplex LVDS channel, interconnection speed over 800Mbit/s in each direction
- ◆ Commercial (0...+50C) and industrial (-40...+85C) temperature range



TECHNICAL SPECS

- ◆ Two main FPGAs, each can be Xilinx Virtex-4 (LX40-LX160 or SX55), for each FPGA: over 152000 logic cells (LX160), up to 512 Xtreme DSP blocks (SX55), up to 5760 kbit Block RAM (SX55)
- ◆ Four 72Mbit ZBT SRAM memory banks for each main FPGA, 72MB for total memory
- ◆ 256Mbit of nonvolatile Flash memory for main FPGAs configurations and 8Mbit of nonvolatile Xilinx PlatformFLASH memory for Service FPGA configuration
- ◆ Reference quartz oscillator with base frequency 200MHz, frequency range 10..550MHz and stability from 50ppm
- ◆ CompactPCI 3U 4HP board in commercial (0...+50C) or industrial (-40...+85C) temperature range

AVAILABILITY

Now

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Wired Communications, Wireless Communications

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Virtex-6 FPGA ML605 Evaluation Kit

Supported Xilinx FPGA/CPLDs: Virtex-6 LXT

The Xilinx® Virtex®-6 FPGA ML605 Evaluation Kit provides a development environment for system designs that demand high performance, serial connectivity and advanced memory interfacing. As a Xilinx Base Targeted Design Platform, the kit provides all the hardware, software, IP and targeted reference designs needed to design right out of the box

The ML605 Evaluation Kit simplifies development of systems-on-chip (SoC) for wired telecommunications, wireless infrastructure, broadcast, and other high performance applications. Integrated tool suites streamline creation of elegant solutions to complex design requirements. Multiple pre-verified targeted reference designs jumpstart development. Industry-standard FPGA Mezzanine Card (FMC) base boards and daughter card extensions provide plug-in scaling and customization.

The ML605 Evaluation Kit with Virtex-6 LX240T FPGA enables 50 percent lower power and 20 percent lower cost designs than previous generations. System-level capabilities include built-in high-speed serial transceivers, PCI Express® 2.0 Endpoint blocks, and DDR3 memory control to name just a few.

The kit is also supported by mainstream industry standard peripherals, such as PCI Express x8 edge connector (version 1.1 and 2.0), Tri-mode Ethernet, DDR-3 SO-DIMM, BPI linear flash, USB 2.0 (host and device), DVI output, SFP, LCD character display, GTX port (TX, RX) with four SMA connectors and two VITA-57 compliant FMC connectors.

FEATURES & BENEFITS

- ◆ Full-featured FPGA evaluation board with x8 PCI Express and standalone form factor
- ◆ ISE® Design Suite: Logic Edition tailored for logic and connectivity designers (Device-locked to Virtex-6 LX240T FPGA)
- ◆ Base reference design with Gigabit Ethernet, DDR3, DSP, and serial loopback
- ◆ Pre-verified demonstrations for PCI Express 2.0 x4 , PCI Express 1.1 x8, DDR3, ChipScope™ Pro Serial IO Toolkit IBERT transceiver test, and board diagnostic



TECHNICAL SPECS

- ◆ Virtex-6 FPGA ML605 board with Virtex-6 LX240T-1FFG1156 device, universal power supply, and accessory cables
- ◆ Communication and networking ports for PCI Express, Tri-mode Ethernet, USB 2.0, SFP, FMC, and SMA
- ◆ Supported by BPI Liner Flash and DDR3 memory
- ◆ Downloadable documentation with schematics, Gerber files, board BOM, and detailed user guides

AVAILABILITY

Available today at: www.xilinx.com/ml605

APPLICATION AREAS

Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications

CONTACT INFORMATION



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www.xilinx.com/ml605

Synplify Premier - Fast, Reliable FPGA Implementation and Debug

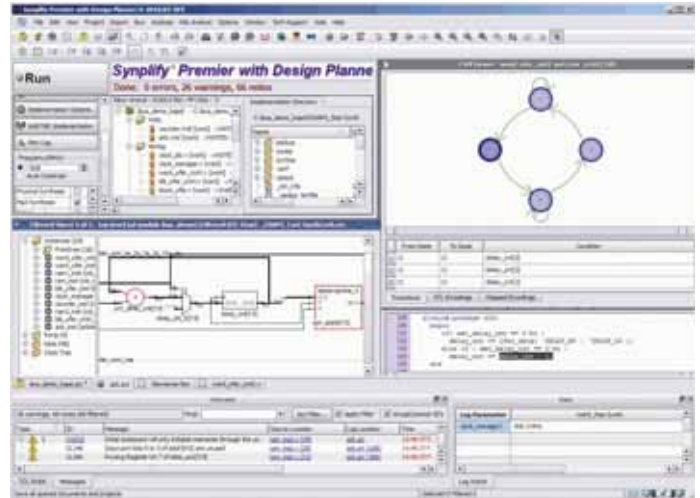
Supported FPGAs/CPLDs: All the major FPGA/CPLD families of devices from Achronix, Actel, Altera, Lattice Semiconductor, Silicon Blue and Xilinx are supported

As part of the Synopsys FPGA Design Solution, Synplify Premier software performs FPGA synthesis for programmable devices sold by Actel, Achronix, Altera, Lattice Semiconductor, SiliconBlue and Xilinx. The tool delivers the industry's best Quality of Results (QoR), rapid runtimes using incremental synthesis, FAST synthesis mode and automated block-based design. Automatic compile-point technology automatically shortens synthesis runtimes by leveraging multi-core computers. Team-design features allow design team members to perform parallel and distributed development autonomously, further increasing efficiency. The Synplify Premier tool's path-group technology makes design schedules more predictable by delivering results that are reproducible from one run to the next. The tool also delivers block-based RTL synthesis flows which fully integrate with 3rd party FPGA vendor block-based place and route design preservation flows, thereby shortening iteration runtimes, and preserving working, verified parts of the design from one run to the next.

For more information on Synplify Premier and other Synopsys FPGA implementation tools, visit us at www.synopsys.com/fpga

FEATURES & BENEFITS

- ◆ High reliability design for DO-254 compliance: Automatically implement safe FSMs and TMR insertion. Specify portions of the design to be preserved as debug logic or for deliberate redundancy purposes
- ◆ Fast synthesis mode: Synthesize even the largest design in a fraction of the time required by other tools
- ◆ DesignWare support: Easy ASIC code migration into an FPGA for prototyping. Integration with datapath and building block components in DesignWare IP
- ◆ Automatic handling of DSP function: Infer DSP functions from RTL and map into vendor's DSP hardware (e.g.: MACs, DSP48) for improved QoR
- ◆ Team-design: Faster design iterations and design preservation. Develop a design in parallel and/or distributed environment using bottom-up or hybrid flow. No floorplanning required



TECHNICAL SPECS

- ◆ Comprehensive language support including Verilog, VHDL, SystemVerilog and mixed-language
- ◆ Supports Windows XP Pro and Windows 7 (32/64 bit)
- ◆ Supports Linux, RHEL4, RHEL5, and SLES9 (32/64 bit)
- ◆ Minimum hardware requirements: CPU 1 GHz speed or better, RAM 2Gb, HDD 300Mb free space

AVAILABILITY

Synopsys' Synplify Premier FPGA implementation software is available now. Request a free evaluation at www.synopsys.com/fpga

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications

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Xilinx ISE Design Suite 12

The ISE® Design Suite 12 software unlocks greater design productivity with breakthrough technologies for power optimization and cost. The Design Suite enables the fastest time to design completion with Xilinx Targeted Design Platforms — available in four different configurations aligned to user preferred methodology—logic, embedded, DSP, or system design.

Available starting with the ISE Design Suite 12 release:

- “Intelligent” clock-gating technology that reduces dynamic power consumption by as much as 30 percent
- Advances in timing-driven design preservation, AMBA® 4 AXI4™-compliant IP support for plug-and-play design
- Intuitive design flow with fourth-generation partial reconfiguration capabilities that lowers system cost for a broad range of high performance applications

Xilinx Targeted Design Platforms provide embedded, DSP, and hardware designers alike with access to a wide array of silicon devices supported by open standards, common design flows, IP, and run-time platforms. The ISE Design Suite brings it all together with domain-specific design environments, while enabling design teams to meet their power and performance goals with Xilinx CPLDs and FPGAs, including the new Virtex®-6 and Spartan®-6 families.

ISE Design Suite provides a tight connection between embedded and DSP flows to enable integration of designs that contain embedded, DSP, IP, and user blocks in one system. To better serve users familiar with differing design environments, the ISE Design Suite 12 provides specific accommodations for designers ranging from the pushbutton user to the ASIC designer.

To learn more about the ISE Design Suite, and to download a full-featured 30-day evaluation version, please visit <http://www.xilinx.com/ise>

FEATURES & BENEFITS

- ◆ Four domain-specific solutions tailored for logic/connectivity, embedded, DSP, and system designers
- ◆ PlanAhead™ Design Analysis Tool for evaluation, analysis, and optimization of performance goals



- ◆ ChipScope™ Pro Analyzer and Serial IO Toolkit for real-time debug and verification
- ◆ Platform Studio Design Suite and EDK for IDE with embedded processing tools and design generators, MicroBlaze™ soft core, IP, software, and 3rd party interfaces
- ◆ System Generator for DSP for developing high performance DSP systems using products from The MathWorks, Inc.

TECHNICAL SPECS

- ◆ ISE Design Suite Logic Edition for logic and connectivity designers with the Xilinx Base Targeted Design Platform
- ◆ ISE Design Suite DSP Edition for algorithm, system, and hardware developers with DSP Domain Targeted Design Platform
- ◆ ISE Design Suite Embedded Edition for embedded system designers (both hardware and software programmers) with Embedded Domain Targeted Design Platform
- ◆ ISE Design Suite System Edition for system designers with Connectivity Domain

INDUSTRIES SERVED

Automotive, Aerospace and Defense, Broadcast, Consumer Electronics, Wired and Wireless Communications, as well as Industrial, Scientific and Medical Instrumentation

CONTACT INFORMATION



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TRACE32 PowerTools

Supported Xilinx FPGA/CPLDs: Virtex-5 LX, Virtex-5 LXT, Virtex-5 SXT, Virtex-5 FXT, Virtex-5 TXT, Virtex-4 LX, Virtex-4 SX, Virtex-4 FX, Virtex-II Pro, Virtex-II, Spartan-3/3E/3A/3AN, Spartan-3A DSP, Spartan-3 XA, Virtex-6 LXT, Virtex-6 SXT, Virtex-6 HXT, Virtex-6 CXT, Spartan-6 LX, Spartan-6 LXT

TRACE32 comprises a complete set of development and testing tools for the MicroBlaze, PowerPC PPC405, PPC440 and ARM Cortex processor IP. The modularity of TRACE32-PowerTools allows the user to extend the debugger with a trace extension and logic analyzer tools. The trace extension provides full support for program flow and data trace. In the context of FPGA system TRACE32-PowerTools enables the Xilinx ChipScope analyzer to access the target via the Lauterbach debug interface, fully parallel with an ongoing debugging session.

It also allows to configure the FPGA via the debugger and thus obviates the need for dedicated programming cables.

TRACE32 works with a high variety of host interfaces. The communication link to the host is done by USB or Ethernet, allowing a high-speed data transfer. It is possible to share TRACE32 tools in a LAN of PCs and workstations.

TRACE32-PowerTools are controlled by TRACE32-PowerView, a powerful IDE allowing HLL debugging on C or C++ level. It supports all third party compilers. TRACE32-PowerView allows unlimited software breakpoints and also supports the on-chip hardware break- and watch-points. A fast flash programming utility is included. The comfortable graphical user interface is completely configurable by the user. No other system offers more flexibility.

FEATURES & BENEFITS

- ◆ Interface to all compilers for C/C++
- ◆ RTOS awareness
- ◆ FLASH programming utility
- ◆ Cache debugging and MMU support
- ◆ Trace extension up to 550 MHz and 4 GByte trace memory

TECHNICAL SPECS

- ◆ Download speed up to 5 MByte/s
- ◆ Display of internal and external peripherals at a logical level (peripheral browser)
- ◆ Powerful script language
- ◆ High-speed link via Ethernet or USB
- ◆ Universal hardware for all supported debuggers



AVAILABILITY

All products are available.
More information can be found under:
http://www.lauterbach.com/pro_xilinx.html

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications

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FPGAs Pave Way for 5G, 400Gb/s Communications

By Gilles Garcia, director, Wired Communication Business Unit, Xilinx Inc.

The rapid proliferation of wirelessly interconnected technologies and their ability to handle music, streaming video, and live TV in addition to voice is creating an insatiable need to quickly transmit and receive ever larger amounts of data. This demand for bandwidth is creating tremendous pressure on network infrastructures and with it great opportunities for the electronics industry. The recent introduction of field programmable gate arrays (FPGAs) that can facilitate data rates of 400Gb/s is occurring at a time when the electronics industry is still in the process of creating and deploying infrastructure for 40Gb/100Gb/s communications. These FPGA vendors are paving the way for customers to build an impressive array of new, life-changing technologies.

To give you some context of the enormity of this demand, the Cisco Visual Networking Index estimates that by 2014, annual global IP traffic will exceed three-quarters of a zettabyte (1,000,000,000,000,000,000 bytes). It would take a person 72 million years to watch all the video content expected to cross global IP networks in 2014 (see Figure 1).

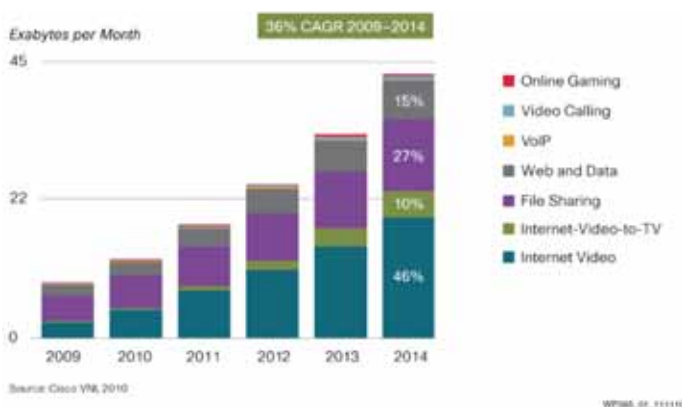


Figure 1: Projected IP Bandwidth Demand

There are several drivers of this demand. Certainly the rising middle class of China's and India's 3 billion people is a significant factor. In 2009, Internet usage in China increased by over 110 million users in a 12-month period, and subscribers for recently deployed 3G mobile services in China reached over 16 million. This number is expected to grow by a staggering 10X to over 170 million users by the end of 2010 –on top of the current base of 1 billion mobile and fixed-line telephone subscribers.

Next to China, India has the largest telecom subscriber base in the world, with over 671 million connections, and the second largest mobile network of over 635 million subscribers. The middle class in China and India are expected to almost triple in size to more than 1.2 billion by 2030, (Source: World Bank)

so it's safe to assume that Asia will play an even greater role in driving future Internet traffic and bandwidth demand.

The rising middle class in Asia isn't the only driver. The pace of adoption of intelligent wireless devices and infrastructure with greater bandwidth is allowing many emerging economies to simply install wireless infrastructure and bypass wired infrastructure altogether. What's more, a rising number of products—from automobiles to medical equipment to factory equipment to home appliances—are connected to the Internet, wired or wirelessly.

The sheer volume of these products that connect to the Internet is bringing the global communications infrastructure to its knees and altering the fabric of the semiconductor industry that serves the communications sector. In the face of stark new economic and market realities, traditional semiconductor business models are proving unsustainable.

At 32/28nm, IC development costs are on the order of \$30M to \$97million (Source: Design Implementation Market Outlook, IBS 2009). This is making application-specific integrated circuits (ASICs) and application-specific standard products (ASSPs) too complex, expensive, and thus too risky to design and manufacture in shrinking market windows.

Instead, designers are increasingly turning to FPGAs because they are already manufactured thus have no manufacturing costs or risks and allow companies to reprogram the hardware as well as the software running on the devices, even after customers have deployed their systems in the field. The companies that lead the worldwide communications infrastructure market have for years benefited from FPGA versatility and flexibility. Now FPGAs are moving ahead of the game.

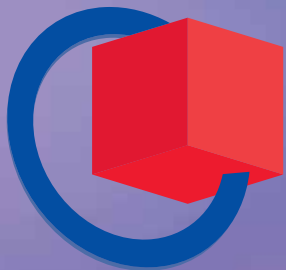
With the introduction of FPGAs that facilitate data transfer at 400Gb/s, design groups now have devices that will quickly allow them to more quickly develop 4G infrastructure at 40Gb/s wireless and 100Gb/s wired data rates and offer a path to 5G 400Gb/s well before the industry has even defined standards for 5G. For more information, visit http://www.xilinx.com/support/documentation/white_papers/wp385_V7_28G_for_400G_Comm_Line_Cards.pdf.

Gilles Garcia is Director of Wired Communications and is responsible for product marketing in the Xilinx Communications Business Unit. Gilles has more than 20 years experience in the networking/telecom field, including experience in customer wins, P&L, strategic direction and investment, and corporate marketing and communications.



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