Introduction to VHDL

Prepared By :

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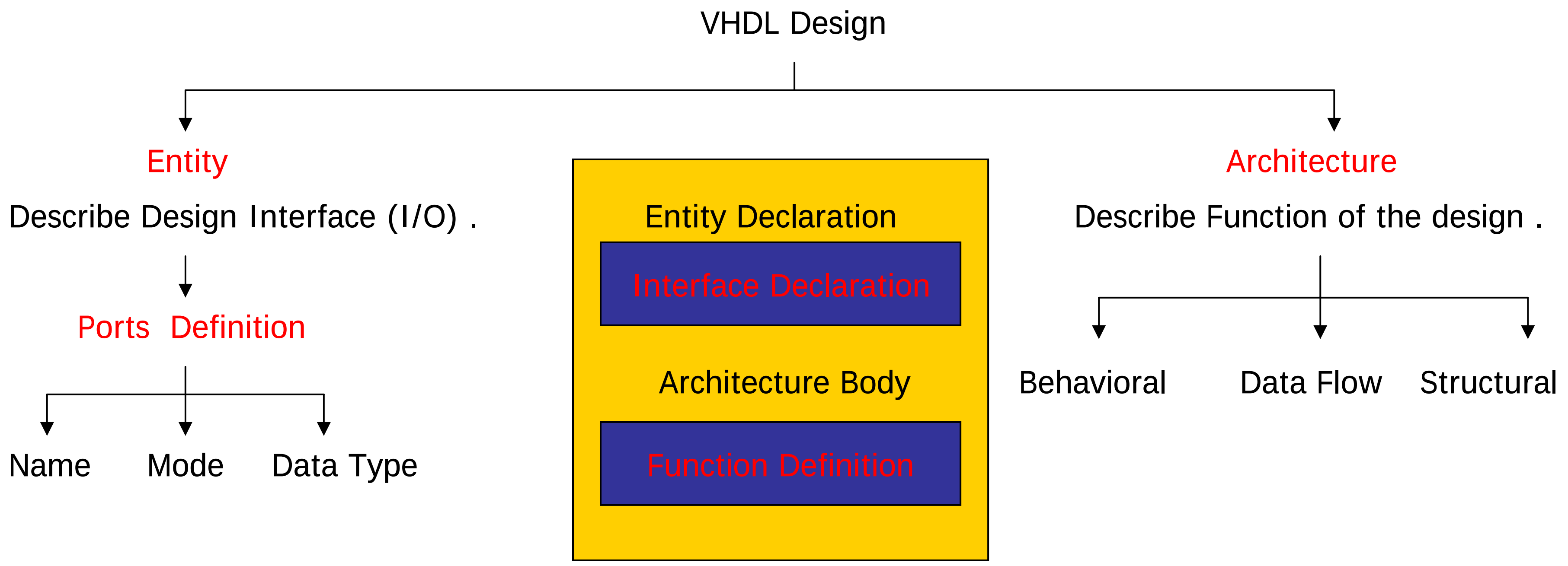
Part (1) : VHDL Code

1.Introduction

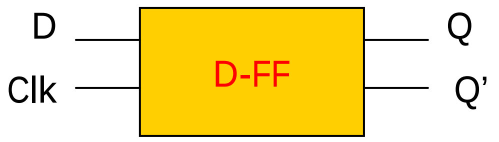
VHDL ➔ Very high speed integrated circuit Hardware Description Language .

Used in testing using simulation for digital systems .



2.Entity Declaration

Ex : D-FF :



```
entity DFF is
 Port ( D , Clk : in std_logic ;
          Q  , Q’  : out std_logic ) ;
end DFF ;
```

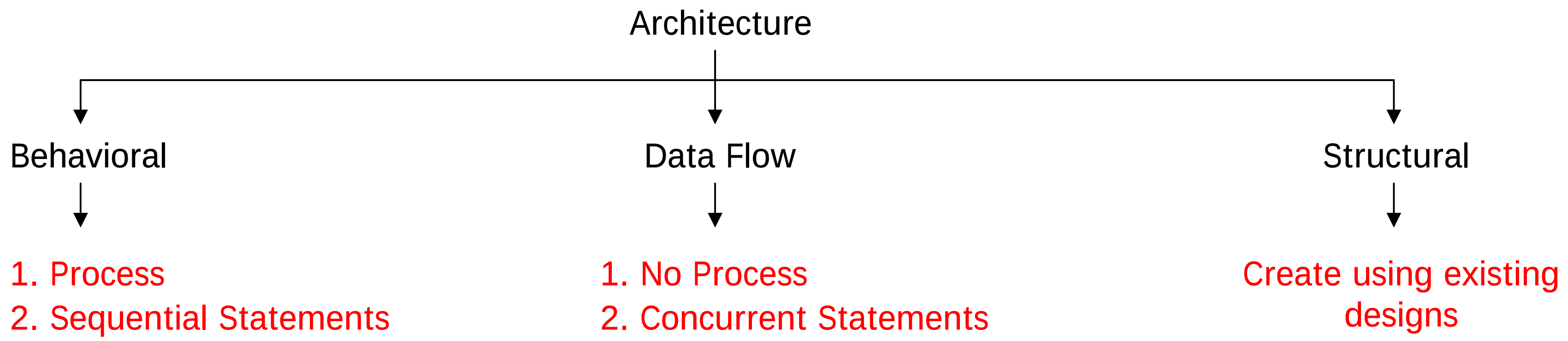
Red bold words ➔ Reserved words .

Port Definition

- **Name**
  - User specified .
  - Don’t use reserved words .
- **Mode**
  - In
  - Out
  - Buffer — Out with internal FB
  - In-Out — Bidirectional
- **Data Type**
  - Boolean
  - Bit , Bit_vector
  - Std_logic

Library : ieee . Std_logic_1164.all

3.Architecture Bodies



Sequential Statements : Used inside a process , ordering of statements is important , because each statement is executed in order in which it appears .

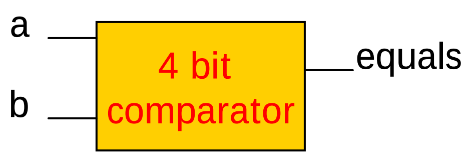
Concurrent Statements : Executed simultaneously .

Statements inside a process are sequential , processes are concurrent

Process Sensitivity List : Identifies which signals will cause the process to execute " a change in sensitivity list would trigger the process ".

3.1.Behavioral

Ex : 4 bit comparator :



Note :

1. Process sensitivity list ➔ a , b .

2. If statements are sequential .

```
entity eqcomp4 is
 Port ( a , b : in bit_vector (3downto 0) ;
         equals  : out bit ) ;
end eqcomp4 ;
architecture behavioral of eqcomp4 is
 begin
 Comp : Process (a , b)
 begin
 if a = b then    equals <= '1' ;
 else equals <= '0' ;
 end if
 end process comp ;
end behavioral ;
```

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3.2.Data Flow

For the 4 bit comparator entity in previous ex :

```
architecture dataflow of eqcomp4 is
 begin
 equals <= ‘1’ when ( a = b ) else ‘0’ ;
end dataflow ;
```

Note :

1. No process is defined .
2. Concurrent statements are used “ no sequential statements “ .

3.3.Structural

Using existed designs ➔ wire between components using reserved word **Portmap**

Ex :

```
U0 : xnor2 portmap ( a , b , X ) ;
```

We will make a structural design using existing components and generate its structural description code “ using simulator “ .

4.Concurrent Statements

Concurrent Statements

Boolean

Selective Signal Assignment

Conditional Signal Assignment

<u>1. Boolean Equations :</u>   Mux example :

```
architecture archmux of mux is
begin
X <= ( a and not (S(1)) and not (S(0))))
    or ( b and not (S(1)) and S(0) )
    or  ( c and (S(1)) and not (S(0))
    or  ( d and (S(1)) and S(0) ) ;
end archmux ;
```

<u>2. Selective Signal Assignment :</u>

```
architecture archmux of mux is
begin
with S select
X <= a when ’ 00 ‘ ;
        b when  ’01’ ;
        c when  ’10’ ;
        d when others ;
end archmux ;
```

4.Concurrent Statements

3. Conditional Signal Assignment :

```
architecture archmux of mux is

begin

when S = ’00’ then X <= a
else when S = ’01’ then X <= b
else when S = ’10’ then X <= c
else X <= d


end archmux ;
```

Note :

In all concurrent statements no processes where defined .

5.Sequential Statements

$$\begin{tikzcd}[column sep=small]
 & & \text{Sequential Statements} \arrow[dll] \arrow[dl] \arrow[dr] \arrow[drr] & & \\
\text{IF} & \text{Case} & & \text{For Loop} & \text{Wait}
\end{tikzcd}$$

IF

if S = ’00’ **then** X <= a ;
else if S = ’01’ **then** X <= b;
else if S = ’10’ **then** X <= c ;
else X <= d ;
end if ;

Case

case S **is**
when ’00’ => X <=a ;
when ’01’ => X <=b ;
when ’10’ => X <=c ;
when others => X <=d ;
end case ;

For Loop

For variable **in** init. **to** final **loop**
Sequential statement
end loop ;

Wait

Wait for specific time ;
Wait on signal ;
Wait until condition ;
Wait ;

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Part (2) : Simulation

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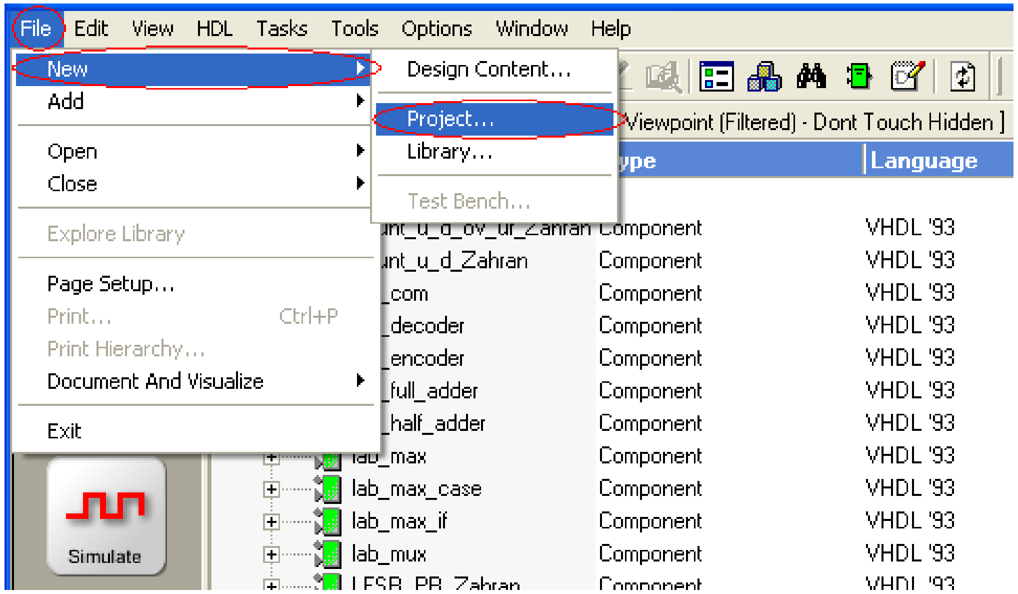
1.Create New Project

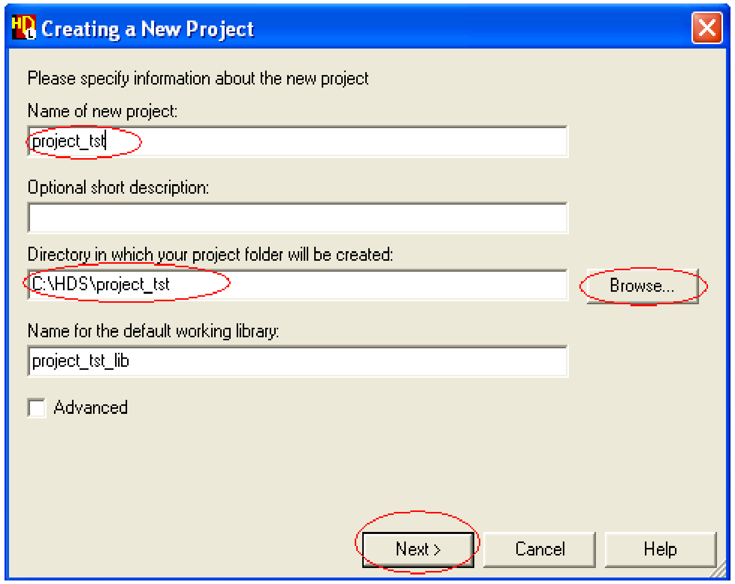
Open HDL designer

File > New > Project

Specify Project name & Location



int_u_d_ov_ur_Zahran	Component	VHDL '93
int_u_d_Zahran	Component	VHDL '93
_com	Component	VHDL '93
_decoder	Component	VHDL '93
_encoder	Component	VHDL '93
_full_adder	Component	VHDL '93
_half_adder	Component	VHDL '93
lab_max	Component	VHDL '93
lab_max_case	Component	VHDL '93
lab_max_if	Component	VHDL '93
lab_mux	Component	VHDL '93
LFSR_PB_Zahran	Component	VHDL '93


Creating a New Project

Please specify information about the new project

Name of new project: project_tst

Optional short description:

Directory in which your project folder will be created: C:\HDS\project_tst

Name for the default working library: project_tst_lib

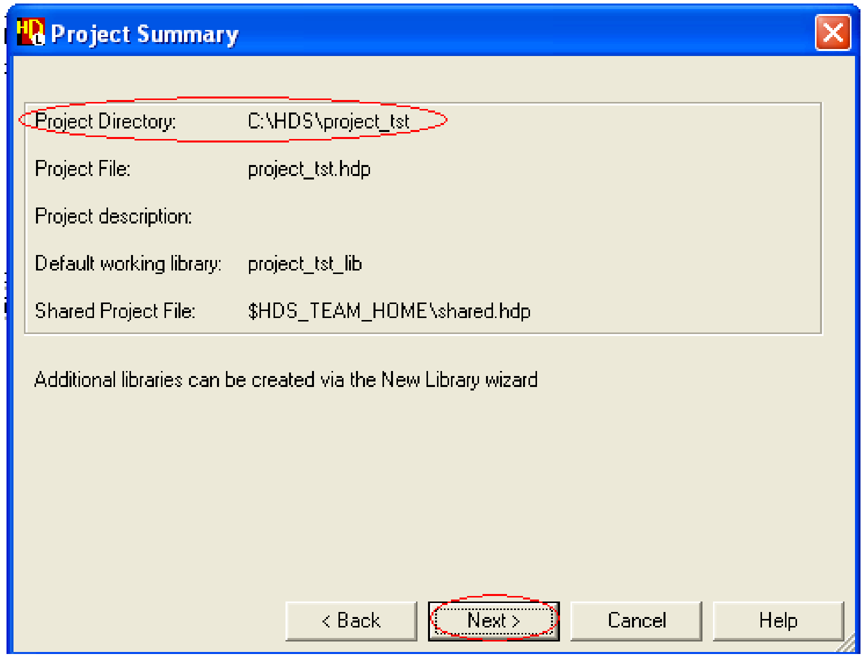
Advanced

Press Next

1.Create New Project Cont.

Project summary ➔ Press Next

Create New Design Files



Project Summary

Project Directory: C:\HDS\project_tst

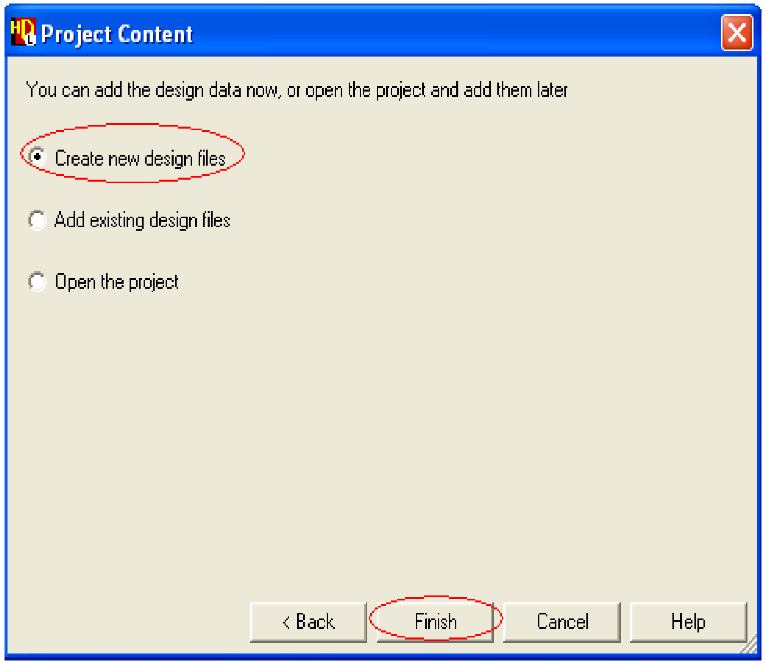
Project File: project_tst.hdp

Project description:

Default working library: project_tst_lib

Shared Project File: $HDS_TEAM_HOME\shared.hdp

Additional libraries can be created via the New Library wizard



Project Content

You can add the design data now, or open the project and add them later

[✓ Create new design files]

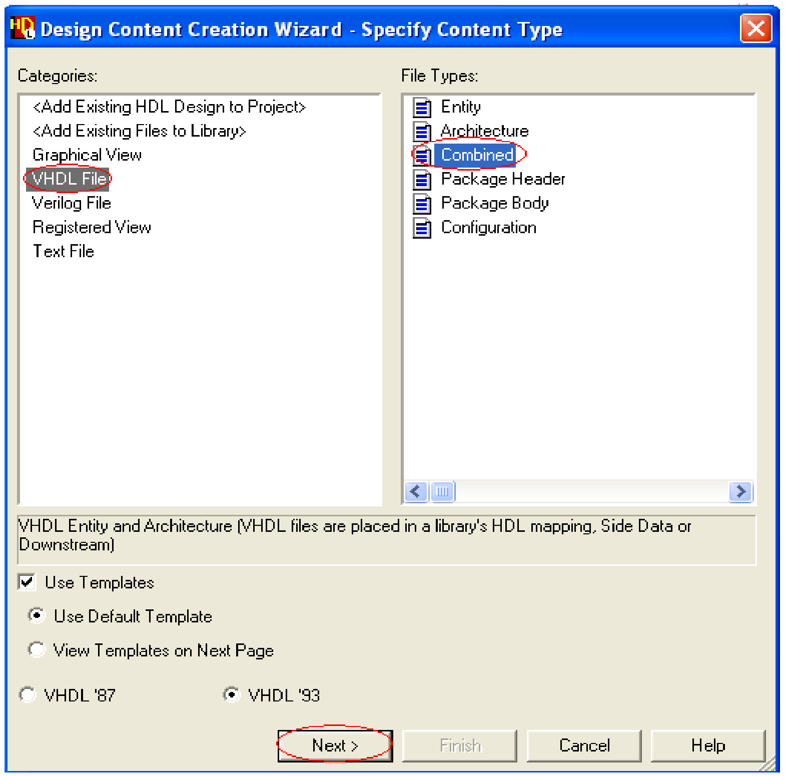
Add existing design files

Open the project

Press Finish

1.Create New Project Cont.

Choose : VHDL File ➔ Combined



Design Content Creation Wizard - Specify Content Type

Categories:
- <Add Existing HDL Design to Project>
- <Add Existing Files to Library>
- Graphical View
- VHDL File
- Verilog File
- Registered View
- Text File

File Types:
- Entity
- Architecture
- Combined
- Package Header
- Package Body
- Configuration

VHDL Entity and Architecture (VHDL files are placed in a library's HDL mapping, Side Data or Downstream)

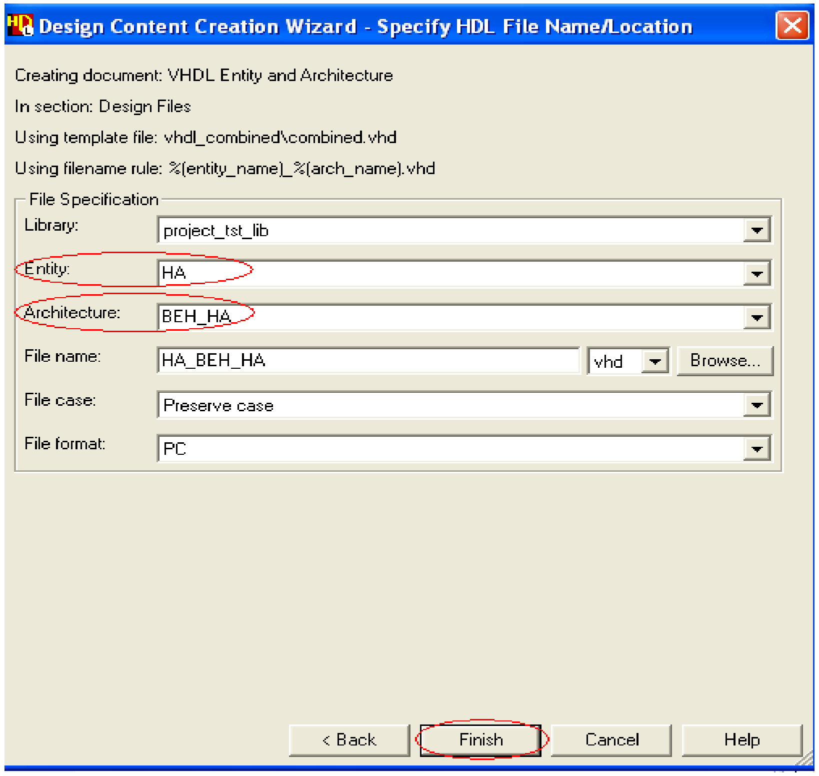
☑ Use Templates

● Use Default Template

○ View Templates on Next Page

○ VHDL '87 ● VHDL '93

Specify : Entity , Architecture name



Design Content Creation Wizard - Specify HDL File Name/Location

Creating document: VHDL Entity and Architecture

In section: Design Files

Using template file: vhdl_combined\combined.vhd

Using filename rule: %(entity_name)_%(arch_name).vhd

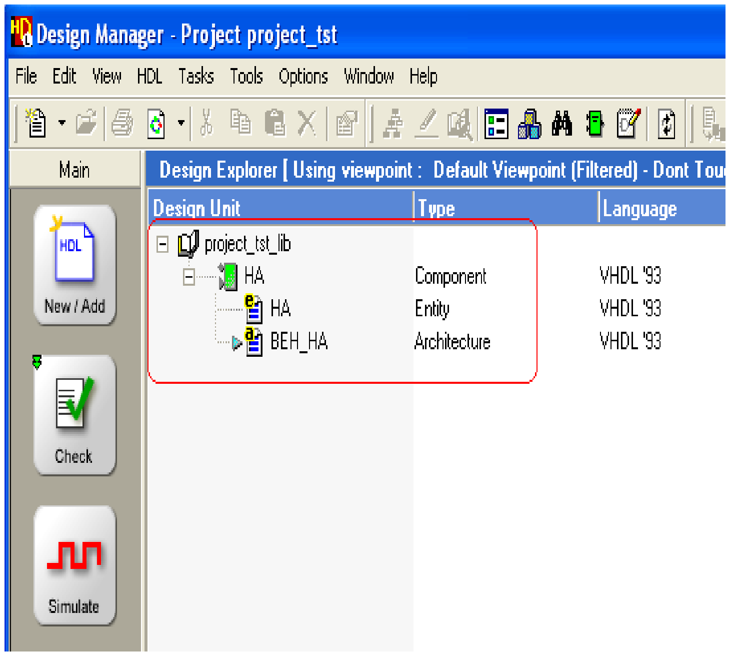
File Specification

Library:	project_tst_lib
Entity:	HA
Architecture:	BEH_HA
File name:	HA_BEH_HA vhd
File case:	Preserve case
File format:	PC

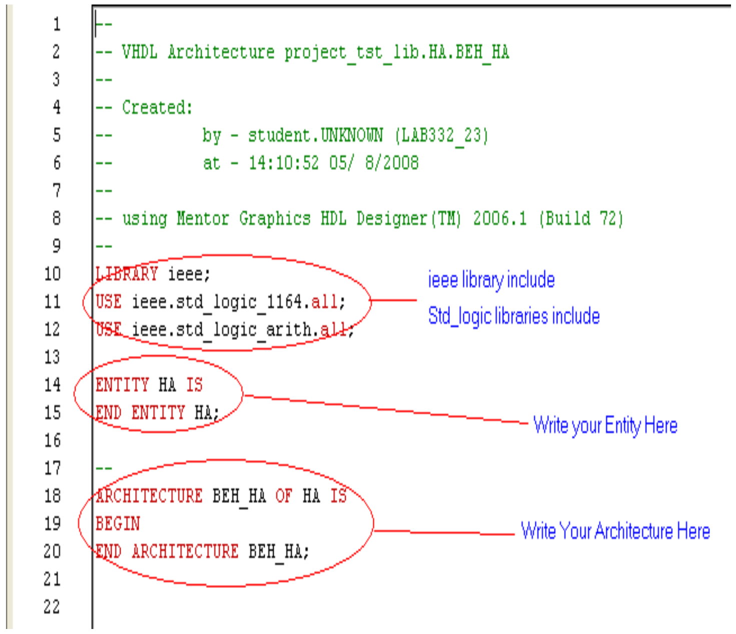
Press Finish

1.Create New Project Cont.

In the design manager , you ‘ll find your entity & architecture


Design Manager - Project project_tst
File Edit View HDL Tasks Tools Options Window Help
Main
Design Explorer [Using viewpoint : Default Viewpoint (Filtered) - Dont Tou
New / Add
Check
Simulate

Design Unit	Type	Language
project_tst_lib		
HA	Component	VHDL '93
HA	Entity	VHDL '93
BEH_HA	Architecture	VHDL '93

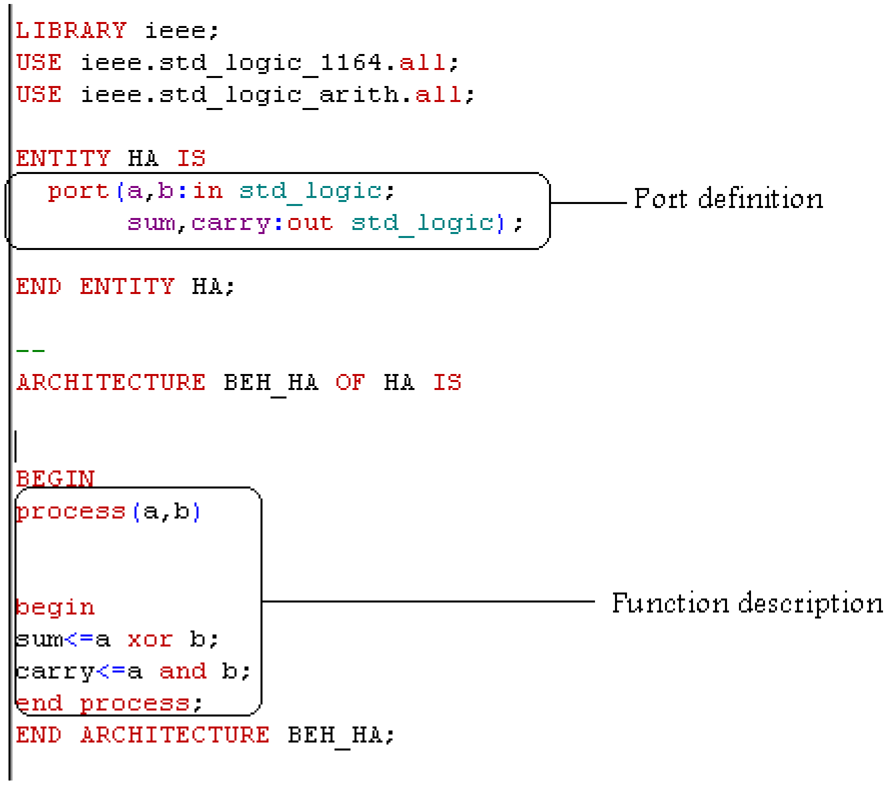


```
--
-- VHDL Architecture project_tst_lib.HA.BEH_HA
--
-- Created:
--          by - student.UNKNOWN (LAB332_23)
--          at - 14:10:52 05/ 8/2008
--
-- using Mentor Graphics HDL Designer(TM) 2006.1 (Build 72)
--
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

ENTITY HA IS
END ENTITY HA;

--
ARCHITECTURE BEH_HA OF HA IS
BEGIN
END ARCHITECTURE BEH_HA;

```

Fill in your entity & architecture

2.Write VHDL Code

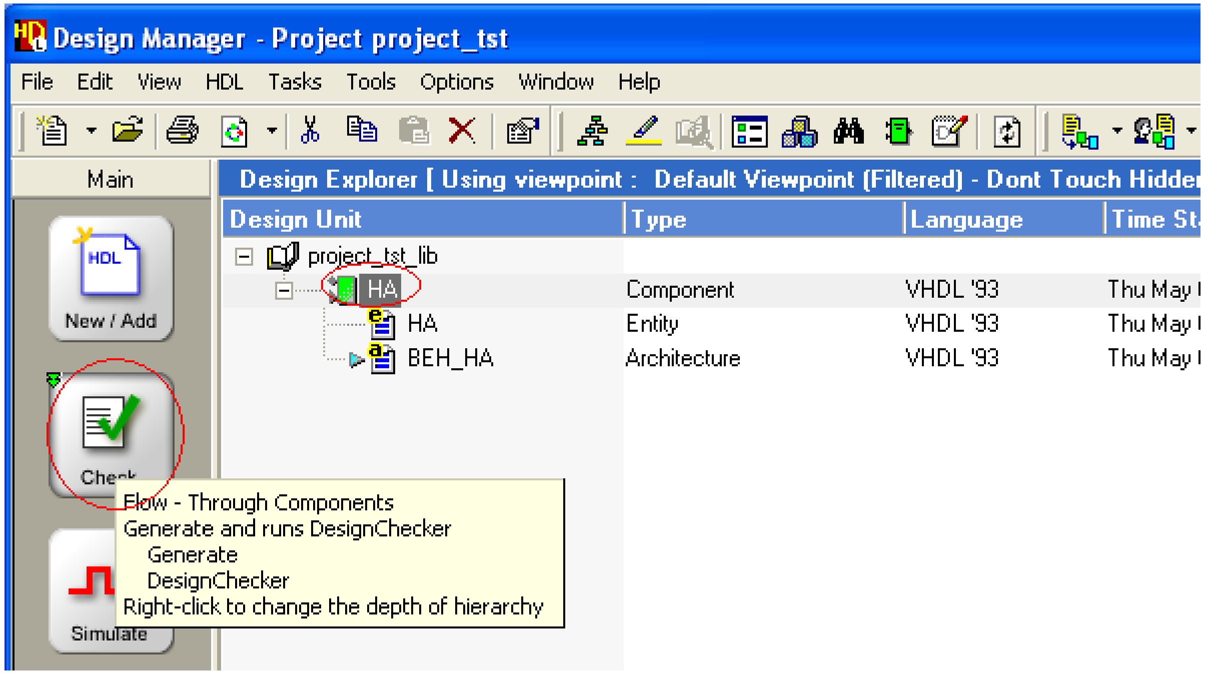
Fill in your Half Adder VHDL code



```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_arith.all;

ENTITY HA IS
   port(a,b:in std_logic;
        sum,carry:out std_logic);

END ENTITY HA;

--
ARCHITECTURE BEH_HA OF HA IS


BEGIN
process(a,b)


begin
sum<=a xor b;
carry<=a and b;
end process;
END ARCHITECTURE BEH_HA;
```

3. Check Errors

Check your code for errors


Design Manager - Project project_tst
File Edit View HDL Tasks Tools Options Window Help
Main
New / Add
Check
Simulate

Design Explorer [Using viewpoint : Default Viewpoint (Filtered) - Dont Touch Hidde

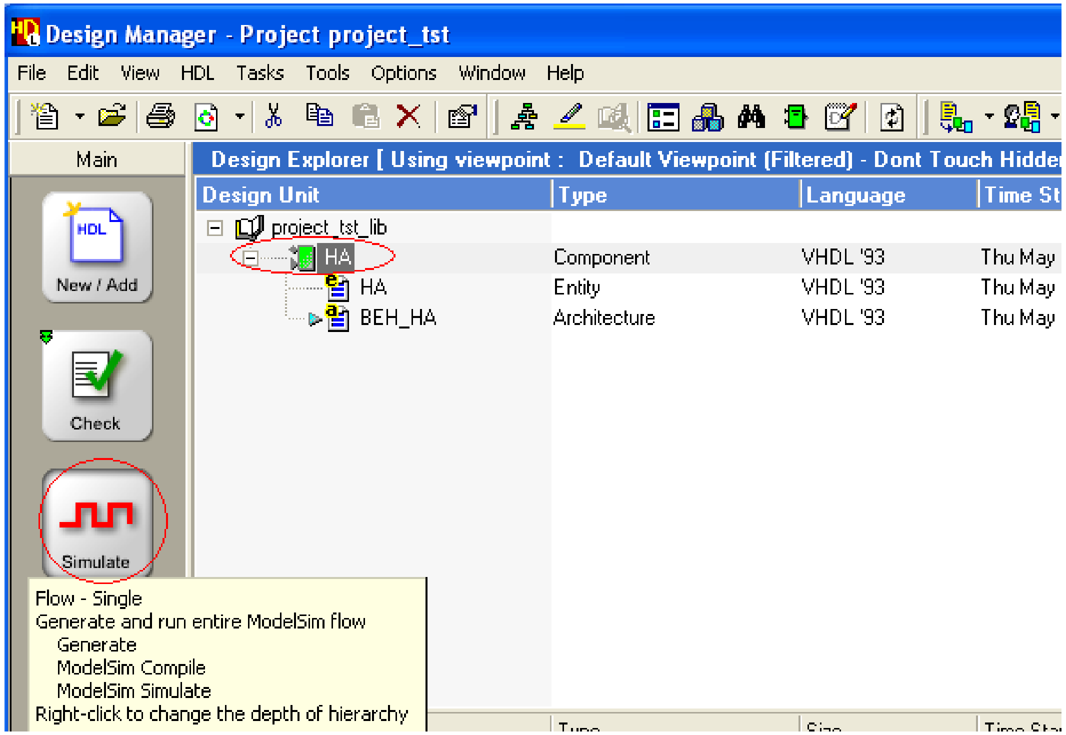
Design Unit	Type	Language	Time St
project_tst_lib			
HA	Component	VHDL '93	Thu May
HA	Entity	VHDL '93	Thu May
BEH_HA	Architecture	VHDL '93	Thu May

Flow - Through Components
Generate and runs DesignChecker
Generate
DesignChecker
Right-click to change the depth of hierarchy

Activate your component > Select Check

4. Start ModelSim

Compile your code & Simulate


Design Manager - Project project_tst
File Edit View HDL Tasks Tools Options Window Help
Main
New / Add
Check
Simulate
Design Explorer [Using viewpoint : Default Viewpoint (Filtered) - Dont Touch Hidde

Design Unit	Type	Language	Time St
project_tst_lib			
HA	Component	VHDL '93	Thu May
HA	Entity	VHDL '93	Thu May
BEH_HA	Architecture	VHDL '93	Thu May

Flow - Single
Generate and run entire ModelSim flow
    Generate
    ModelSim Compile
    ModelSim Simulate
Right-click to change the depth of hierarchy

Activate your component

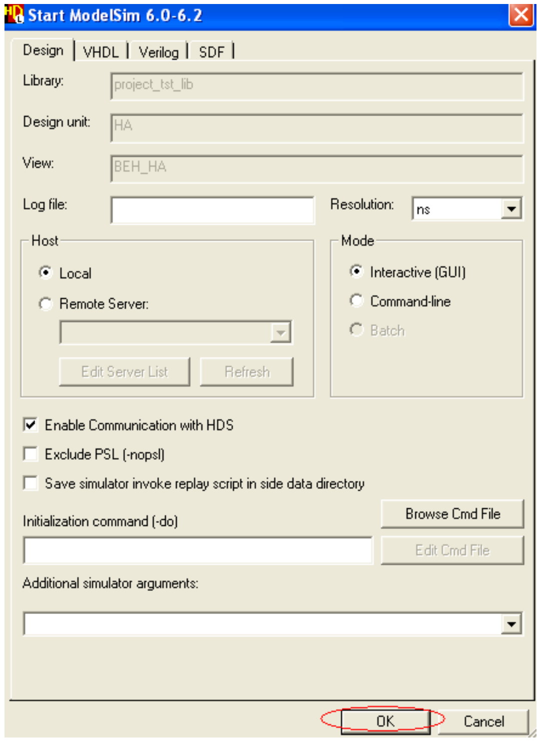
Select Simulate

This opens ModelSim

4. Start ModelSim

ModelSim Starts > Press OK

You 'll find in ModelSim your ports , Force an IP and check OP



Start ModelSim 6.0-6.2

Design | VHDL | Verilog | SDF

Library: project_tst_lib

Design unit: HA

View: BEH_HA

Log file:

Resolution: ns

Host: [✓ Local] Remote Server:

Mode: [✓ Interactive (GUI)] Command-line Batch

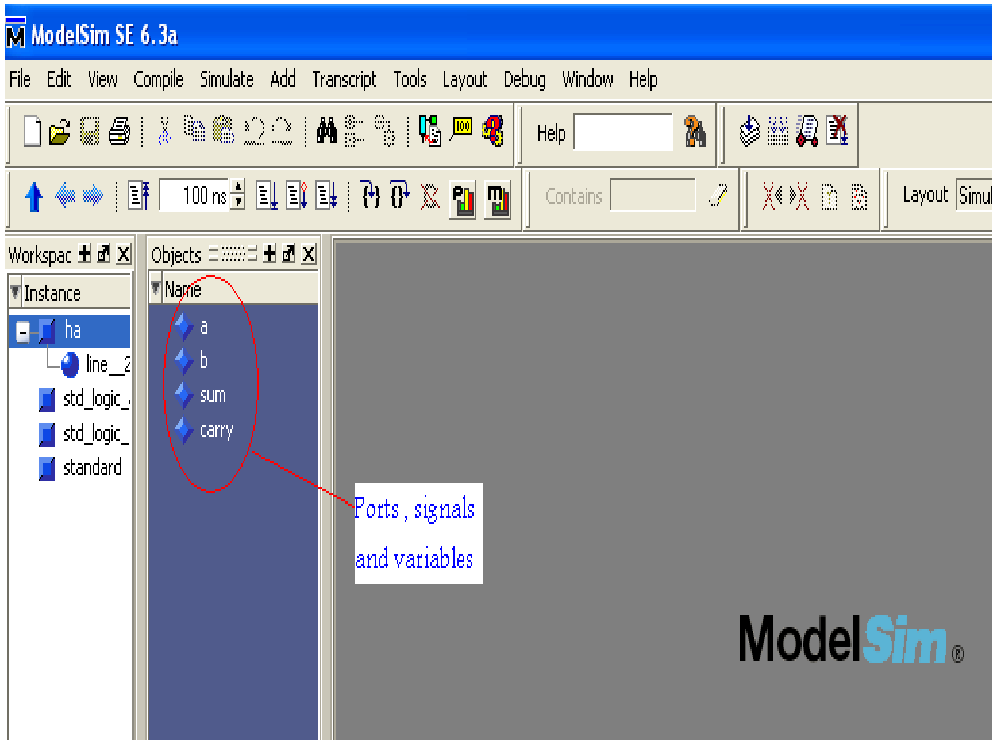
[✓ Enable Communication with HDS]

Exclude PSL (-nopsl)

Save simulator invoke replay script in side data directory

Initialization command (-do)

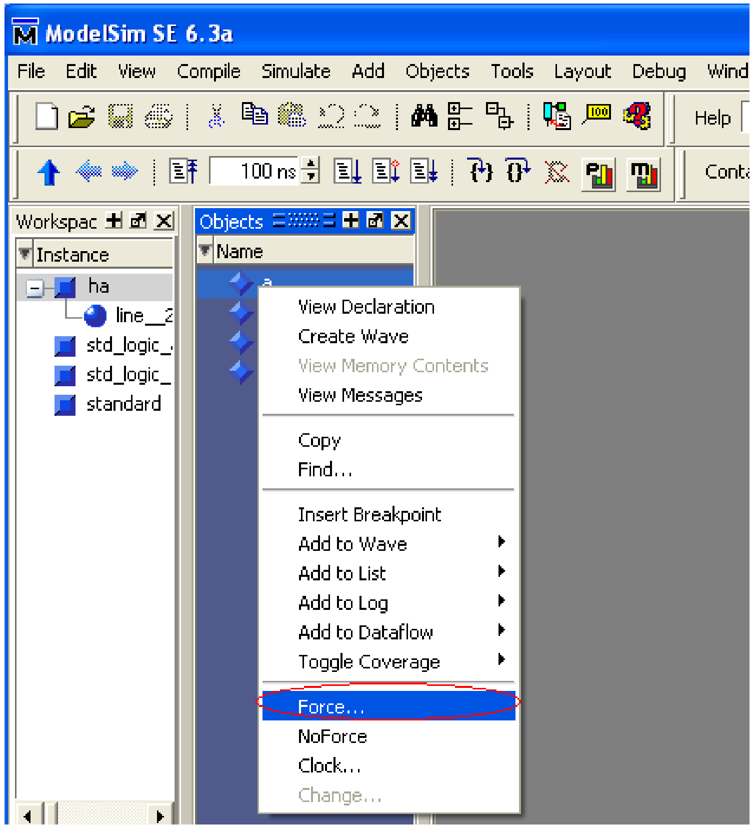
Additional simulator arguments:



ModelSim SE 6.3a

5. Apply IP = Force

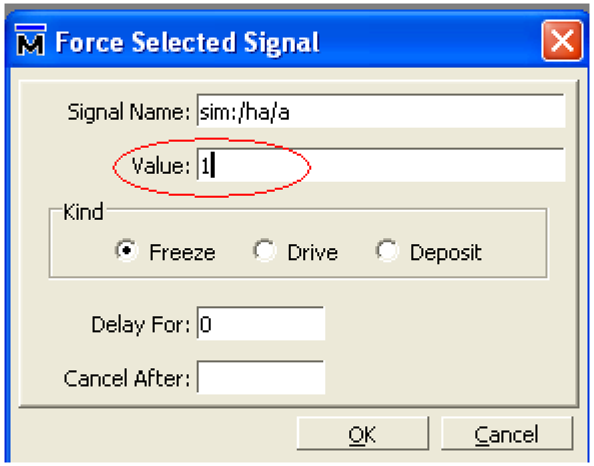
To Force a const. IP :



Right click on Port a

Select Force

Fill in Value = 1


Force Selected Signal

Signal Name: sim:/ha/a

Value: 1

Kind

[✓ Freeze] Drive Deposit

Delay For: 0

Cancel After:

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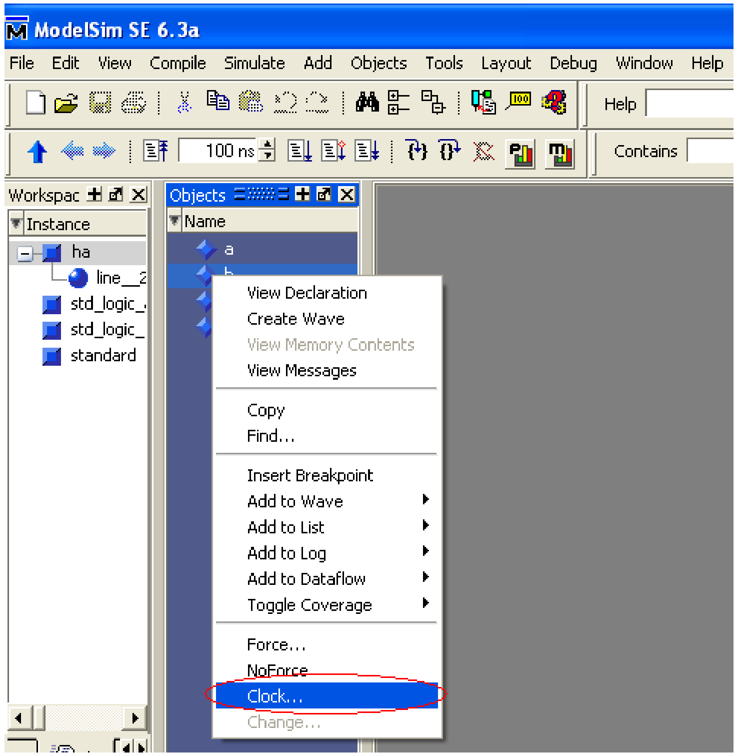
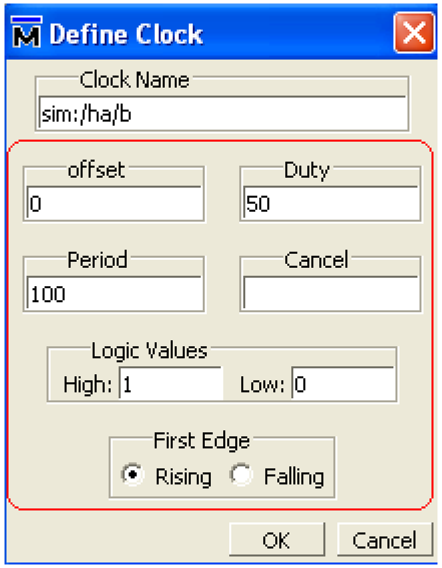
5. Apply IP = Clock

Force an IP clock :



Specify Clock values


Define Clock

Clock Name: sim:/ha/b

offset: 0

Duty: 50

Period: 100

Cancel:

Logic Values

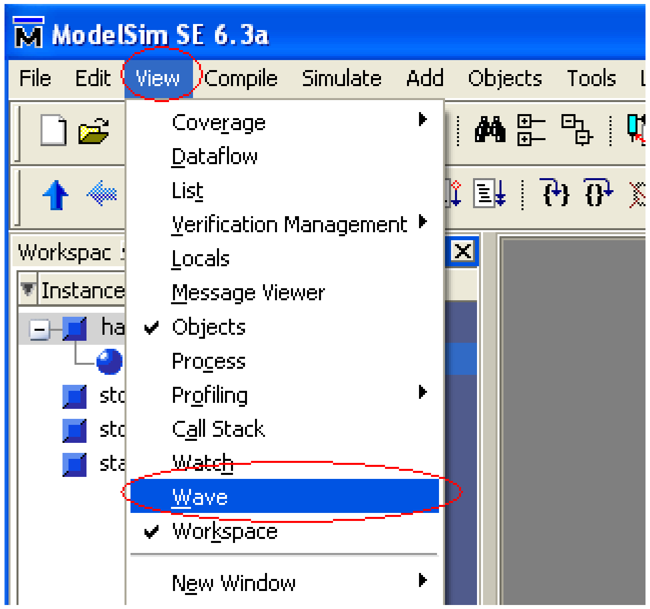
High: 1

Low: 0

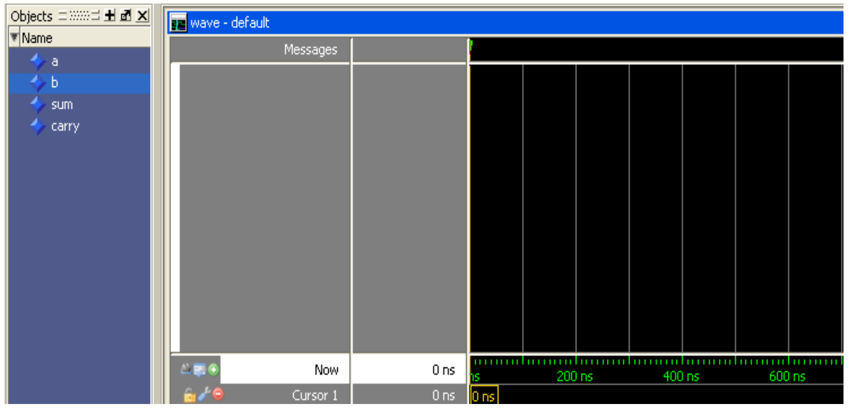
First Edge: [✓ Rising] Falling

6.Wave Display

Select View > Wave



Wave Display Region Appears



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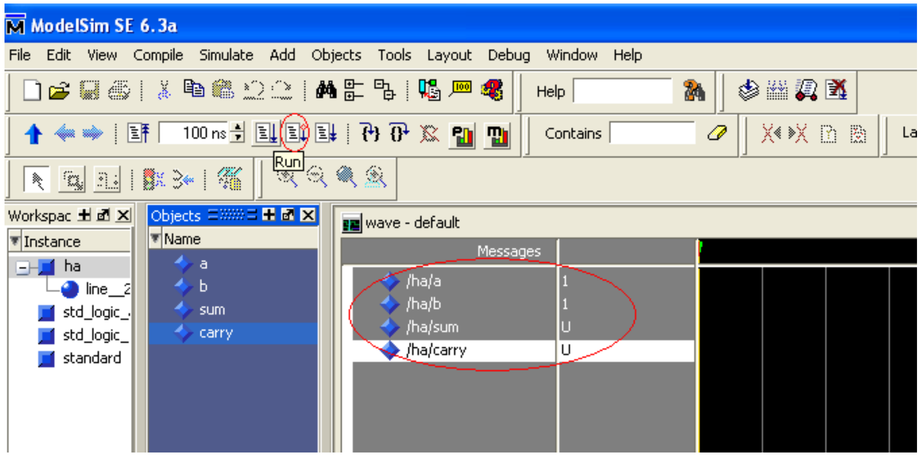
6.Wave Display Cont.

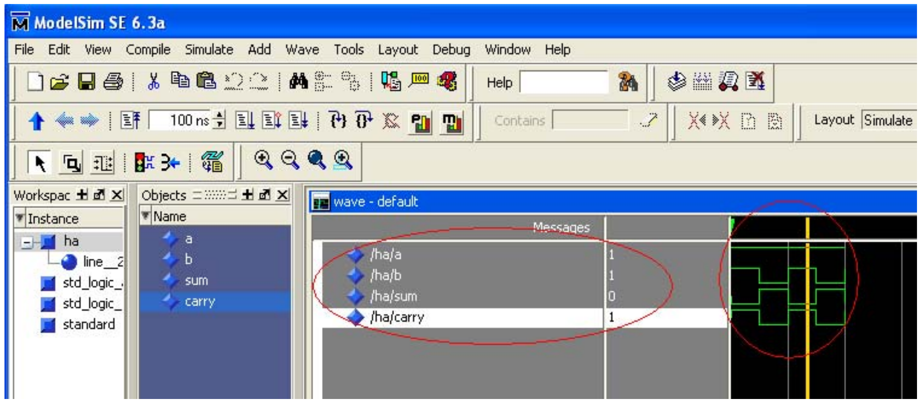
Drag Signals from object view list to wave view list

Press Run



Signal	Value
/ha/a	1
/ha/b	1
/ha/sum	U
/ha/carry	U

Use Cursor to display signal values at certain instant



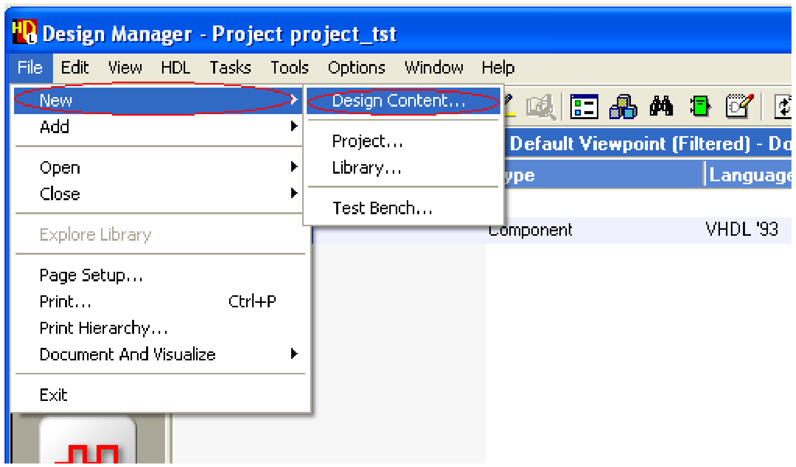
Signal	Value
/ha/a	1
/ha/b	1
/ha/sum	0
/ha/carry	1

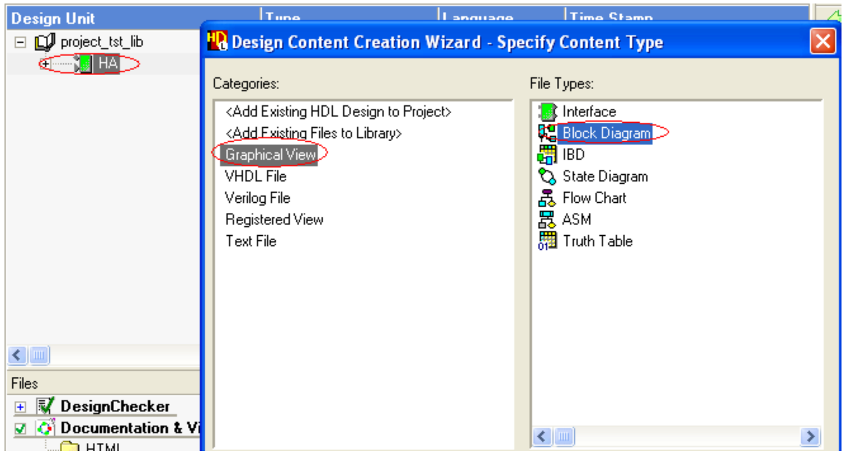
7.Working With Blocks

In the following we shall create a full adder from half adder :

To create new design within same library

We'll create FA from HA using block diagrams



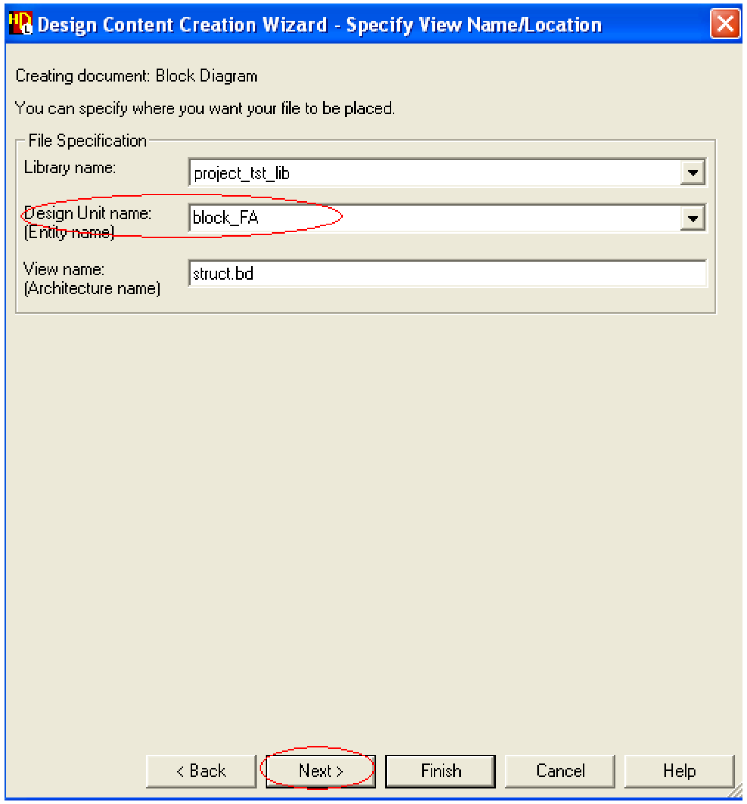


File > New > Design content

Select Graphical view ➔ Block diagram

7.Working With Blocks Cont.

Fill in entity name ONLY



Design Content Creation Wizard - Specify View Name/Location

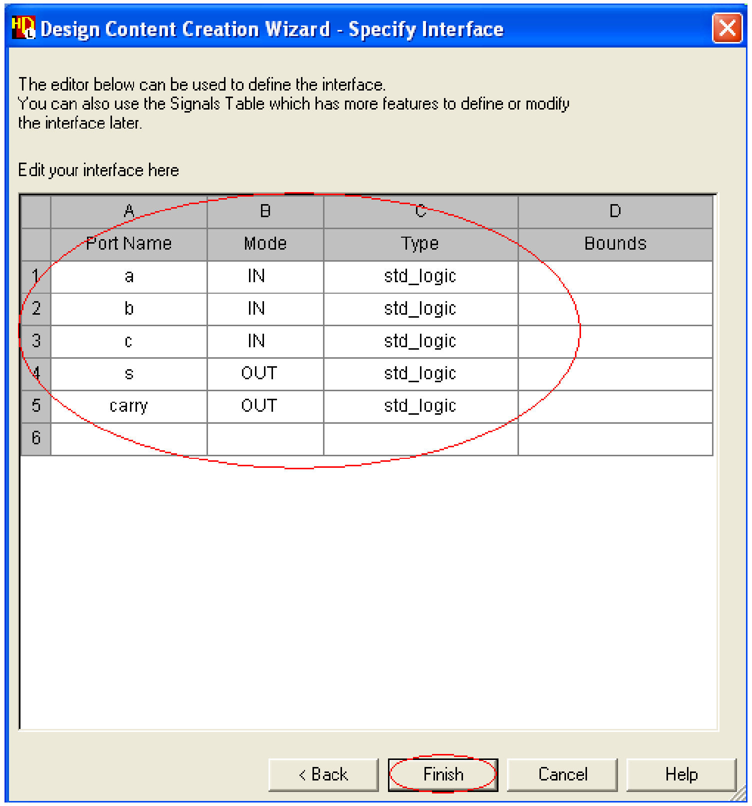
Creating document: Block Diagram

You can specify where you want your file to be placed.

File Specification

Library name:	project_tst_lib
Design Unit name: (Entity name)	block_FA
View name: (Architecture name)	struct.bd

Fill in Port names for FA , specify Mode & type as shown



Design Content Creation Wizard - Specify Interface

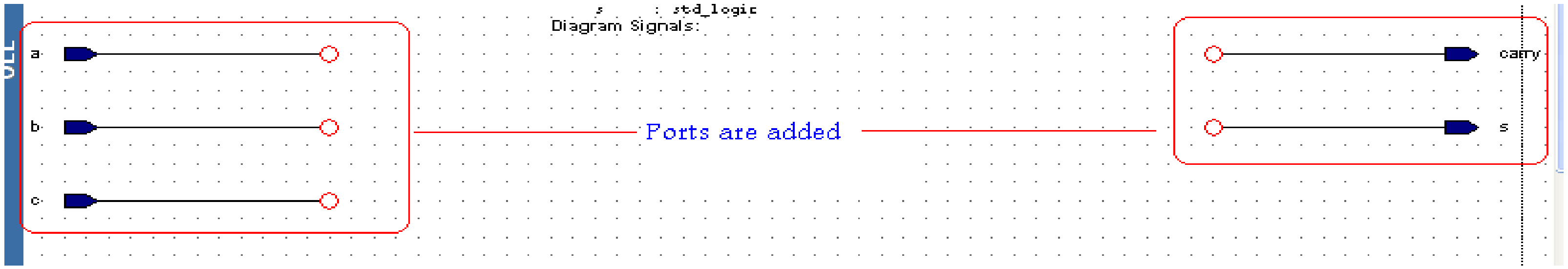
The editor below can be used to define the interface.
You can also use the Signals Table which has more features to define or modify the interface later.

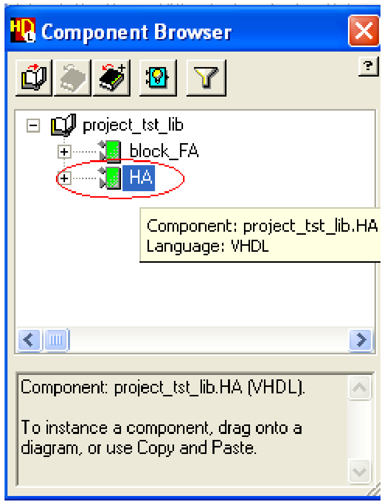
Edit your interface here

	A	B	C	D
	Port Name	Mode	Type	Bounds
1	a	IN	std_logic	
2	b	IN	std_logic	
3	c	IN	std_logic	
4	s	OUT	std_logic	
5	carry	OUT	std_logic	
6				

7.Working With Blocks Cont.

The ports you specified are added :

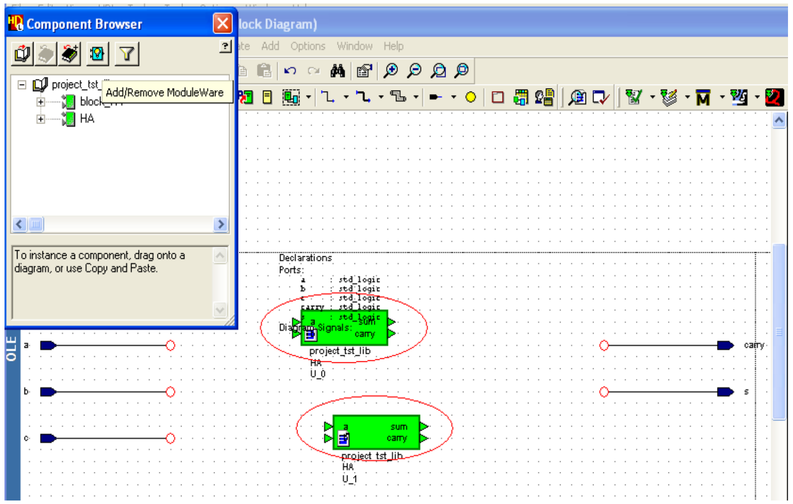




Component: project_tst_lib.HA
Language: VHDL

Component: project_tst_lib.HA (VHDL).

To instance a component, drag onto a diagram, or use Copy and Paste.



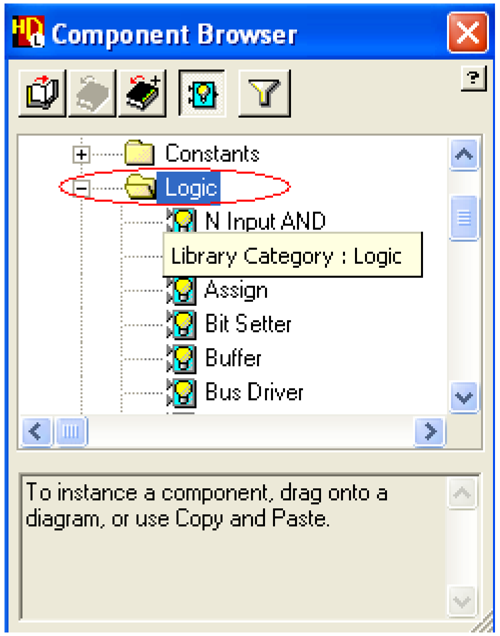
To instance a component, drag onto a diagram, or use Copy and Paste.

Select Add Component from upper toolbar

Drag two blocks of HA to create your FA

7.Working With Blocks Cont.

From component browser choose logic > gated OR



Component Browser

Constants

Logic

N Input AND

Library Category : Logic

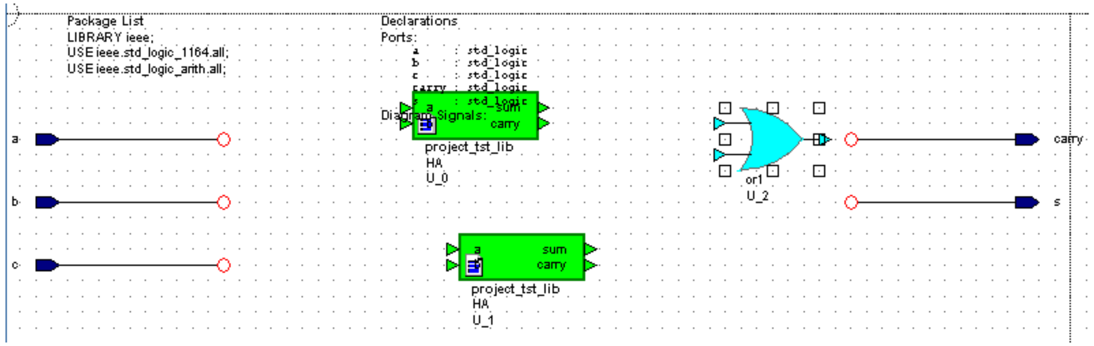
Assign

Bit Setter

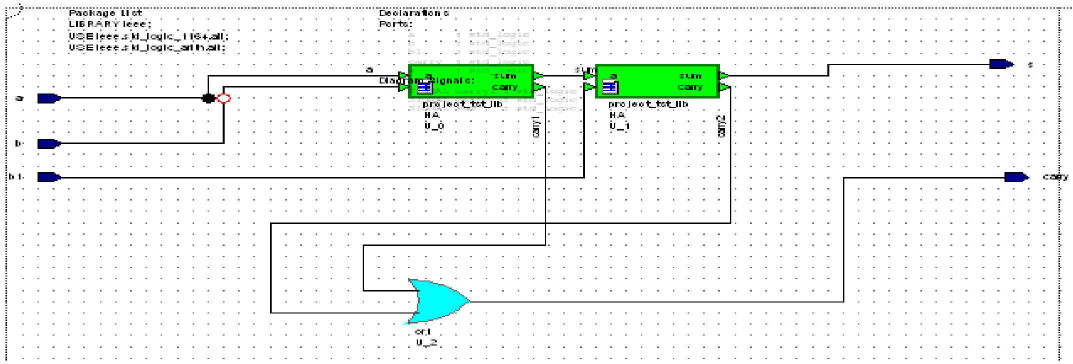
Buffer

Bus Driver

To instance a component, drag onto a diagram, or use Copy and Paste.

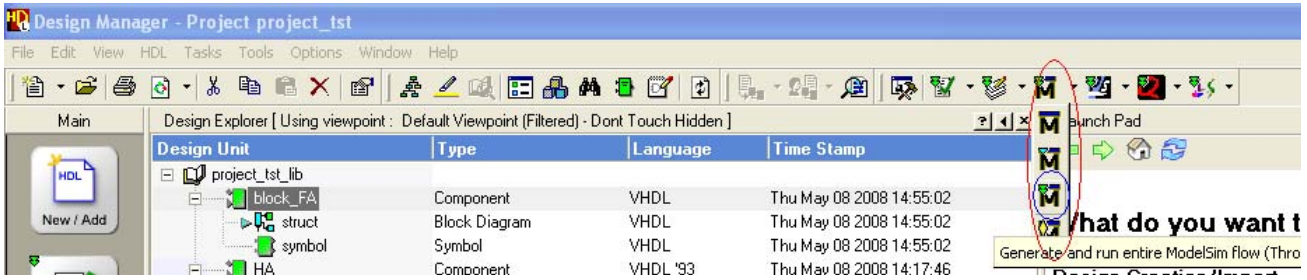


Wire all components together



7.Working With Blocks Cont.

From tool bar > ModelSim Icon > Simulate through components


Design Manager - Project project_tst

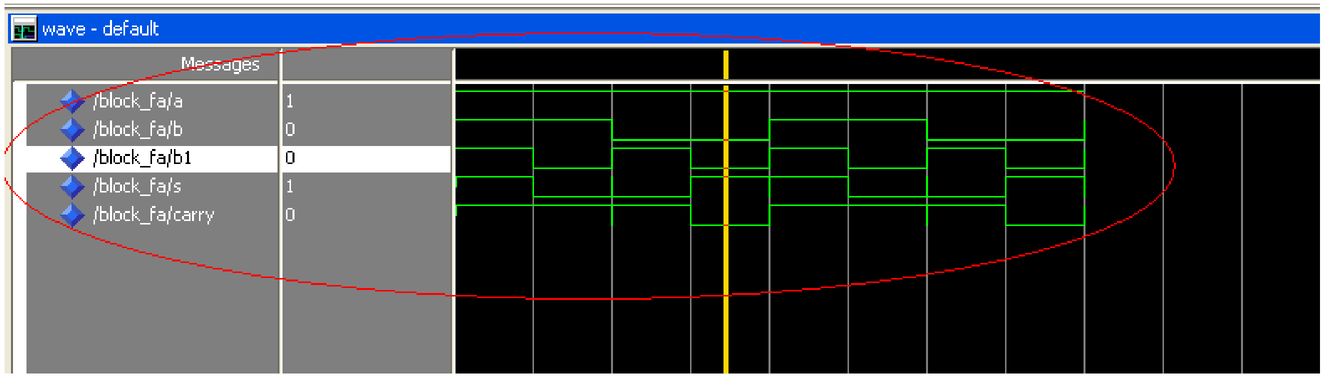
File Edit View HDL Tasks Tools Options Window Help

Design Explorer [Using viewpoint : Default Viewpoint (Filtered) - Dont Touch Hidden]

Design Unit	Type	Language	Time Stamp
project_tst_lib			
block_FA	Component	VHDL	Thu May 08 2008 14:55:02
struct	Block Diagram	VHDL	Thu May 08 2008 14:55:02
symbol	Symbol	VHDL	Thu May 08 2008 14:55:02
HA	Component	VHDL '93	Thu May 08 2008 14:17:46

Generate and run entire ModelSim flow (Thro

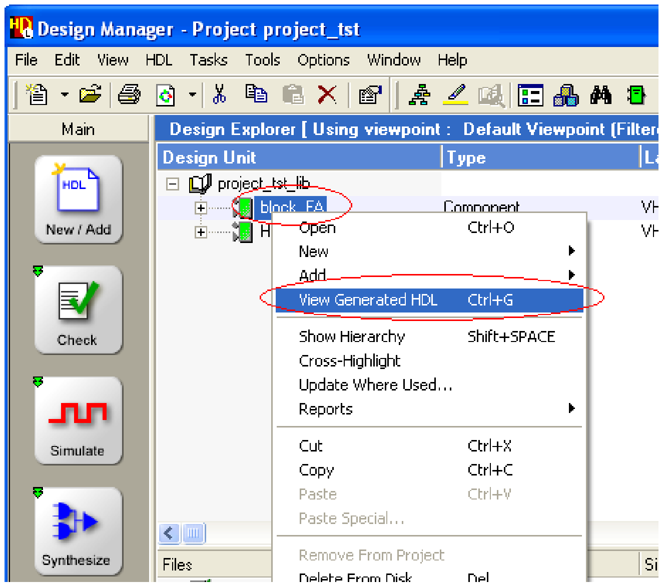
Simulation Results :


wave - default

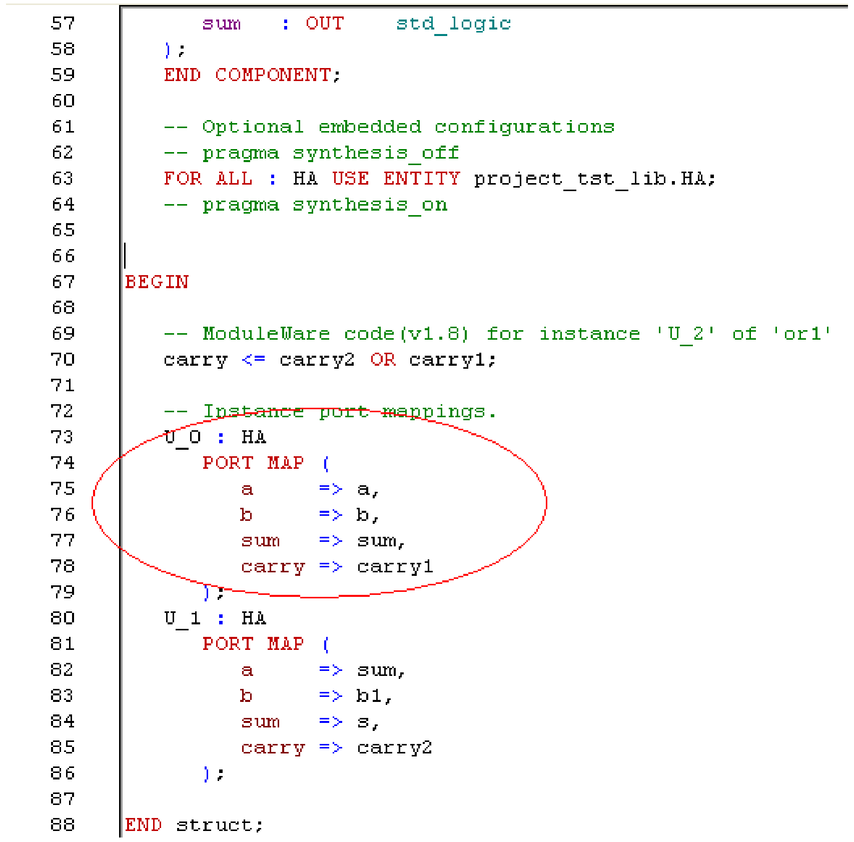
Messages	
/block_fa/a	1
/block_fa/b	0
/block_fa/b1	0
/block_fa/s	1
/block_fa/carry	0

7.Working With Blocks Cont.

To display the FA structural code :



View Generated HDL



```
    sum   : OUT    std_logic
  );
  END COMPONENT;

  -- Optional embedded configurations
  -- pragma synthesis_off
  FOR ALL : HA USE ENTITY project_tst_lib.HA;
  -- pragma synthesis_on


BEGIN

  -- ModuleWare code(v1.8) for instance 'U_2' of 'or1'
  carry <= carry2 OR carry1;

  -- Instance port mappings.
  U_0 : HA
    PORT MAP (
      a     => a,
      b     => b,
      sum   => sum,
      carry => carry1
    );
  U_1 : HA
    PORT MAP (
      a     => sum,
      b     => b1,
      sum   => s,
      carry => carry2
    );

END struct;
```