Evaluating Power
for Altera Devices

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Introduction

A critical element of system reliability is the capacity of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature. This application note discusses how to evaluate and manage power, and provides sample worksheets for performing a power evaluation.

Power Evaluation

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To evaluate the power usage in your system, use the following steps:

1. Estimate the power consumption of the application.
2. Calculate the maximum power for the device and package.
3. Compare the estimated and maximum power values.

Table 1 shows the variables used for estimating power consumption.

Table 1. Variables Used for Evaluating Power Consumption (Part 1 of 2)

Variable	Unit
$I_{CCSTANDBY}$	mA
K	µA/(MHz × LE)
f_{MAX}	MHz
N	LE
I_{CCINT}	mA
P_{INT}	mW
MC_{TON}	LE
MC_{DEV}	LE
MC_{USED}	LE
P_{DCOUT}	mW

Table 1. Variables Used for Evaluating Power Consumption (Part 2 of 2)

Variable	Unit
C_{AVE}	pF
P_{ACOUT}	mW
P_{IO}	mW
P_{EST}	mW
θ_{JA}	° C/W
T_J	° C
T_A	° C
P_{MAX}	W

Estimating Power Consumption

Use the following formula to compute the estimated power consumption (P_{EST}) of the application:

$$P_{EST} = P_{INT} + P_{IO}$$

Where: $P_{INT} = I_{CCINT} \times V_{CCINT}$
$P_{IO} = P_{ACOUT} + P_{DCOUT}$

Therefore:

$$P_{EST} = (I_{CCINT} \times V_{CCINT}) + (P_{ACOUT} + P_{DCOUT})$$

The no-load power (P_{INT}) value can be obtained from the "Power Consumption" section in each device family data sheet. Because this value is "unloaded," it is necessary to add the power dissipated by the I/O buffers—P_{DCOUT} from steady-state outputs and the P_{ACOUT} current from frequently switching outputs. P_{DCOUT} depends on the number of steady-state outputs, the logic levels they drive, and the resistive load on each output, as shown in the following formula:

$$P_{DCOUT} = \sum_{n=1}^{d} P_{DCn}$$

Where: d = Number of DC outputs
P_{DCn} = DC output power of output n
V_n = Voltage swing of output n
f_n = Switching frequency of output n

Table 2 shows the DC power dissipated by the output drivers of a device with V_{CCIO} set at 5 V under typical types of loads. The DC power dissipated by the output driver does not equal the $V_{CC} \times I_{CCIO}$ value because most of the DC power is consumed by the load. If you are using a 2.5-V or 3.3-V device or a non-5.0-V V_{CCIO}, you can compute the power based on the device's I_{OH} and I_{OL} figures shown in the device family data sheet.

Table 2. DC Power Dissipated

Load Driven	P_{DCn} (mW)
1-K pull-up resistor for low outputs	0.49
1-K pull-down resistor for high outputs	5.04
Bipolar for low outputs	0.16
Bipolar for high outputs	0.0576
CMOS inputs	Negligible

P_{ACOUT} depends on the capacitive load on each output and the frequency at which each output switches, as shown in the following formula:

$$P_{ACOUT} = \sum_{n=1}^{a} C_n V_n f_n \times V_{CCIO}$$

Where: a = Number of AC outputs
C_n = Capacitive load on output n
V_n = Voltage swing of output n
f_n = Switching frequency of output n

The following equation shows the frequency of each output (f_n), in terms of the maximum clock frequency ($\mathbf{f_{MAX}}$) of the design and the average ratio of I/O pins toggling at each clock ($\mathbf{tog_{IO}}$):

$$f_n = (0.5) \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}}$$

Inserting the equation for f_n into the P_{ACOUT} equation and resolving the summation for an average capacitive load yields the following formula:

$$P_{ACOUT} = (0.5) \times OUT \times C_{AVE} \times V_O \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}} \times V_{CCIO}$$

Where: OUT = Total number of output and bidirectional pins

Table 3 shows the V_{CCIO} and V_O values for Altera® devices.

Table 3. V_{CCIO} & V_O Values

V_{CCIO} (V)	V_O (V)
5.0	3.8
3.3	3.3
2.5	2.5

For example, the following equation provides the power consumed by driving a capacitive load for applications with V_{CCIO} = 5 V:

$$P_{ACOUT} = (0.5) \times OUT \times C_{AVE} \times 3.8\ V \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}} \times 5.0\ V$$

Calculating Maximum Power for the Device & Package

The following formulas are used to calculate the maximum allowed power (P_{MAX}) for a device:

$$P_{MAX} = \frac{T_J - T_A}{\theta_{JA}} \quad \text{or} \quad P_{MAX} = \frac{T_J - T_C}{\theta_{JC}}$$

The maximum allowed power is dependent on the maximum allowed junction temperature (T_J) of the silicon, the ambient temperature of operation (T_A), and the package's thermal resistance (θ_{JA}) when configured in the system. The maximum junction temperature is specified in the Altera device family data sheets. The ambient temperature depends on the application. The worst-case P_{MAX} value is estimated using the formula with θ_{JA}, the junction-to-ambient thermal resistance. The θ_{JA} value for Altera devices is provided for still air (with convection cooling only), and for a forced-air flow of 100 feet/second, 200 feet/second, and 400 feet/second. If heat-sinking is used to dissipate heat and θ_{JA} for a heat sink is given, you should use the case temperature (T_C) and the junction-to-case thermal resistance (θ_{JC}) to calculate P_{MAX} for a device. θ_{JC} is a measure of the lowest possible thermal resistance.

For thermal resistance values (θ_{JC} and θ_{JA}) of Altera devices, refer to the *Altera Device Packaging Information Data Sheet*.

Comparing Maximum Allowed Power & Estimated Power

To avoid reliability problems, you should compare the values calculated for the maximum allowed power and estimated power. The estimated power should be the smaller of the two values. If the estimated power exceeds the maximum allowed power, refer to "Thermal Management" on page 10 for suggestions on how to reduce power requirements for a design. Figure 1 shows a sample worksheet for evaluating power.

Figure 1. Power Evaluation Worksheet (Part 1 of 2)

Design_____ Device_____

Estimating the Power Consumption of the Application

Internal Power Calculation for All Altera Devices

FLEX 10K, FLEX 8000 & FLEX 6000 Devices

Standby current ($I_{CCSTANDBY}$)	$I_{CCSTANDBY}$ = _____	mA
Coefficient for I_{CC} calculation. See the appropriate device family data sheet for this value.	K = _____	µA/(MHz × LE)
Maximum clock frequency ($\mathbf{f_{MAX}}$)	$\mathbf{f_{MAX}}$ = _____	MHz
Total number of logic elements (LEs) used in the device (N)	N = _____	LE
Average ratio of logic cells toggling ($\mathbf{tog_{LC}}$) at each clock (typically 0.125)	$\mathbf{tog_{LC}}$ = _____	
Total internal current (I_{CCINT})	I_{CCINT} = _____	mA
$I_{CCINT} = I_{CC0} + K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}}$		
Total internal power (P_{INT})	P_{INT} = _____	mW
$P_{INT} = V_{CC} \times I_{CCINT}$		

MAX 9000, MAX 7000 & MAX 3000A Devices

Coefficients for I_{CC} calculation. See the appropriate device family data sheet for these values.	A = _____	mA/LE
	B = _____	mA/LE
	C = _____	mA/(MHz × LE)
Number of macrocells with the Turbo Bit™ on (MC_{TON})	MC_{TON} = _____	LE
Number of macrocells in the device (MC_{DEV})	MC_{DEV} = _____	LE
Number of macrocells in the design (MC_{USED})	MC_{USED} = _____	LE
Maximum clock frequency ($\mathbf{f_{MAX}}$)	$\mathbf{f_{MAX}}$ = _____	MHz
Average ratio of logic cells toggling ($\mathbf{tog_{LC}}$) at each clock (typically 0.125)	$\mathbf{tog_{LC}}$ = _____	
Total internal current (I_{CCINT})	I_{CCINT} = _____	mA
$I_{CCINT} = (A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$		
Total internal power (P_{INT})	P_{INT} = _____	mW
$P_{INT} = V_{CC} \times I_{CCINT}$		

Figure 1. Power Evaluation Worksheet (Part 2 of 2)

External Power Calculation for All Altera Devices

Power consumed by the DC output load (P_{DCOUT})	P_{DCOUT} = _____	mW
$P_{DCOUT} = P_{DCn}$		
Average capacitive load (C_{AVE}) at output pins	C_{AVE} = _____	pF
Number of output/bidirectional pins in the design (OUT)	OUT = _____	
Average ratio of I/O pins toggling (**tog_{IO}**) at each clock (typically 0.125)	**tog_{IO}** = _____	
Power consumed by AC output load (P_{ACOUT})	P_{ACOUT} = _____	mW
$P_{ACOUT} = 1/2 \times OUT \times C_{AVE} \times V_O \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}} \times V_{CCIO} \times 0.001$		
Total external power (P_{IO})	P_{IO} = _____	mW
$P_{IO} = P_{DCOUT} + P_{ACOUT}$		

Total Power Calculation for All Altera Devices

Estimated total power (P_{EST})	P_{EST} = _____	mW
$P_{EST} = P_{INT} + P_{IO}$		

Calculating Maximum Allowed Power for the Device & Package

Thermal resistance of the device	θ_{JA} = _____	°C/W
Maximum junction temperature (T_J) as specified in the appropriate device family data sheet.	T_J = _____	°C
Ambient temperature (T_A) of the design	T_A = _____	°C
Maximum power (P_{MAX}) allowed for the device	P_{MAX} = _____	W
$P_{MAX} = (T_J - T_A) / \theta_{JA}$		

Comparing Maximum Power Allowed & Estimated Power

Is $P_{EST} < P_{MAX}$? Yes or No

Tables 4 and 5 show design parameters for the sample power evaluations shown in Figures 2 and 3. The design parameters are unique to the sample designs and are not found in device family data sheets.

Table 4. Parameters for the Sample FLEX 10K Design

Parameter	Description	Value
OUT	Number of outputs	150
Number of 1-KΩ pull-up resistors	Type of load	50
CMOS inputs	Type of load	100
C_{AVE}	Average capacitance	35 pF
N	Number of logic elements used	2,747 LE
$\mathbf{f_{MAX}}$	Maximum operating frequency	20 MHz
P_{DCOUT}	Static power consumed by outputs	(0.49 mW × 50) + (0 mW × 231) = 24.5 mW

Table 5. Parameters for the Sample MAX 9000 Design

Parameter	Value
MC_{TON}	139
MC_{DEV}	560
MC_{USED}	500
MC_{TOFF}	421
$\mathbf{f_{MAX}}$	40 MHz
OUT	211
Number of 1-KΩ pull-down resistors	10
CMOS inputs	201
C_{AVE}	35 pF
P_{DCOUT}	(5.04 mW × 10) + (0 mW × 201) = 50 mW

Figures 2 and 3 provide power evaluations for sample designs implemented in FLEX® 10K and MAX® 9000 devices, respectively.

Figure 2. Sample Power Evaluation for a FLEX 10K Device (Part 1 of 2)

Design: dsp_fir.tdf Device: EPF10K50VBC356-2

Estimating the Power Consumption of the Application

Internal Power Calculation

FLEX 10K, FLEX 8000 & FLEX 6000 Devices

Standby current ($I_{CCSTANDBY}$)	$I_{CCSTANDBY}$ =	0.500	mA
Coefficient for I_{CC} calculation. See the appropriate device family data sheet for this value.	K =	45	µA/(MHz × LE)
Maximum clock frequency ($\mathbf{f_{MAX}}$)	$\mathbf{f_{MAX}}$ =	50	MHz
Total number of logic elements used in the device (N)	N =	2,747	LE
Average ratio of logic cells toggling ($\mathbf{tog_{LC}}$) at each clock (typically 0.125)	$\mathbf{tog_{LC}}$ =	0.125	
Total internal current (I_{CCINT})	I_{CCINT} =	773.09	mA
$I_{CCINT} = I_{CCSTANDBY} + K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}}$			
Total internal power (P_{INT})	P_{INT} =	2,551.2	mW
$P_{INT} = V_{CC} \times I_{CCINT}$			

External Power Calculation for All Altera Devices

Power consumed by the DC output load (P_{DCOUT})	P_{DCOUT} =	35	mW
$P_{DCOUT} = P_{DCn}$			
Average capacitive load (C_{AVE}) at output pins	C_{AVE} =	35	pF
Number of output/bidirectional pins in the design (OUT)	OUT =	150	
Average ratio of I/O pins toggling ($\mathbf{tog_{IO}}$) at each clock (typically 0.125)	$\mathbf{tog_{IO}}$ =	0.125	
Power consumed by AC output load (P_{ACOUT})	P_{ACOUT} =	178.66	mW
$P_{ACOUT} = 1/2 \times OUT \times C_{AVE} \times 3.3\ V \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}} \times 3.3\ V \times 0.001$			
Total external power (P_{IO})	P_{IO} =	213.66	mW
$P_{IO} = P_{DCOUT} + P_{ACOUT}$			

Total Power Calculation for All Altera Devices

Estimated total power (P_{EST})	P_{EST} =	2,764.9	mW
$P_{EST} = P_{INT} + P_{IO}$			

Figure 2. Sample Power Evaluation for a FLEX 10K Device (Part 2 of 2)

Calculating Maximum Allowed Power for the Device & Package

Thermal resistance of the device	θ_{JA} =	8	° C/W
Maximum junction temperature (T_J) as specified in the appropriate device family data sheet.	T_J =	85	° C
Ambient temperature (T_A) of the design	T_A =	40	° C
Maximum power (P_{MAX}) allowed for the device	P_{MAX} =	5.625	W

$P_{MAX} = (T_J - T_A) / \theta_{JA}$

Comparing Maximum Power Allowed & Estimated Power

Is $P_{EST} < P_{MAX}$? (Yes) or No

Figure 3. Sample Power Evaluation for a MAX 9000 Device (Part 1 of 2)

Design: atm_pkt.tdf Device: EPM9560ARC304-15

Estimating the Power Consumption of the Application

Internal Power Calculation

MAX 9000, MAX 7000 & MAX 3000A Devices

Coefficients for I_{CC} calculation. See the appropriate device family data sheet for these values.	A =	0.68	mA/LE
	B =	0.26	mA/LE
	C =	0.052	mA/(MHz × LE)
Number of macrocells with the Turbo Bit on (MC_{TON})	MC_{TON} =	139	LE
Number of macrocells in the device (MC_{DEV})	MC_{DEV} =	560	LE
Number of macrocells in the design (MC_{USED})	MC_{USED} =	500	LE
Maximum clock frequency ($\mathbf{f_{MAX}}$)	$\mathbf{f_{MAX}}$ =	40	MHz
Average ratio of logic cells toggling ($\mathbf{tog_{LC}}$) at each clock (typically 0.125)	$\mathbf{tog_{LC}}$ =	0.125	
Total internal current (I_{CCINT})	I_{CCINT} =	333.98	mA
$I_{CCINT} = (A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$			
Total internal power (P_{INT})	P_{INT} =	1,669.9	mW
$P_{INT} = V_{CC} \times I_{CCINT}$			

External Power Calculation for All Altera Devices

Power consumed by the DC output load (P_{DCOUT})	P_{DCOUT} =	50	mW
$P_{DCOUT} = P_{DCn}$			
Average capacitive load (C_{AVE}) at output pins	C_{AVE} =	35	pF
Number of output/bidirectional pins in the design (OUT)	OUT =	211	
Average ratio of I/O pins toggling ($\mathbf{tog_{IO}}$) at each clock (typically 0.125)	$\mathbf{tog_{IO}}$ =	0.125	
Power consumed by AC output load (P_{ACOUT})	P_{ACOUT} =	350.79	mW

Figure 3. Sample Power Evaluation for a MAX 9000 Device (Part 2 of 2)

$P_{ACOUT} = 1/2 \times OUT \times C_{AVE} \times 3.8\ V \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}} \times 5\ V \times 0.001$

Total external power (P_{IO}) P_{IO} = 400.79 mW

$P_{IO} = P_{DCOUT} + P_{ACOUT}$

Total Power Calculation for All Altera Devices

Estimated total power (P_{EST}) P_{EST} = 2,070.69 mW

$P_{EST} = P_{INT} + P_{IO}$

Calculating Maximum Allowed Power for the Device & Package

Thermal resistance of the device θ_{JA} = 8 °C/W

Maximum junction temperature (T_J) as specified in the appropriate device family data sheet. T_J = 90 °C

Ambient temperature (T_A) of the design T_A = 70 °C

Maximum power (P_{MAX}) allowed for the device P_{MAX} = 2.5 W

$P_{MAX} = (T_J - T_A) / \theta_{JA}$

Comparing Maximum Power Allowed & Estimated Power

Is $P_{EST} < P_{MAX}$? (Yes) or No

Thermal Management

The following guidelines reduce power dissipation and heat build-up for an application:

- *Use available low-power features of the device.* By turning the Turbo Bit™ off, Classic™ devices and individual macrocells in MAX 9000, MAX 7000, and MAX 3000A devices can be configured for low-power operation, with only a nominal increase in propagation delays. Macrocells in MAX 9000, MAX 7000, or MAX 3000A devices that do not need to run in high-performance mode should be set to low-power mode.
- *Choose a different device package.* A ceramic or higher-pin-count package can be used. Ceramic packages dissipate more heat than plastic packages. Also, packages with higher pin counts can dissipate more heat through the connections to the printed circuit board (PCB).
- *Use forced-air cooling and/or heat-sinking.* Forced-air cooling improves the efficiency of convection cooling, which reduces the surface temperature of the device. A heat sink connected to a device significantly increases heat dissipation by radiating heat via the metal mass.

- *Slow the operation in portions of the circuit.* I_{CC} is proportional to the frequency of operation. Slowing parts of a circuit lowers the I_{CC} and hence reduces the power. Altera devices provide global or array clock sources for all registers. Signals that do not require high-speed operation can use a slower array clock that significantly reduces the system power consumption.

- *Reduce the number of outputs.* DC and AC current is required to support all I/O pins on the device. Reducing the number of I/O pins may reduce the current necessary for the device, and thereby reduce the power.

- *Reduce the amount of circuitry in the device.* Power depends on the amount of internal logic that switches at any given time. Reducing the amount of logic in a device reduces the current in the device. The same effect may be achieved by using a larger device, which also provides increased heat dissipation and maintains a single-device solution.

- *Choose a different device family.* Some device families consume less power than others. For example, the MAX 7000 family provides more power-saving features than the MAX 5000 family. The Classic family provides power-saving features for low-density designs, and low-speed designs consume less power when implemented in FLEX devices.

- *Modify the design to reduce power.* Identify areas in the design that can be revised to reduce the power requirements. Common solutions include reducing the number of switching nodes and/or required logic, and removing redundant or unnecessary signals. For assistance in locating less obvious changes, contact Altera Applications at (800) 800-EPLD.

Revision History

The information contained in *Application Note 74 (Evaluating Power for Altera Devices)* version 3.01 supersedes information published in previous versions. In version 3.01, Table 1 was added.