Designing with FineLine BGA Packages

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Introduction

As programmable logic devices (PLDs) increase in density and I/O pins, the demand for small packages and diverse packaging options continues to grow. Ball-grid array (BGA) packages are an ideal solution because the I/O connections are on the interior of the device, improving the ratio between pin count and board area. Typical BGA packages contain up to twice as many connections as quad flat pack (QFP) packages for the same area. Further, BGA solder balls are considerably stronger than QFP leads, resulting in robust packages that can tolerate rough handling.

Altera has developed a new BGA solution for users of high-density PLDs called the FineLine BGA™ package. The new format requires less than half the board space of standard BGA packages. This application note provides guidelines for designing your printed circuit board (PCB) for Altera's FineLine BGA packages and discusses the following topics:

- Overview of BGA packages
- PCB layout terminology
- PCB layout for FineLine BGA packages

Overview of BGA Packages

As PLDs grow to 1 million gates and beyond, designers require more advanced, flexible packages. BGA packages empower designers by offering the technological benefits and flexibility to meet future system requirements.

In BGA packages, the I/O connections are located on the interior of the device. Leads normally placed along the periphery of the package are replaced with solder balls arranged in a matrix across the bottom of the substrate. The final device is soldered directly to the PCB using assembly processes virtually identical to the standard surface mount technology preferred by system designers.

In addition, BGA packages provide the following advantages:

- *Fewer damaged leads*—BGA leads consist of solid solder balls, which are less likely to suffer damage during handling.

- *More leads per unit area*—Lead counts are increased by moving the solder balls closer to the edges of the package and by decreasing the pitch to 1.0 mm.

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- *Less expensive surface mount equipment*—BGA packages can tolerate slightly imperfect placement during mounting, requiring less expensive surface mount equipment. The placement can be imperfect because the BGA packages self-align during solder reflow.

- *Smaller footprints*—BGA packages are usually 20% to 50% smaller than QFP packages, making BGA packages more attractive for applications that require high performance and a smaller footprint.

- *Integrated circuit speed advantages*—BGA packages can operate well into the microwave frequency spectrum and can achieve high electrical performance by using ground planes, ground rings, and power rings in the package construction.

- *Improved heat dissipation*—Because the die is located at the center of the FineLine BGA package and most VCC and GND pins are located at the center of the package, the GND and VCC pins are located under the die. As a result, the heat generated in the device can be transferred out through the GND and VCC pins (i.e., the GND and VCC pins act as a heat sink).

PCB Layout Terminology

This section defines common terms used in PCB layout.

Escape Routing

Escape routing is the method used to route each signal from a package to another element on the PCB.

Multi-Layer PCBs

The increased I/O count associated with BGA packages has made multi-layer PCBs the industry-standard method for performing escape routing. Signals can be routed to other elements on the PCB through various numbers of PCB layers.

Vias

Vias, or plated through holes, are used in multi-layer PCBs to transfer signals from one layer to another. Vias are actual holes drilled through a multi-layer PCB and provide electrical connections between various PCB layers. All vias provide layer-to-layer connections only; device leads or other reinforcing material are not inserted into vias.

Table 1 describes the terms used to define via dimensions.

Table 1. Via Dimension Terms

Term	Definition
Aspect ratio	The aspect ratio is the ratio of a via's length or depth to its pre-plated diameter.
Drilled hole diameter	The drilled hole diameter is the diameter of the actual via hole drilled in the board.
Finished via diameter	The finished via diameter is the diameter of a via hole that has been finished.

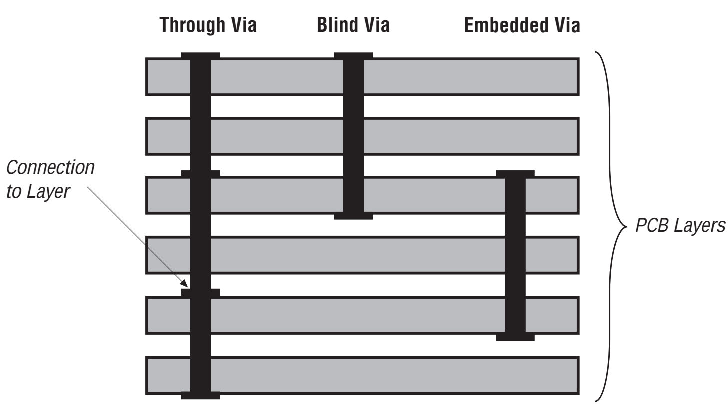
Table 2 shows the three via types typically used on PCBs.

Table 2. Via Types

Type	Description
Through via	An interconnection between the top and the bottom layer of a PCB. Through vias can also provide interconnections to inner PCB layers.
Blind via	An interconnection from the top or bottom layer to an inner PCB layer.
Embedded via	An interconnection between any number of inner PCB layers.

Figure 1 shows all three via types.

Figure 1. Types of Vias



Blind vias and through vias are used more frequently than embedded vias. Blind vias can be more expensive than through vias, but overall costs can be reduced because signal traces can be routed under a blind via, requiring fewer PCB layers. Through vias, on the other hand, do not permit signals to be routed through lower layers, which can increase the required number of PCB layers and overall costs.

Via Capture Pad

Vias are connected electrically to PCB layers through via capture pads, which surround each via.

Surface Land Pad

Surface land pads are the areas on the PCB to which the BGA solder balls adhere. The size of these pads affects the space available for vias and escape routing. In general, surface land pads are available in the following two basic designs:

- Non solder mask defined (NSMD), also known as copper defined
- Solder mask defined (SMD)

The main differences between the two surface land pad types are the size of the trace and space, the type of vias you can use, and the shape of the solder balls after solder reflow.

Non Solder Mask Defined Pad

In the non solder mask defined (NSMD) pad, the solder mask opening is larger than the copper pad. Thus, the surface land pad's copper surface is completely exposed, providing greater area to which the BGA solder ball can adhere (see Figure 2). Altera recommends that you use a NSMD pad for most applications because it provides more flexibility, fewer stress points, and more line-routing space between pads.

Solder Mask Defined Pad

In the solder mask defined (SMD) pad, the solder mask overlaps the surface land pad's copper surface (see Figure 2). This overlapping provides greater adhesion strength between the copper pad and the PCB's epoxy/glass laminate, which can be important under extreme bending and during accelerated thermal cycling tests. However, the solder mask overlap shrinks the amount of copper surface available for the BGA solder ball.

Figure 2. Side View of NSMD & SMD Land Pads

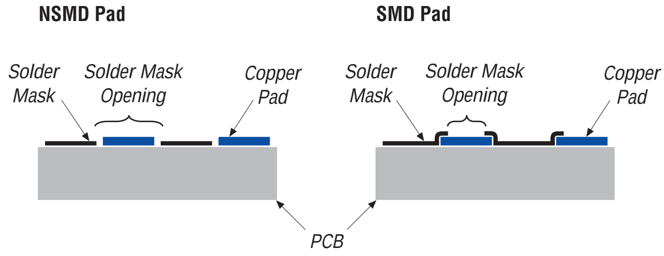
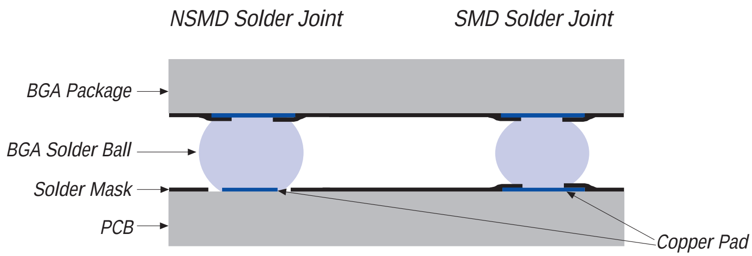


Figure 3 shows the side view for an NSMD and SMD solder joint.

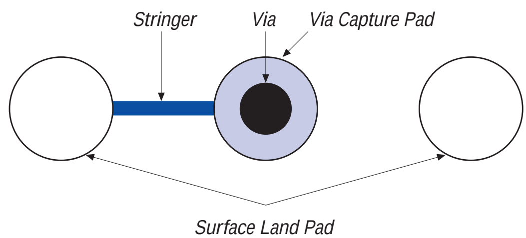
Figure 3. Side View of NSMD & SMD Solder Joints



Stringer

Stringers are rectangular or square interconnect segments that electrically connect via capture pads and surface land pads. Figure 4 shows the connection between vias, via capture pads, surface land pads, and stringers.

Figure 4. Via, Land Pad, Stringer & Via Capture Pad



PCB Layout for FineLine BGA Packages

When designing a PCB for FineLine BGA packages, consider the following factors:

- Surface land pad dimension
- Via capture pad layout and dimension
- Signal line space and trace width
- Number of PCB layers

☞ For all FineLine BGA figures, the controlling dimension is millimeters.

Surface Land Pad Dimension

Surface land pads should be the same size as the BGA pad to provide a balanced stress on solder joints. For this reason, Altera recommends using a 15.75-mil surface land pad, because it is the same size as the BGA pad. Figure 5 shows a 15.75-mil BGA pad.

Figure 5. 15.75-Mil BGA Pad

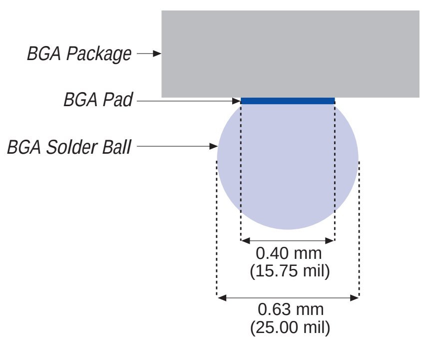
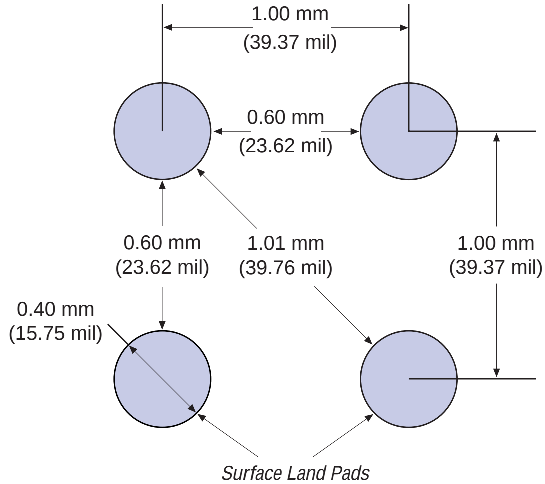


Figure 6 shows how much space is available for vias and escape routing when you use 15.75-mil surface land pads.

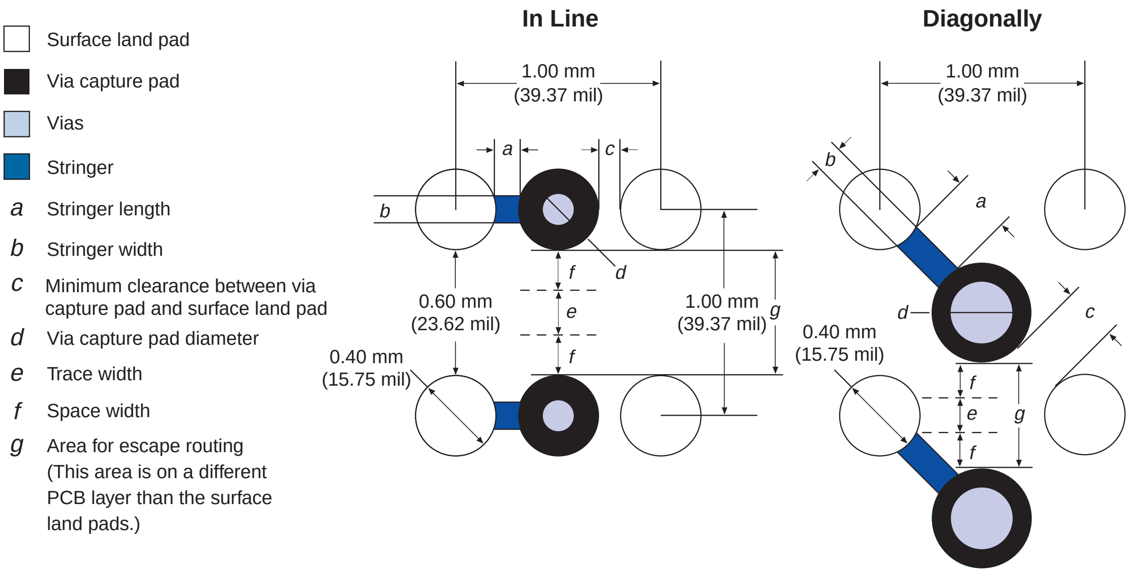
Figure 6. Space Available for 15.75-Mil Surface Land Pads



Via Capture Pad Layout & Dimension

The size and layout of via capture pads affect the amount of space available for escape routing. In general, you can layout via capture pads in the following two ways: in-line with the surface land pads or in the diagonal of surface land pads. Figure 7 shows both layouts.

Figure 7. Placement of Via Capture Pad



The decision to place the via capture pads diagonally or in-line with the surface lands pads is based on the following factors:

- Diameter of the via capture pad
- Stringer length
- Clearance between via capture pad and surface land pad

To decide how to lay out your PCB, use the information shown in Figure 7 and Table 3. If your PCB design guidelines do not conform to either equation in Table 3, contact Altera Applications for further assistance.

Table 3. Formula for Via Layouts

Layout	Formula
In-line	$a + c + d \leq 23.62$ mil
Diagonally	$a + c + d \leq 39.76$ mil

Table 3 shows that you can place a larger via capture pad diagonally than in-line with the surface land pads.

Via capture pad size also affects how many traces can be routed on a PCB. Figure 8 shows sample layouts of typical and premium via capture pads. The typical layout shows a via capture pad size of 27 mil, a via size of 8 mil, and an inner space/trace of 4 mil. With this layout, only one trace can be routed between the vias. If more traces are required, you must reduce the via capture pad size or the space/trace size.

The premium layout shows a via capture pad size of 20 mil, a via size of 5 mil, and an inner space/trace of 3 mil. This layout provides enough space to route two traces between the vias.

Figure 8. Typical & Premium Via Capture Pad Sizes

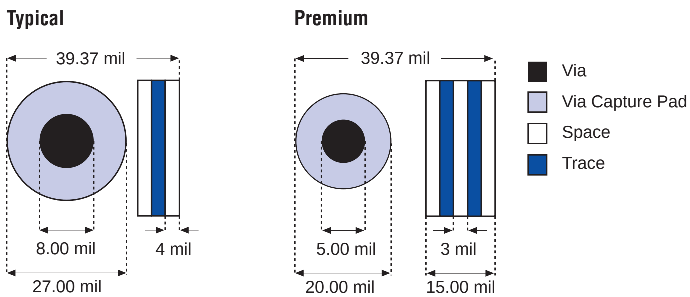


Table 4 shows the typical and premium layout specifications used by most PCB vendors.

Table 4. Vendor Specifications

Specification	Typical (Mil)	Premium (Mil)
Trace/space width	5/5	3/3
Drilled hole diameter	12	10
Finished via diameter	8	≤ 5
Via capture pad	25.5	20
Aspect ratio	7:1	10:1

For detailed information on drill sizes, via sizes, space/trace sizes, or via capture pad sizes, contact your PCB vendor directly.

Signal Line Space & Trace Width

The ability to perform escape routing is defined by the width of the trace and the minimum space required between traces. The minimum area for signal routing is the smallest area that the signal must be routed through (i.e., the distance between two vias, or g in Figure 7). This area is calculated by the following formula:

$$g = 39.37 - d$$

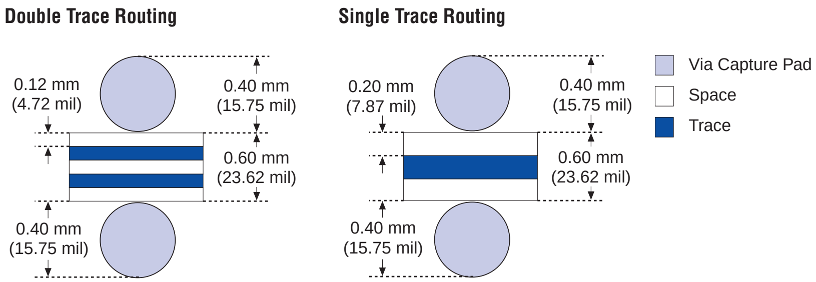
The number of traces that can be routed through this area is based on the permitted line trace and space widths. You can use Table 5 to determine the total number of traces that can be routed through g.

Table 5. Number of Traces

Number of Traces	Formula
1	$g \geq [2 \times (\text{space width})] + \text{trace width}$
2	$g \geq [3 \times (\text{space width})] + [2 \times (\text{trace width})]$
3	$g \geq [5 \times (\text{space width})] + [3 \times (\text{trace width})]$

Figure 9 shows that by reducing the trace and space size, you can route more traces through g. Increasing the number of traces reduces the required number of PCB layers and decreases the overall cost.

Figure 9. Escape Routing for Double & Single Traces



Number of PCB Layers

In general, the number of PCB layers required to route signals is inversely proportional to the number of traces between vias (i.e., the greater the number of traces, the fewer the number of PCB layers required). You can estimate the number of layers your PCB requires by first determining:

- Trace and space size
- Number of traces routed between the via capture pads
- Type of vias used

Table 6 shows the number of PCB layers required to route signals for various FineLine BGA packages in EPF10K50E devices, assuming the use of a power plane, ground plane, and all I/O pins. This table shows that using double traces and blind vias reduces the required number of layers.

Table 6. Maximum Required PCB Layers

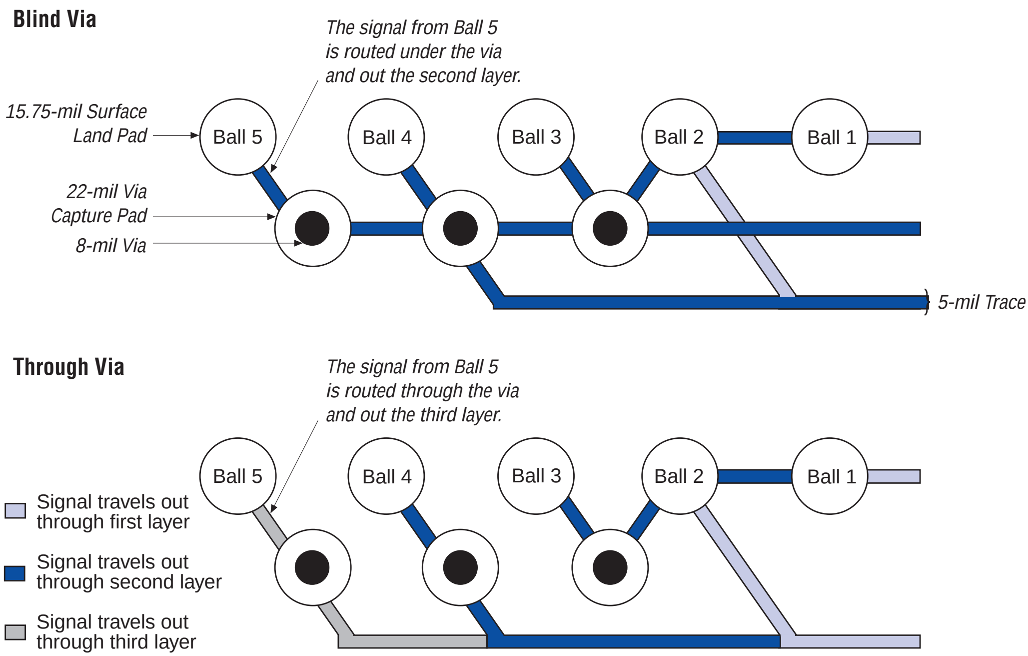
FineLine BGA Package (Balls)	Single Trace		Double Trace	
	Blind Vias (Layers)	Through Vias (Layers)	Blind Vias (Layers)	Through Vias (Layers)
100	2	2	1	1
144	*(1)*	*(1)*	*(1)*	*(1)*
256	2	2	2	2
324	*(1)*	*(1)*	*(1)*	*(1)*
484	2	3	2	2
672	3	4	2	3
1,020	*(1)*	*(1)*	*(1)*	*(1)*

Note:

(1) For information on the number of PCB layers required, contact Altera Applications at (800) 800-EPLD.

Using fewer I/O pins than the maximum can reduce the required number of layers. Via type can also reduce the number of layers required. To see how the via type can affect the required number of PCB layers, consider the sample layouts shown in Figure 10.

Figure 10. Sample PCB Layout



The blind via layout in Figure 10 requires only two PCB layers. The signals from the first two balls can be routed directly through the first layer. The signals from the third and fourth balls can be routed through a via and out the second layer, and the signal from the fifth ball can be routed under the vias for Ball 4 and Ball 3 and out the second layer. Together, only two PCB layers are required.

In contrast, the through via layout in Figure 10 requires three PCB layers, because signals cannot be routed under through vias. The signals from the third and fourth balls can still be routed through a via and out the second layer, but the signal from the fifth ball must be routed through a via and out the third layer. Using blind vias rather than through vias in this example saves one PCB layer.

Conclusion

Altera has taken a leadership position in PLD packaging with the recent introduction of 1.00-mm FineLine BGA packages. These packages use a reduced PCB area while maintaining a very high pin count. By using the information in this application note, you can easily design PCBs to use FineLine BGA packages, and take advantage of the package's reduced size.

Revision History

Information contained in *Application Note 114 (Designing with FineLine BGA Packages)* version 1.03 supersedes information published in previous versions.

Version 1.03

Version 1.03 of *Application Note 114 (Designing with FineLine BGA Packages)* contains the following changes:

- Dimensions in Figures 5, 6, 7, 9, and 10 and Tables 3 and 6 were updated.
- Minor textual and style changes were made throughout the document.

Version 1.02

Version 1.02 of *Application Note 114 (Designing with FineLine BGA Packages)* contains the following changes:

- The dimension of the BGA solder ball in Figure 5 was updated.
- The surface land pad size in Figure 10 was updated.

Version 1.01

Version 1.01 of *Application Note 114 (Designing with FineLine BGA Packages)* contains the following changes:

- Information is Table 6 was updated.
- Minor textual and style changes were made throughout the document.