Implementing Voice Over Internet Protocol

Introduction

This application note describes an example implementation of voice over Internet protocol (VOIP) functionality using Altera® high-density APEX™ devices and intellectual property (IP) functions from the Altera Megafunction Partners Program (AMPP ᴿᴹ) and the MegaCore® program.

This application note discusses the following topics:

- VOIP fundamentals
- Creating a system-on-a-programmable-chip (SOPC) solution with APEX devices
- IP functions that can be used in a VOIP system

VOIP Fundamentals

A VOIP system captures, packetizes, and transports telephone conversations (voice data) over a network originally designed to transport computer-generated data (a data network). This new approach to transporting voice traffic solves long-term cost issues for organizations that use existing voice traffic transport systems, called circuit-switched networks. By implementing VOIP and transporting voice traffic over the Internet, circuit-switched networks and their associated maintenance costs are replaced by a less expensive solution.

Comparing Circuit-Switched Networks & Data Networks

The topology and behavior of circuit-switched networks and data networks are significantly different. Voice traffic carried over a system originally designed for data creates technical challenges that must be addressed to ensure a high quality of service (QoS). QoS refers to the ability of a network to satisfy voice traffic and service requirements. Circuit-switched networks sacrifice maintenance costs for a high QoS, and data networks sacrifice QoS for bandwidth efficiency.

Circuit-switched networks have a high QoS because they dedicate bandwidth resources to each individual call for the duration of that call. However, dedicating permanent resources to an individual call creates significant cost disadvantages for circuit-switched networks. Additionally, because most voice conversation consists of "pauses" where no voice transmission takes place, circuit-switched networks cannot utilize available bandwidth efficiently, resulting in a cost disadvantage when compared to data networks.

Unlike circuit-switched networks, data networks do not dedicate permanent resources to an individual call between two locations. Instead, data is prepared for network transport by attaching classification information to the packet header, which is attached to the payload. The data network uses the path in the network that optimizes the utilization of available bandwidth. Figure 1 illustrates how voice data can be prepared for traveling over a data network.

Figure 1. Packetization of Voice Traffic
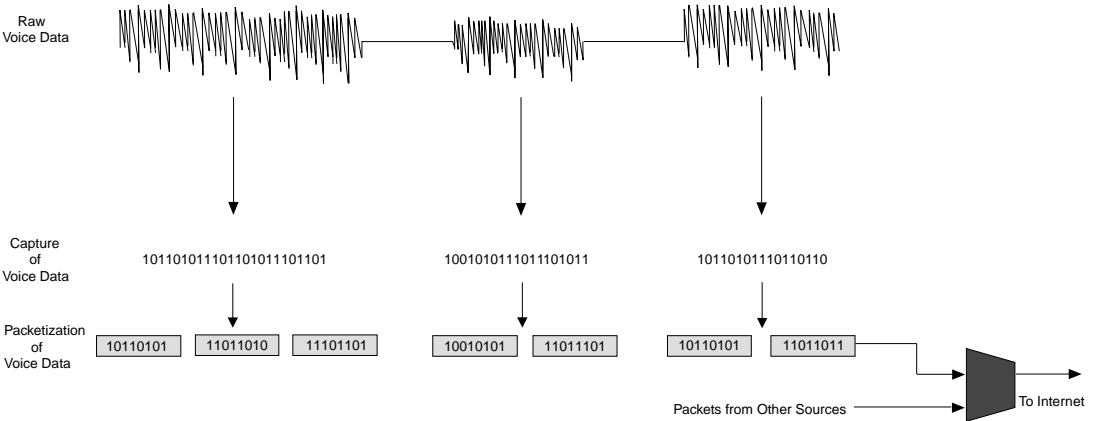
Absence of Industry Standards

Currently, very few industry standards exist for VOIP products. System implementations vary from complete software architectures to complete hardware architectures to combinations of both. Because a VOIP environment lacks defined standards, specifying and fabricating an ASIC device using a particular standard introduces significant risk as standards evolve. Altera programmable logic devices (PLDs) in VOIP-enabled products are ideal because they can be reconfigured and can provide fast time-to-market.

Altera & VOIP

To illustrate the advantages of designing a VOIP system using Altera products, this application note details the architecture of a VOIP gateway. The VOIP gateway architecture is an example of how to utilize APEX devices and IP functions that reduce system costs and simplify the development cycle.

Intellectual Property

Altera provides a range of IP functions that give the designer access to a vast array of applications commonly used within VOIP applications. Parameterizable, shrink-wrapped solutions allow the designer to concentrate on system architecture optimization. The VOIP system example uses more than 20 different IP functions, all of which can be obtained from the AMPP and MegaCore programs on the Altera web site at **http://www.altera.com/IPMegaStore**.

APEX Device Family

The Altera APEX family of high-density PLDs offers a number of advantages for developing VOIP systems. APEX devices can be reconfigured to meet future standards, even when deployed in the field. Content addressable memory (CAM) can be implemented on-chip to perform quick searches for routing information. The APEX device family also supports the gunning transceiver logic plus (GTL+) I/O standard, which can be used to implement the stringent requirements for a Time-Division Multiplexed (TDM) bus.

Quartus Software

The Quartus™ software provides a world-class SOPC development environment and also incorporates best-in-class third-party tool flows with NativeLink™ integration to achieve the best design possible for APEX devices. Additionally, the Quartus software features the SignalTap™ logic analyzer, an SOPC debugging tool.

☞   For more information on the SignalTap logic analyzer, see the *SignalTap Embedded Logic Analyzer Megafunction Data Sheet*.

SOPC Solution Example for VOIP

The VOIP gateway example network system provided in this section highlights the IP functions and APEX device features that can provide implementation-level benefits to VOIP developers. The VOIP gateway network system consists of a shelf, which contains three bus lines and two types of cards, each featuring an APEX device. Figure 2 shows an overview of an example VOIP gateway network system.

Figure 2. VOIP Network System Overview
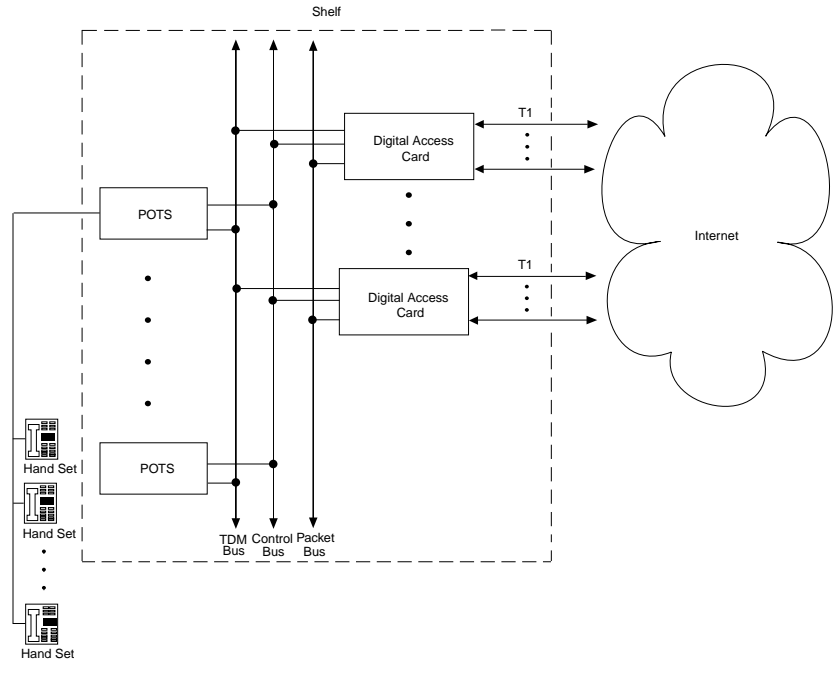
The first type of card in the VOIP network interfaces with the Internet infrastructure and is referred to as the digital access card (DAC). The second type of card manages the interface between the telephone hardware and the routing network. Because much of its functionality is based on standard telephony requirements, it is referred to as a "plain old telephone service" (POTS) card. Additional DAC and POTS cards can be added to the system to meet the availability and performance needs of the service.

Telephones are connected externally to the cards with a standard telephone wire that connects to the POTS card. Each POTS card can handle up to 128 phone lines, and the system can be scaled to meet specific needs by adding POTS cards to the board.

The DAC cards interface with the Internet via a T1 line. Each DAC card can carry up to four T1 lines. In this example, The T1 lines connect the gateway to the Internet via a frame relay network; however, other types of networks can also be connected to a similar shelf.

Three separate buses allow control and data information to be passed between all cards in the system. The TDM bus carries unpacketized voice data between all cards in the system. The Packet bus carries voice traffic in ethernet packets between DAC cards, and the Control bus manages communication between the DAC and POTS cards.

POTS Card

The POTS card is similar to other standard cards used in telephone networking systems today. In the POTS card example used in this document, all possible functionality available in the form of IP functions has been implemented within an APEX device to demonstrate the functionality of an SOPC. Figure 3 illustrates the role of the IP functions and the APEX device within the POTS card.

Figure 3. POTS Card Functional Diagram
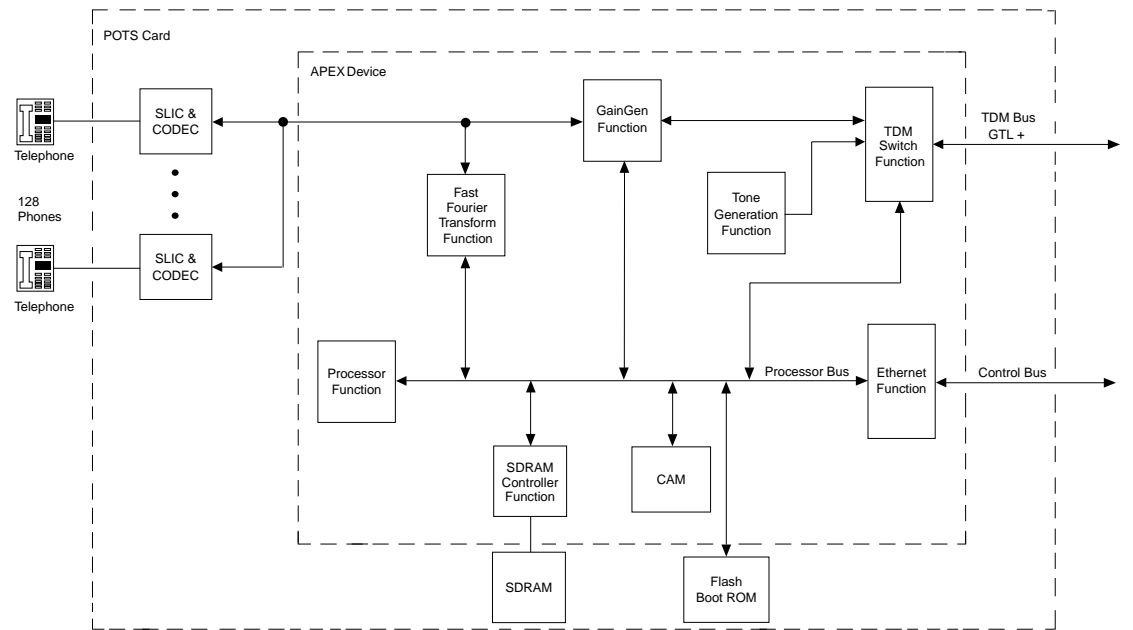
The POTS card's primary purpose is to route calls to and from its attached telephones. It does not perform any packetization. The subscriber line interface circuit (SLIC) and the standard coder/decoder (CODEC) convert the voice signal to digital data and compress the pulse-code modulation (PCM) signal.

The following section describes in detail the role of each IP function in the APEX EP20K200EFC672-1 device for the VOIP system example. This particular APEX device was chosen because it offers the right combination of logic capacity and memory.

This section describes the following IP functions in the POTS card:

- Gain Generation Function
- TDM Switch Function
- Tone Generation Function
- Processor Function
- Ethernet Media Access Control (MAC) Function
- Tone Detection Function
- Memory Functions

Gain Generation Function

When the digitized voice data is multiplexed together off-chip, the Gain Generation function receives the voice data and adjusts the gain to the appropriate level, depending on the final destination of the voice signal. If the voice data is to be sent over the Internet, a decibel adjustment may not be necessary. If a call is to be sent within the gateway, a standard 6-dB loss may be added to the signal. Regardless of the call's final destination or the number of signals on the bus, the function can easily scale the appropriate gain level with the correct processor input.

TDM Switch Function

Once the gain is properly adjusted, the Time-Division Multiplexed (TDM) Switch function receives the incoming data and maps it to the appropriate destination. The TDM Switch function samples the incoming multiplexed signal and sends data over the TDM bus according to instructions provided by the microprocessor.

The TDM Switch function reduces the constant delay to 125 ms for an 8 kHz signal. Also, the variable frame width/bit level switching feature allows greater control between channels. The number of input streams, output streams, bits per time slot, and time slots per frame can be modified to meet specific system needs. Because many POTS cards may introduce contention on the TDM bus, collision detection is enabled with a GTL+ bus I/O interface, available directly on the APEX device. If a collision is detected, every card in the system can be notified via the Ethernet control bus.

Tone Generation Function

The Tone Generation function provides up to 32 audible tones informing the user of the operation mode for the current call. The selected tones are not turned on or off, but are simultaneously supplied to the TDM Switch function (the Tone Generation function does not have an input). The TDM Switch function selects the appropriate tone based on the data it receives from the Processor bus. The TDM Switch function sends this tone as a signal back to the handset.

For example, when a call has been routed successfully and is waiting for a response, the processor in the POTS card tells the TDM Switch to select the channel that generates a "ringing" sound. If the other end of the connection is already in use, the processor instructs the TDM Switch function to select the channel that generates a "busy" signal.

The Tone Generation function from AMPP partner NComm, Inc. has a MegaWizard® Plug-In, which allows the user to select only the tone parameters required. Using the MegaWizard interface also ensures optimum embedded system block (ESB) usage by calculating the least number of PCM samples required to generate the tone sequence. The Tone Generation function also supports optional gain control, Mu-law, and A-law encoding. The resource utilization summary in this example reflects the instantiation of the NComm function, which includes a dial tone, ring back tones, and a busy signal.

Processor Function

The Processor function is modeled on the 32-bit MIPS-based™ instruction set with an R3000 class architecture. It is capable of operating at 33 MHz on an Altera APEX device and executes instructions over a five-stage pipeline. All transactions within the Processor and its interfaces occur on the positive edge of the processor clock and do not require two-phase clocks for implementation. As a result, the Processor function does not use on-chip phase-locked loops (PLLs). The Processor function selected for this example is the LX-4180 from Lexra.

The Processor function receives input from an incoming call and determines where to route the signal based on the phone number dialed (outgoing) or the IP address (incoming). It also supplies control information to peripheral IP functions, including the Tone Generation function, the Fast Fourier Transform (FFT) function, and SDRAM Controller functions. The Processor function on the POTS card only accesses the TDM bus and the Control bus via the Ethernet function. The TDM bus does not have access to the Packet bus, which is reserved for communication between the DAC cards.

All 32-bit co-processor operations are supported, including moves to and from the co-processor's general registers and control registers. The co-processor loads and stores based on the co-processor condition flags. All co-processor operations execute in a single clock cycle without pipeline stalls. The Processor function also features configurable cache sizes and separate data and instruction memory spaces, which are implemented using ESBs in the APEX device.

Ethernet MAC Function

The Ethernet function transmits and receives signals on the Control bus. The function implements the media access control (MAC) and complies with the IEEE standard 802.3. The Ethernet function selected for this example is from CoreEl Microsystems. This function supports both Reduced Media Independent Interface (RMII) and Media Independent Interface (MII) to the physical ethernet layer, which is implemented off-chip. The instantiation in this example uses the MII interface and supports a 16-bit host interface.

Tone Detection Function

The Tone Detection block is not an IP function from Altera or its AMPP partners; it is a custom piece of logic. The Tone Detection block detects tones generated by handsets and correlates these tones to the numerical address that represents the destination of the call.

Memory Functions

There are three types of memory functions within the POTS card example: Flash ROM, SDRAM, and CAM.

The Flash ROM stores the software needed to initialize all of the hardware. The SDRAM Controller provides a handshaking protocol to the processor function and a standard interface to the SDRAM. This example system requires 32 Mbytes of off-chip SDRAM. The SDRAM Controller allows programmable or constrained timing, as well as bank management and bus cascading. The SDRAM Controller also supports up to eight banks of memory with 2 Gbits of memory space and has a maximum speed of 133 MHz within an APEX device in a single data rate mode. A special interface for connecting the 32-bit MIPS-based processor to the SDRAM Controller is required to complete the integration of these two functions.

CAM, which is implemented within the APEX device, performs quick database searches for routing information. In the POTS card, CAM stores telephone numbers corresponding to specific IP addresses, allowing the processor to execute faster searches.

Digital Access Card

The DAC card, shown in Figure 4, prepares data for travel over the Internet, unpacks data received from the Internet via T1 lines, and converts it back to the voice format used by the shelf. In addition to the Ethernet control and TDM Switch buses, the DAC also uses an Ethernet packet bus which routes packetized voice information between DAC cards on the shelf.

Figure 4. DAC Card Block Diagram
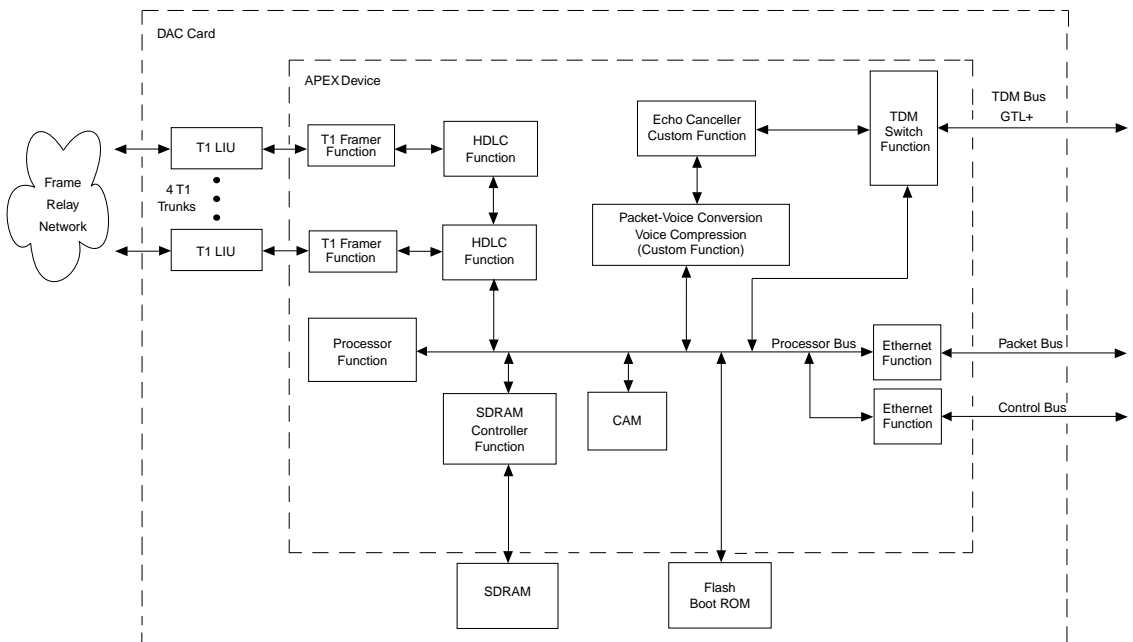
The DAC card can support up to 4 T1 lines. The DAC card can also access all three buses in the shelf: the TDM Switch bus, the Control bus (Ethernet-based) and the Packet bus (Ethernet-based). The APEX device selected for the DAC card, based on resource requirements, is the EP20K400EFC672-1.

The T1 line interface unit (LIU) is an off-chip, analog device that connects the APEX device to the packet network. In this example, frame relay is the protocol for the packet network. When the APEX device receives the synchronous signal, the packets are streamed through the T1 Framer function for bit detection.

The following section describes in detail the role of each IP function in the DAC card for the VOIP system example.

This section describes the following IP functions:

- T1 Framer Function
- High-Level Data Link Controller (HDLC) Function
- TDM Switch Function
- Processor Function
- Ethernet MAC Function
- Memory Functions

T1 Framer Function

The T1 Framer function identifies every 193rd bit of data as the framing bit, with the first 192 bits of data carrying addresses and packetized voice information. This function partitions the bit stream for processing by using the HDLC function. Each T1 Framer function handles one T1 line with up to four T1 lines per board. The T1 Framer function selected in this example is from CoreEl Microsystems, an Altera AMPP partner. When transmitting, the function clocks data in serial form and puts it in frame format as a serial T1 stream.

HDLC Function

The HDLC function adds and removes protocol information during packet transit. When a packet arrives from the frame relay network, it no longer needs the communication protocol bits required for network transit. Therefore, these protocol bits are stripped, leaving the packet with its local routing information. When leaving the system to enter the network, the packet needs these bits added to its addressing information.

The HDLC function used in this example is from Premier AMPP partner Innocor Ltd. The HDLC function is a high-performance module for bit-oriented data transmission. The function was designed to maximize speed while reducing resource consumption on the APEX device. Available control features include a 16-bit cycle redundancy checker (CRC), flag insertion/deletion, zero insertion/detection, and abort generation/detention. The design is fully synchronous and can operate at up to 51 MHz.

TDM Switch Function

Once the gain is properly adjusted, the TDM Switch function receives the incoming data and maps it to the appropriate destination. The TDM Switch function samples the incoming multiplexed signal and sends the data over the TDM bus according to instructions provided by the microprocessor.

The TDM Switch function reduces the constant delay to 125 ms for an 8 kHz signal. Also, the variable frame width/bit level switching feature allows for greater control between channels. The number of input streams, output streams, bits per time slot, and time slots per frame can be modified to meet specific system needs. Because many DAC cards may introduce contention on the TDM bus, collision detection is enabled with a GTL+ bus I/O interface, available directly on the APEX device. If a collision is detected, every card in the system can be notified via the Ethernet control bus.

Processor Function

The Processor function is modeled on the 32-bit MIPS-based instruction set with an R3000 class architecture. It is capable of operating at 33 MHz on an Altera APEX device and executes instructions over a five-stage pipeline. All transactions within the Processor and its interfaces occur on the positive edge of the processor clock and do not require two-phase clocks for implementation. As a result, the Processor function uses no on-chip PLLs. The Processor function selected for this example is the LX-4180 from AMPP partner Lexra.

The Processor function receives packetized information from the frame relay network and determines where to route the signal based on the phone number dialed (outgoing) or the IP address (incoming). The Processor function also supplies control information to peripheral IP functions including the Tone Generation function, the signal detection logic, and the SDRAM Controller functions. The Processor function does not have access to the Packet bus, which is reserved for communication between the DAC cards.

The system supports all 32-bit co-processor operations, including moves to and from the co-processor's general registers and control registers. The co-processor loads and stores based on the co-processor condition flags. All co-processor operations execute in a single clock cycle without pipeline stalls. The Processor function also features configurable cache sizes and separate data and instruction memory spaces, which are implemented using ESBs in the APEX device.

Ethernet MAC Function

The DAC card has two Ethernet MAC functions. One function provides MAC for the Control bus and the other function provides MAC for the Packet bus. The function implements the MAC and complies with the IEEE standard 802.3. The Ethernet MAC function selected for this example is from CoreEl Microsystems. This function supports both RMII and MII interfaces to the physical ethernet layer, which is implemented off-chip. The instantiation in this example uses the MII interface and supports a 16-bit host interface.

Memory Functions

The DAC card example uses three types of memory functions: Flash ROM, SDRAM, and CAM.

The Flash ROM stores the software needed to initialize all of the hardware. The SDRAM Controller provides a handshaking protocol to the processor and a standard interface to the SDRAM. This example system requires 32 Mbytes of off-chip SDRAM. The SDRAM Controller allows programmable or constrained timing, as well as bank management and bus cascading. The SDRAM Controller also supports up to eight banks of memory with 2 Gbits of memory space and has a maximum speed of 133 MHz in an APEX device in a single data rate mode. A special interface for the 32-bit MIPS-based processor to the SDRAM Controller is required to complete the integration of these two functions.

CAM, which is implemented within the APEX device, performs quick database searches for routing information. In the DAC card, CAM stores telephone numbers corresponding to specific IP addresses, allowing the processor to execute faster searches.

Reconfigurability

A fixed solution requires a separate board for each network to accommodate the packet protocols specific to each system. In the VOIP system described in this document, programmable logic allows the designer to replace the HDLC function with other network interface functions. For example, the same cards could be used in the same shelf by replacing the HDLC function with an asynchronous transfer mode (ATM) adaptation layer segmentation and reassembly (SAR) function to use the same board to connect to an ATM network. This approach not only cuts costs in board development and prototyping, but it also eliminates debugging problems associated with a multiple board solution.

Conclusion

As networks get larger and maintenance costs continue to rise, a VOIP network for voice communication becomes more attractive. Because VOIP is a major step in a new direction for voice communication, many solutions have been implemented in an attempt to best serve the marketplace. Altera provides a flexible VOIP network system solution using an APEX device and IP combination that can meet the changing needs of consumers as industry standards evolve and systems improve.

The Altera APEX device and IP functions enable designers to retain flexibility without sacrificing any functionality provided by a fixed solution. The APEX device comes equipped with advanced I/O and memory features providing designers with more options within the design environment. The Altera IP portfolio reduces time-to-market with a substantial set of advanced IP functions. The Altera IP functions also easily adjust to fit a designer's specific needs and work seamlessly with the Quartus design integration tool. Altera's APEX device and IP functions provide a powerful and flexible solution to the VOIP network system.

References

For more information on Altera IP functions and APEX devices, refer to the documents listed below. All documents are available through the Altera Megafunction Partners Program (AMPP) or through the Altera web site at **http://www. altera.com**.

- *FIR Compiler MegaCore Function User Guide*
- *SB 2 (High-Speed Adaptive FIR Filter Megafunction)*
- *SB 12 (Fast Fourier Transform MegaCore Function)*
- *Operating Requirements for Altera Devices Data Sheet*
- *Altera Device Package Information Data Sheet*
- *Using I/O Standards in the Quartus Software White Paper*
- *Quartus Programmable Logic Development System & Software Data Sheet*
- *AN 117 (Using Selectable I/O Standards in Altera Devices)*
- *AN 123 (Using Timing Analysis in the Quartus Software)*
- *AN 119 (Implementing High-Speed Search Applications with APEX CAM)*

Revision History

This revision removes references to the Echo Canceller function.

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