APEX Devices

High-Density Embedded Programmable Logic Devices for System-Level Integration

May 2000

APEX: A Revolutionary Embedded Architecture

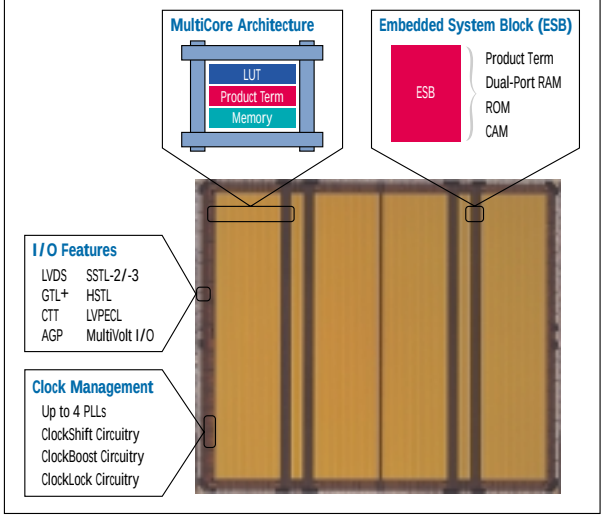
The Altera® APEX™ programmable logic family offers complete system-level integration on a single device. With the innovative MultiCore™ architecture, the APEX family combines and enhances the strengths of previous programmable logic device (PLD) architectures and delivers the ultimate in design flexibility and efficiency for high-performance, the system-on-a-programmable-chip (SOPC) applications.

With densities up to 2.4-million system gates and performance enhancements such as multiple phase-locked loops (PLLs), the APEX device family is designed to be 64-bit, 66-MHz PCI- and PCI-X compliant and can achieve data transfer rates up to 840 Mbits/second. The 2.5-V APEX 20K devices are fabricated on an advanced 0.22-micron, six-layer-metal SRAM process. The 1.8-V APEX 20KE devices, which are a functional superset of the APEX 20K devices, utilize a 0.18-micron, six-layer-metal process.

Breakthrough MultiCore Architecture

The innovative APEX MultiCore architecture contains three types of PLD structures: the look-up-table (LUT) logic of FLEX® 10K and FLEX 6000 devices, the product-term logic of MAX® 7000 devices, and the enhanced embedded memory blocks of FLEX 10KE devices. All three structures are combined into a single integrated architecture, eliminating the need for multiple devices, saving board space, and simplifying the implementation of complex designs.

APEX Device Features



The MultiCore architecture introduces a new level of hierarchy called the MegaLAB™ structure. Each MegaLAB structure contains 16 logic array blocks (LABs) that consist of 10 logic elements each which are used to implement LUT logic, and an advanced embedded structure called an embedded system block (ESB). The MegaLAB local interconnect ties the 16 LABs and the ESB together without using valuable global routing resources. The MegaLAB structures are connected by the FastTrack® Interconnect continuous routing structure for fast, predictable delays.

Embedded System Block Configuration

The embedded system block is the heart of the MultiCore architecture. The 2,048 programmable bits of each APEX ESB can be configured as product-term logic, LUT logic, or one of three types of memory: dual-port RAM, ROM, or content-addressable memory (CAM).

APEX Highlights

FEATURE	BENEFIT
840-MHz data/clock rates	High-speed interface to provide a true system-level programmable solution
MultiCore architecture	Integrates LUT logic, product-term logic, and memory into a single architecture
Embedded system block (ESB)	Implements product-term, LUT, dual-port RAM, FIFO, ROM, and CAM functions
PCI compliance	Meets all specifications for 64-bit, 66-MHz PCI compliance and PCI-X support
Support for emerging I/O standards	Supports LVDS, LVTTL, LVCMOS, GTL+, CTT, AGP, HSTL, LVPECL and SSTL-2/-3 I/O standards
SignalTap logic analysis	Improves verification of chip functionality
Density up to 1.5 million gates (2.34 million system gates)	Addresses system-level density needs
1.8-V and 2.5-V operation	Reduces power consumption
Up to four phase-locked loops (PLLs)	Supports ClockLock, ClockBoost, and ClockShift circuitry, and 0.01x to 133x clock multiplication with an extended frequency range
MultiVolt I/O operation	Ideal for mixed-voltage systems
FineLine BGA™ packaging	Area-optimized, high-pin-count BGA offerings and packaging migration flexibility
Vertical and SameFrame migration	Addresses changing density and I/O needs without the need to re-spin the board

APEX 20K Devices							
Device	Gates	Pin/Package Options[1]	I/O Pins[1]	Supply Voltage	Logic Elements	RAM Bits	Macrocells
EP20K30E	30,000	144-Pin TQFP, 144-Pin FBGA[2], 208-Pin PQFP, 324-Pin FBGA[2]	92, 93, 128, 128	1.8 V	1,200	24,576	192
EP20K60E	60,000	144-Pin TQFP, 144-Pin FBGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin FBGA[2], 356-Pin BGA	92, 93, 148, 151, 196, 196	1.8 V	2,560	32,768	256
EP20K100	100,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 324-Pin FBGA[2], 356-Pin BGA	101, 159, 189, 252, 252	2.5 V	4,160	53,248	416
EP20K100E	100,000	144-Pin TQFP, 144-Pin FBGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin FBGA[2], 356-Pin BGA	92, 93, 151, 183, 246, 246	1.8 V	4,160	53,248	416
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin FBGA[2]	88, 143, 175, 271, 316	1.8 V	6,400	81,920	640
EP20K200	200,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin FBGA[2]	144, 174, 271, 382	2.5 V	8,320	106,496	832
EP20K200E	200,000	208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin FBGA[2], 652-Pin BGA, 672-Pin FBGA[2]	136, 168, 271, 376, 376, 376	1.8 V	8,320	106,496	832
EP20K300E	300,000	240-Pin PQFP, 652-Pin BGA, 672-Pin FBGA[2]	152, 408, 408	1.8 V	11,520	147,456	1,152
EP20K400	400,000	652-Pin BGA, 655-Pin PGA, 672-Pin FBGA[2]	502, 502, 502	2.5 V	16,640	212,992	1,664
EP20K400E	400,000	652-Pin BGA, 672-Pin FBGA[2]	488, 488	1.8 V	16,640	212,992	1,664
EP20K600E	600,000	652-Pin BGA, 672-Pin FBGA[2], 1020-Pin FBGA[2]	488, 508, 588	1.8 V	24,320	311,296	2,432
EP20K1000E	1,000,000	652-Pin BGA, 672-Pin FBGA[2], 1020-Pin FBGA[2]	488, 508, 708	1.8 V	38,400	327,680	2,560
EP20K1500E	1,500,000	652-Pin BGA, 1020-Pin FBGA[2]	488, 808	1.8 V	54,720	466,944	3,648

[1] Preliminary. Contact Altera for the latest information.
[2] Space-saving FineLine BGA package.

Embedded Dual-Port RAM

The APEX ESB supports dual-port RAM with independent read/write ports, synchronous or asynchronous RAM operation, and 192-MHz FIFO performance in a wide range of RAM widths and depths (128 × 16, 256 × 8, 512 × 4, 1,024 × 2, and 2,048 × 1). The APEX ESB also supports 225-MHz cache RAM performance, and ROM performance over 230 MHz. Multiple ESBs can be combined to build wider and deeper memories.

High-Performance CAM

Within APEX 20KE devices, the ESB can also be configured as CAM, a parallel processing memory that facilitates fast address search functions. CAM operates like reverse RAM: while RAM receives an address input and supplies data output, CAM receives data input and supplies the address that contains the input data.

CAM is commonly used in data communication applications. Because the APEX 20KE CAM functions as a high-speed parallel comparator, it opens up many new applications for PLD designs. APEX CAM supports single match multiple match, fast multiple match, and ternary CAM.

CAM Applications	
Address translation	Packet header identification
Cache tagging	Pattern recognition
IP filter	Switch address mapping
MAC address look-up	VPI/VCI translation in ATM switches

Each ESB can be configured as a 32-word × 32-bit CAM, and ESBs can be cascaded to build larger CAMs. The integrated CAM in APEX 20KE devices offers considerable gains in system performance and configuration flexibility relative to discrete CAM solutions.

High-Bandwidth, Low-Voltage I/O

The demand for higher system performance and lower supply voltages is growing. APEX 20KE devices support multiple I/O interfacing standards, including LVTTL, LVCMOS, GTL+, SSTL-3/2, HSTL, AGP, CTT, LVPECL as well as LVDS with performance up to 840 Mbits per second. All APEX devices support the Altera MultiVolt™ I/O interface, which is ideal for mixed-voltage systems.

Enhanced Phase-Locked Loop

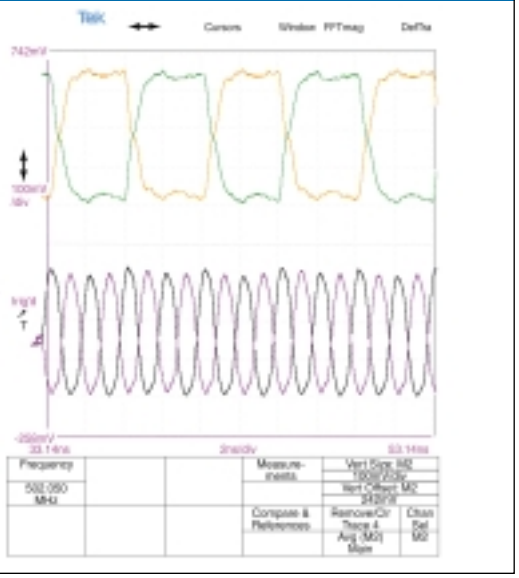
To increase system-clock rates, APEX 20KE devices feature up to four phase-locked loops (PLLs) with enhanced ClockLock™, ClockBoost™, and ClockShift™ circuitry. The ClockLock circuitry uses a synchronizing PLL with an extended frequency range that reduces the clock delay and skew within the device. The ClockBoost circuitry provides a clock multiplier that allows the designer to distribute a low-speed clock and to multiply that clock on the device. The ClockBoost circuitry also allows for resource-sharing within

the device and enhances device area efficiency. The ClockShift circuitry provides a programmable clock delay and phase-shift capability.

High-Bandwidth LVDS Support

APEX 20KE I/O interface meets 840 Mbits per second data transfer rate specifications and supports data transfer rates up to 1 Gbits per second under laboratory conditions. With dedicated built-in LVDS circuitry, the APEX 20KE LVDS supports programmable bandwidths up to 26 Gbps. APEX devices offer the highest performance, highest bandwidth, and the system-on-a-programmable-chip solution for high-speed data transmission design.

APEX 20K LVDS Running at 1 Gbps Data Transfer Rate*

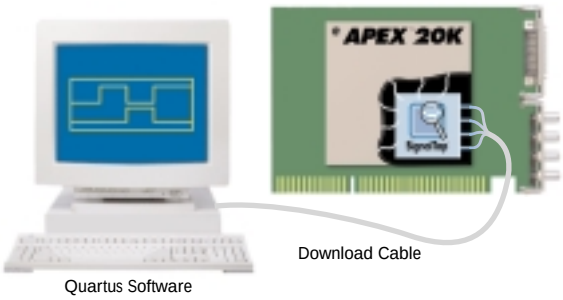


*Data taken under laboratory conditions.

Quartus Development Software & Intellectual Property Simplify Design

Altera's Quartus™ development system allows designers to process multi-million gate designs using advanced features never before seen in PLD development tools. To streamline the development flow and increase productivity, the

SignalTap Logic Analysis Tool



Quartus software supports system-level solutions with block editing, integration with standard source-control software, expanded support for intellectual property megafunctions, and push-button support for advanced device features such as CAM, PLL, and LVDS. The new SignalTap™ logic analysis tool reduces verification time by enabling engineers to see internal chip signal values while the system is running at speed. Enhanced timing analysis tools support designs with single and multiple clocks as well as designs with multicycle paths. Quartus software uses NativeLink™ integration to seamlessly interface with third-party EDA software tools, and is "Internet-aware", providing up-to-the-minute information and file exchanges, software updates, and support services across the Internet. Together these features make the Quartus software the ideal platform for multi-million gate designs.

Contact Altera Today

The APEX device family provides a completely new level of capability and offers a platform for system-on-a-programmable-chip applications. The revolutionary three-in-one MultiCore architecture brings together the power of LUT logic, product-term logic, and embedded memory for system-level integration. Call Altera today to learn more about this multi-million-gate programmable logic family or visit the Altera worldwide web site at http://www.altera.com.

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